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THE DEVELOPMENT OF PASSIVE TRACKING SYSTEM DAF

Final Project Report Mutual Weapons Development Program

Agreement No N-14-MWP-AF-62

NDRE REPORT No S8

Part I

FORSVARETS FORSKNINGSINSTITUTT
Norwegian Defence Research Establishment
PO Box 25 - Kjeller - Norway
May 1964

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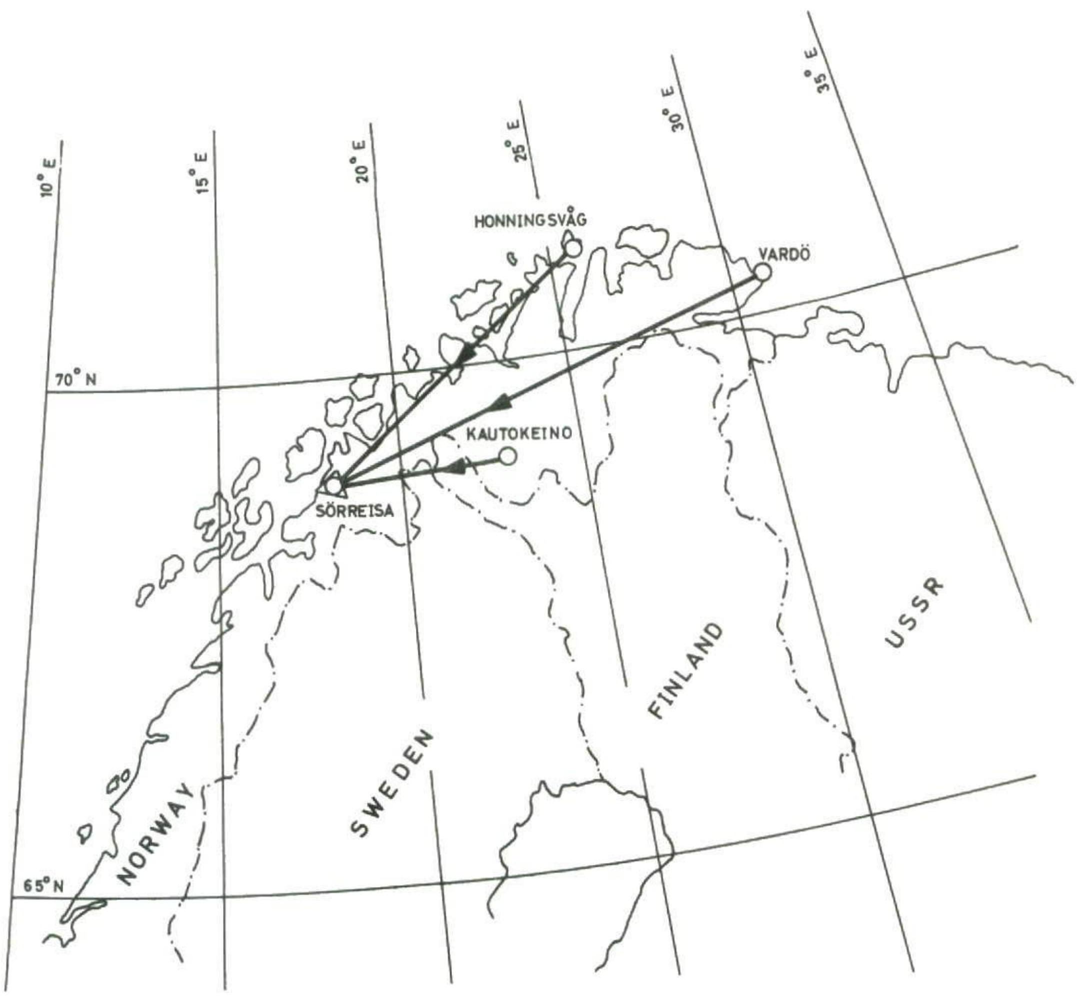
PREFACE

DAF is a passive detection system for the location of jamming aircraft and employs the principles of triangulation. Development of the system was initiated in 1961 as a result of extensive analyses which demonstrated that a potential aggressor could fly over the Northern Region of Allied Command Europe without being located by the Active Air Control and Warning System if he employed a jamming concentration well within his estimated capability.

The project was rather arbitrarily given the neutral code name DAF, the letters having later been interpreted to represent Directions And Fix.

It was originally decided to develop a two-station experimental system to be tested in South Norway. Due to the military importance and urgent problems in North Norway it was later decided to develop a full-scale prototype system embracing the four most northerly stations and fully integrate the central equipment with the semiautomatic radar data display equipment contracted for the local control and reporting centre. The project was in 1960 presented to the Mutual Weapons Development Pro-



The DAF experimental network

O Reporting post and Strobe reporting station
Δ Control and reporting centre and Triangulation centre

gram and has been supported under Agreement No N-14-MWP-AF-62 dated 6 March 1962. The financial and technical support under this contract has enabled our Establishment to accelerate the work and to complete the project in time for implementation under the NADGE plan. We are extremely thankful for all assistance and advice received.

The Royal Norwegian Air Force has also contributed very substantially to the work under the project by providing general guidance and by assistance with personnel. Furthermore, the RNoAF has arranged for operational tests with the system. Again for this we are very thankful.

Within our Establishment the project has been allocated to our Division for Electronics with Mr P T Hiis as chairman for the Project Coordination Board and Mr K Endresen as project leader. To these and to their enthusiastic and devoted colleagues I would also like to express our gratitude for exceptional service.

The present report is divided into the following main parts:

Part I presents in Chapter 1 a brief survey of the military background for the project, together with some very basic principles of triangulation. Chapter 2 gives a condensed description of the DAF system, and concludes with a summary of the main system parameters. Chapter 3 presents the evaluation results.

Part II gives a detailed description of the equipment involved. The description is not intended as a full Technical Order, but rather as a description which should be understood by a maintenance engineer having a fairly good background in regard to semiconductor networks. The reader is not supposed to be familiar with electronic computer technology and terminology.

Part III is an appendix containing the details of the circuit cabling and the printed circuits.

Finn Lied

Finn Lied
Director, NDRE

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THE D A F TRIANGULATION SYSTEM

SUMMARY

The report presents in three volumes a full technical description of a passive detection system for the location of jamming aircraft. The passive system is closely integrated with the active Air Control and Warning System.

1 INTRODUCTION

1.1 The ACE Northern Region Air Control and Warning system and the electronic countermeasure threat

In collaboration with the Royal Air Forces of Denmark and Norway, the Norwegian Defence Research Establishment in early 1960 completed a rather extensive analysis of the Air Control and Warning (AC&W) system in the Northern Region of Allied Command Europe (1). The purpose was to examine the performance of the AC&W system and propose possible improvements for the 1960 - 1970 period in order of priority, in the light of:

a) High and low altitude threat

b) Ballistic missile threat

c) Electronic countermeasures (ECM)

d) Physical vulnerability

e) Cost

It was soon realized that ECM would probably represent the main problem during a possible forthcoming attack, and a very condensed abstract of the findings is given below.

Figure 1.1 indicates the expected radar coverage at 40 000 ft against a light jet bomber (10 m^2 target) when ECM is not used. The coverage is quite satisfactory with good overlap between stations within the greater part of the cover area. At low altitudes, Figure 1.2, the coverage is greatly reduced. The southern part of the region, however, still has a reasonably good overage.

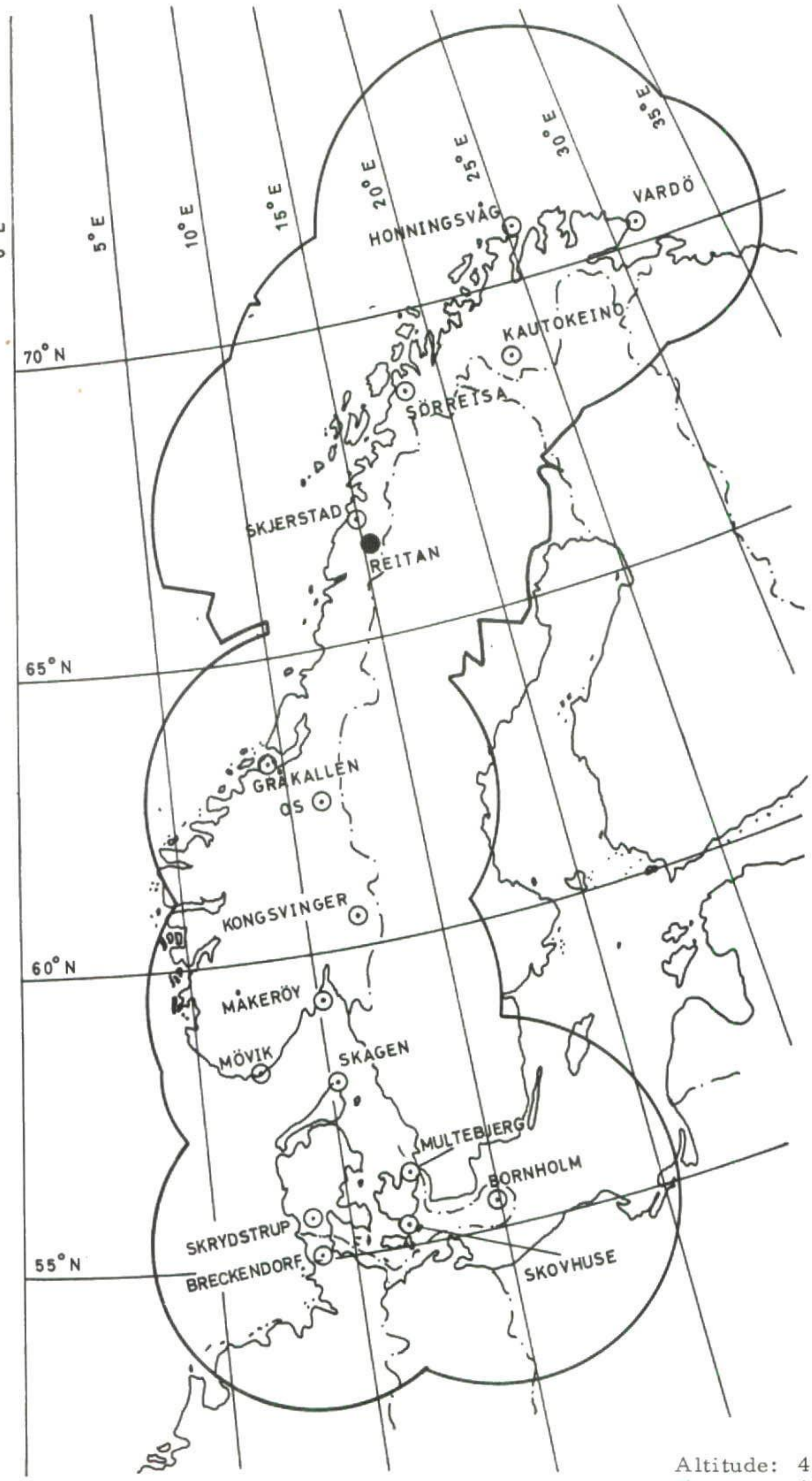
The possible enemy activity is sketched in Figure 1.3. In terms of number of aircraft, the most intense activity may be represented by some 200 - 300 aircraft flying from Baltic bases over the southern part of the region, bound for UK bases. Medium size raids, 20 - 30 aircraft, may cross the Northern Region bound for the Strike Fleet if this is within range. Attacks against targets in Denmark and Norway probably represent the smallest enemy activity.

The ECM threat represented by these aircraft is shown in Table 1.1, which is based on 1959 interpretations. The estimates should be regarded as loose, since no exact information is available. For the following discussion, the estimates must, however, be more than an order of magnitude in error in order to alter the conclusions.

The estimated available jamming power per aircraft is seen to vary between 1 and 5 kW today, and up to 15 kW after 1964.

	Light bomber (Beagle)		Medium bomber (Badger)	
	ECM escort	Bombs and ECM	ECM escort	Bombs and ECM
ECM load, lb	3000	1000	5000	2000
No of jammers	6 (9)	2 (2)	10 (15)	4 (6)
Total jamming power, kW	3 (9)	1 (3)	5 (15)	2 (6)
Chaff, lb	200 (200)	200 (200)	200 (200)	200 (200)

Table 1.1 Possible ECM equipment in Soviet bombers (Figures for 1964- in brackets)



Altitude: 40 000 ft
Target : 10 m^2

Figure 1.1 High altitude coverage of radar stations in the Air Control and Warning System

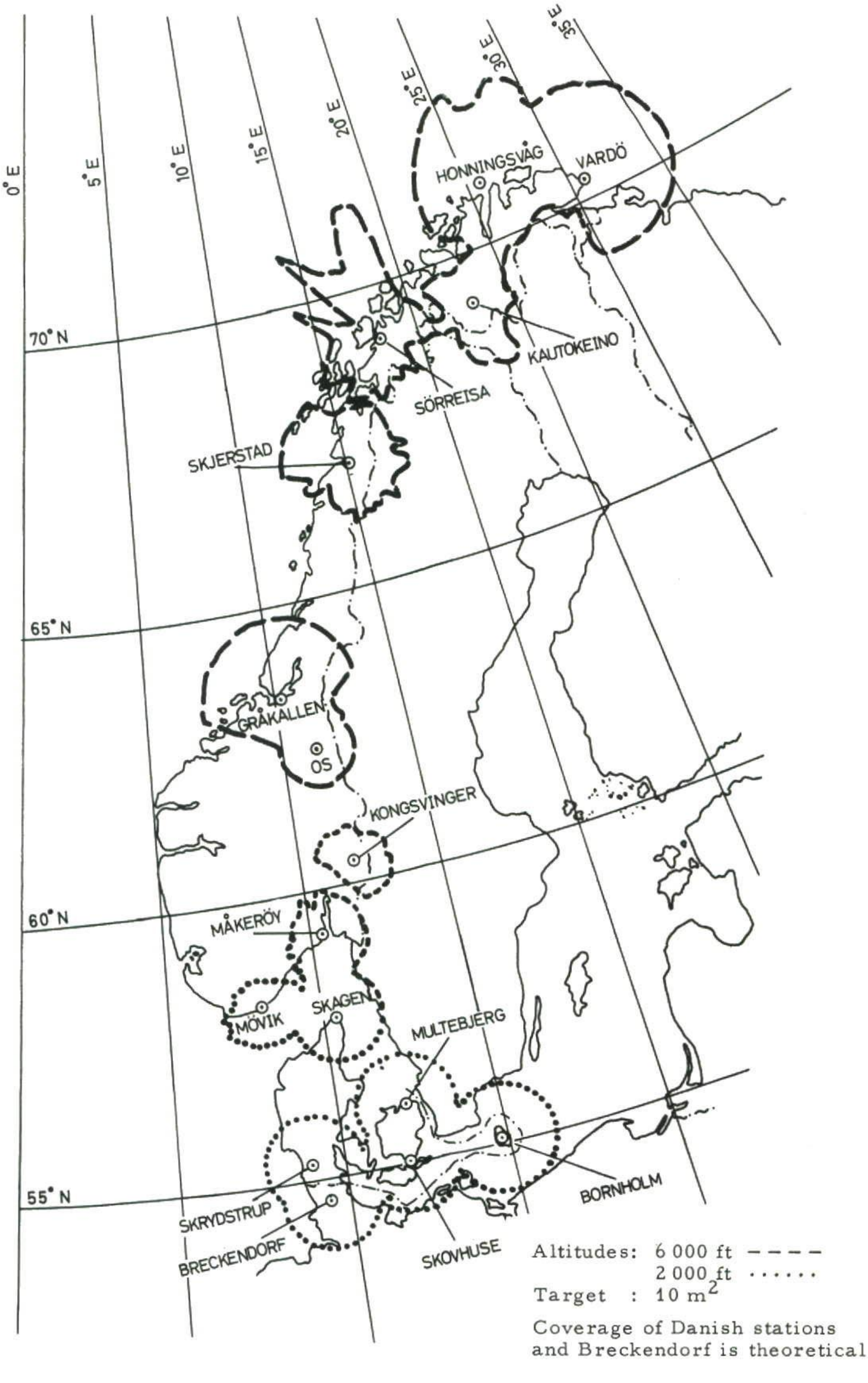


Figure 1.2 Low altitude coverage of radar system in the Air Control and Warning System

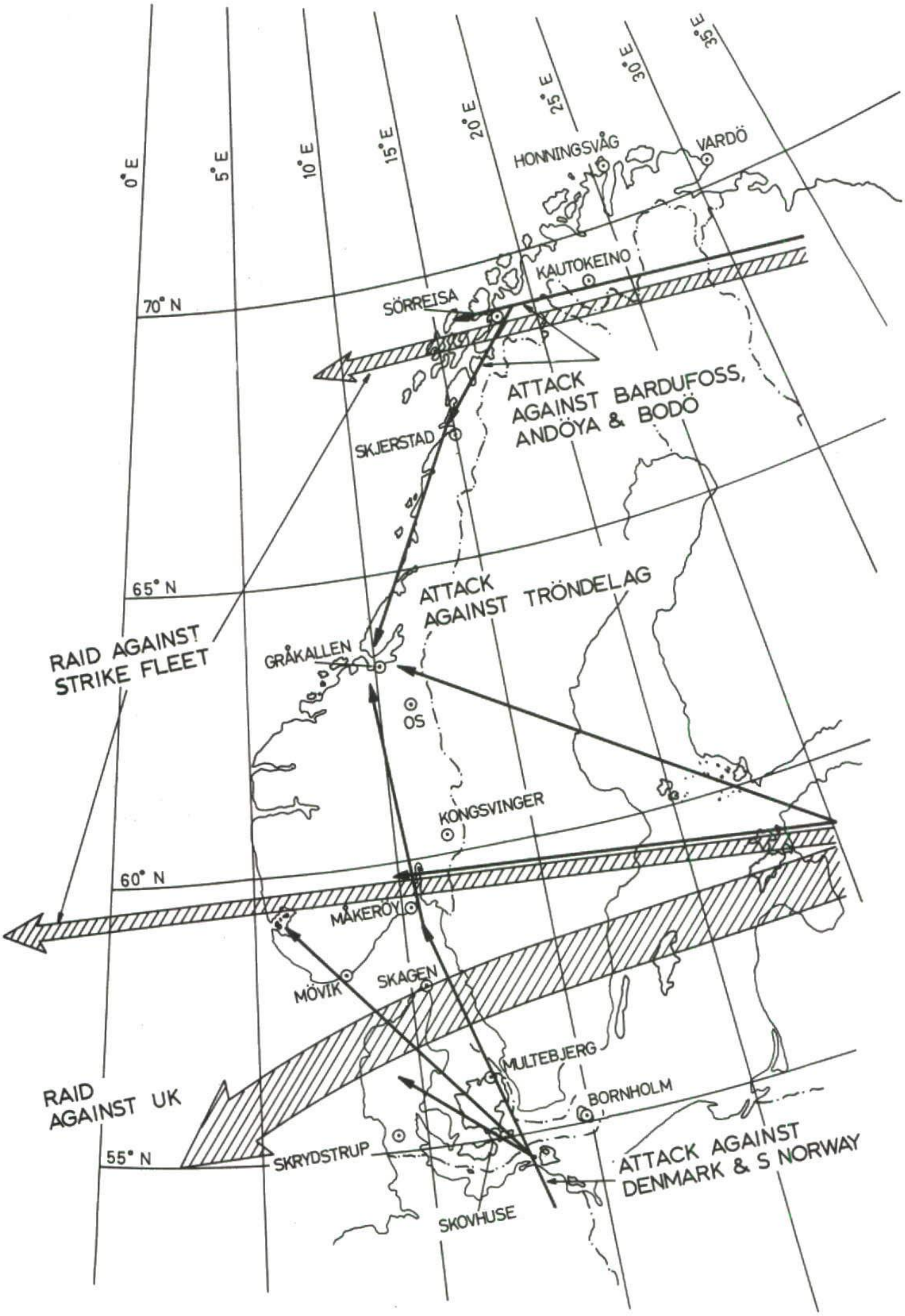


Figure 1.3 Possible attack routes

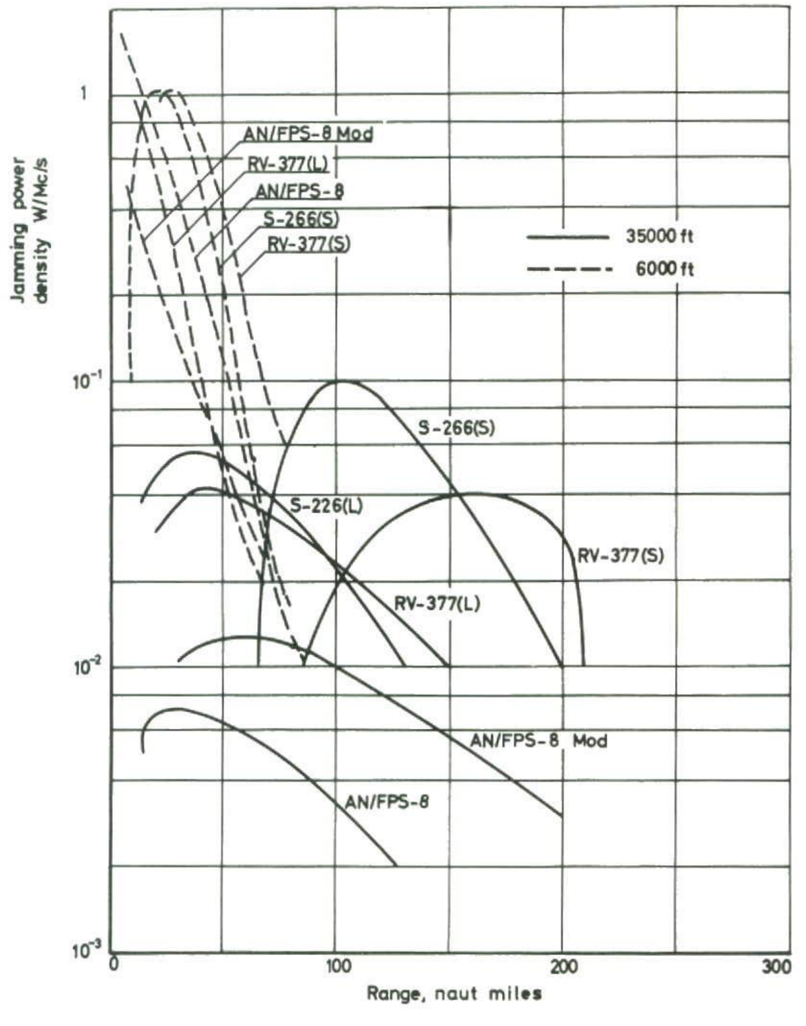


Figure 1.4 Self-screening jamming power density for typical surveillance radars

The figures may be compared with Figure 1.4 showing curves of jamming power intensity in W/Mc/s versus distance required for self-screening against typical surveillance radars. The maximum required power density is seen to vary in the range 0.01 - 1 W/Mc/s dependent upon the radar type and the target altitude. Even if broad barrage jamming over, say, 100 Mc/s is used, a jamming power of 100 W per radar is more than sufficient. As the radar frequencies have been standardized into the narrow L and S bands, one barrage jammer for each of these two bands would suffice in most instances. Comparison with Table 1 thus shows that efficient self-screening requires only a small fraction of the expected capability.

For mutual screening, i e concealment of quiet targets outside the jammer's own sector, higher jammer powers by a factor of 10^3 or more are required, or more sophisticated techniques requiring for example directive and steerable antennas, search receivers and a larger crew must be used.

The above arguments might indicate that self-screening of each aircraft or each close formation would be the rule and mutual screening of distant aircraft by specialist aircraft would be the exception. Available information, however, does not permit any firm deductions to be drawn as to the tactics actually contemplated by a potential aggressor.

The study led to several conclusions. As far as ECM is concerned, the conclusions may be summarized as follows:

a) ECM is the most serious threat. An enemy may blind the system by using only a fraction of his estimated capability.

b) Means for passive detection of jamming aircraft must be provided and integrated with the active radar system.

c) The active radar system must be equipped with specified electronic counter-countermeasure facilities to increase the chances of locating quiet targets in directions different from those of jamming aircraft.

d) Training facilities must be provided for the system as a whole as well as for the individual stations.

e) Alternative routings of early warning messages must be set up.

f) Moderate improvements can restore a broad brush air situation capability. A detailed air situation capability can probably not be restored by reasonable efforts.

1.2 Passive detection system requirements

A passive detection system was found to represent the highest priority. Studies of passive detection schemes in development or in use in other countries revealed that:

a) Automatic correlation schemes, due to the required number of installations, their technical complexity and cost, could not be justified in view of the expected threat and the available weapons.

b) Existing or developmental triangulation systems could not be used for one or more of the following reasons: Operational unreliability, operational mismatch with the active radar system, electronic mismatch with the existing equipment and data links.

It was therefore found necessary to start the development of a new system which could meet the first priority early warning and control tasks and be fully matched to the somewhat diversified operational and electronic background in the Northern Region. The following requirements were established:

a) The system should provide the following data

    Strength (i e number of jamming tracks)

    Approximate positions

    Approximate speeds

    Approximate courses

   The above data are essential for qualified early warning messages to the strategic forces.

b) The operational speed and accuracy should be so high that in case of a light ECM attack a limited weapon control would be possible.

c) The system data should be fully integrated with the active radar data flow.

d) The system should be capable of installation in every NATO and national radar site, whether manual or semi-automatic.

e) Expensive new data links should not be required.

f) Realistic training aids should be an inherent part of the system.

g) Operation should be so simple that normal radar operators could operate the system. This would also ensure flexible manning.

h) The role of the operators should as far as possible be limited to those tasks which an operator's brain can more reliably and readily resolve than can a reasonable quantity of electronic devices.

i) Modern circuit techniques should be used, and special attention should be paid to ease of maintenance.

j) The circuit design should be realistic. Clever solutions which would add complexity, giving diminishing operational returns, should be avoided.

Of the above requirements, the last one was by far the most difficult to meet. Triangulation is by its very nature a simple scheme, but also a very forceful one if it is kept simple. The addition of sophisticated circuitry may well camouflage the simplicity of the basic principles, a net operational profit being obtained only in rare cases. Dozens of proposals for apparently obvious improvements have been ruthlessly rejected during the system planning and development phases, because a careful scrutinization has revealed that they would in fact either reduce the overall performance or add engineering high-lights of no operational value. It is believed that the system as it is now designed has avoided the often well concealed traps of sophistication, without sacrifice to operational requirements, compatibility and reliability.

1.3 Basic principles and limitations of triangulation

Triangulation in the present context implies that the direction to a jammer is determined from two or more geographically separated positions. By plotting these directions on a conformal map at a triangulation centre, the target position is determined by the common intersection.

Figure 1.5 shows a simple example with two stations and two targets. One obtains here the two true target positions (filled circles) plus two false intersections (open circles, ghosts). In this particular example the distant ghost may be eliminated due to an unlikely range. This also eliminates the other ghost.

In Figure 1.6 there are three targets, giving six ghosts. In this case separation of ghosts is more difficult. If, however, a third station can also contribute, the particular situation can be resolved.

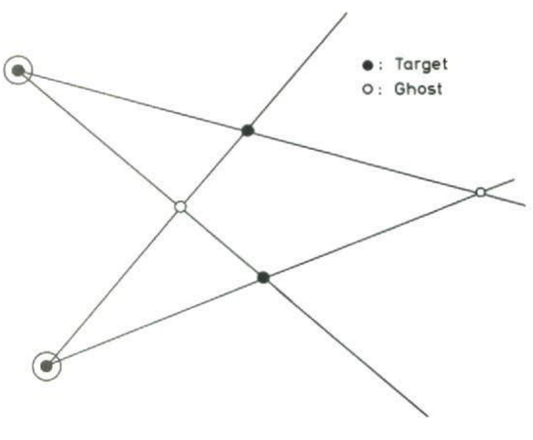


Figure 1.5 Triangulation of two jammers by two stations

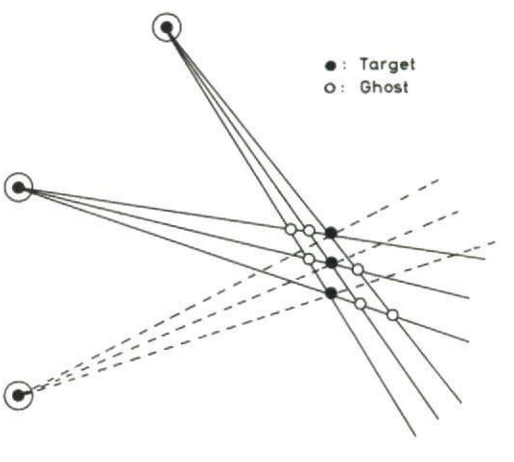


Figure 1.6 Triangulation of three jammers by three stations

Figure 1.7 gives an example where simple logic rules cannot easily be used for resolving the detailed situation. Three stations are taking part. There are three targets on top which are out of range of the lowest station, and six targets to the right direction found by all three stations. Even if all true target positions cannot be unambiguously determined, one can at any rate state that there are at least three targets inside the shaded area on top, and that at least six targets are located inside the shaded area to the right. If the movement of the areas, rather than the individual intersections, are followed for a short while, also the speed categories and the courses may be determined, and these data may be quite adequate for early warning purposes.

If the situation is as in Figure 1.7 or a little more complex, the question might be asked as to whether the best defensive action is to carry out a close interception control, or if some type of loose control or even broadcast control might pay better dividends. The question cannot be answered offhand without a study of the weapons available, and a qualified answer will not be contemplated here.

Figure 1.8 shows as an example a case where a very large number of aircraft are distributed within a 30 nm square. The number of targets is so high that individual direction finding is of little use, and only the outer boundaries of the compactly jammed sector are being defined. In the particular example, the rather crude mass raid sector warning technique employed defines an area which is only some 30 - 40% larger than the true area.

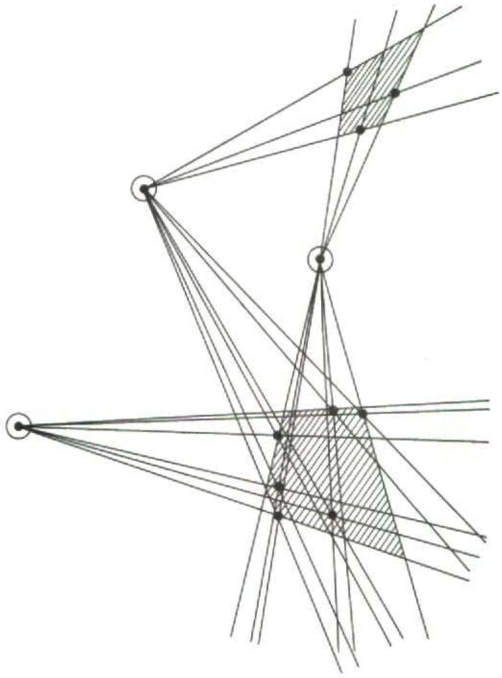


Figure 1.7 Triangulation of semi-dense raids

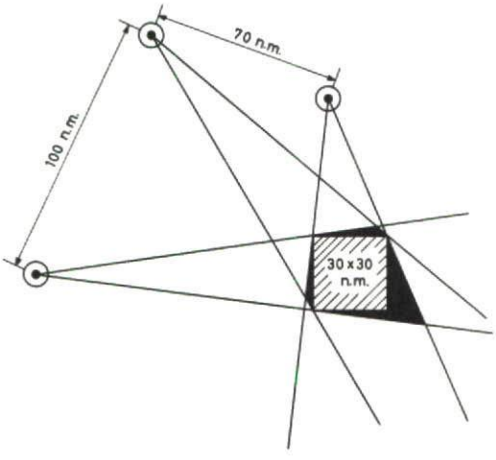


Figure 1.8 Mass raid triangulation

No simple rule can be laid down as to the maximum number of targets which may be resolved as individual tracks. This number is obviously determined by several factors which include direction finding accuracy, aircraft speed, configuration of strobe reporting stations, and operator skill and experience. Results from studies in other countries indicate, however, that as a rough rule of the thumb some 6 - 8 aircraft represent a maximum when three stations are cooperating, and this rule has been supported by the experience gained with the DAF system.

It is of extreme importance that this basic limitation is appreciated in the system design. For this reason the maximum number of individual strobes to be transmitted from a given strobe reporting station has been purposely limited to ten, even though the technical design in itself lends no restrictions. The basic philosophy has been that in the case of overdense raids, the strobe reporting operator shall be forced to transmit sectors rather than individual strobes. The operator will do so by transmitting sector boundaries and informing electronically or verbally that certain strobes represent sectors.

It is of equal importance to realize that a triangulation operator will occasionally mistake ghosts for real targets. A strobe presented at the triangulation table should therefore be of such length that it represents the maximum range at which a jammer might possibly be intercepted. The operator should be forced to study intersections along the entire length of the strobe, and should not have the possibility of shortening a strobe outside the intersection he has decided is a target. Otherwise, he might be at a complete loss when he at some instant discovers that a mistake has been made.

Facilities for electronic computation of intersection speeds with a view to discriminating between targets and ghosts are in general of no use. In the majority of cases a ghost turns out to have an apparent speed which differs from the speed of an actual target by an amount which is less than the possible spread in actual target velocity.

It is extremely difficult, or rather, impossible, to lay down strict rules as to the criteria to be used by an operator in selecting the correct intersections under semi-dense conditions. Systematic training using mixtures of synthetic and live exercises under different conditions, however, leads to rules which are rapidly grasped by the operators, even if the rules cannot be formulated into a standard list. The experience gained in the DAF project indicates that with realistic training aids operator training is much less of a problem than was originally anticipated.

Reference

(1) - An analysis of the 1960 - 1970 Air Control and Warning System in the Northern Region, Intern rapport IR-S-02, Norwegian Defence Research Establishment (1960)

2 GENERAL SYSTEM DESCRIPTION

This section contains a rather brief and generalized description of the DAF system, mainly in block diagram form, together with some of the underlying ideas for the main technical solutions chosen. The detailed technical description is deferred to Part II.

2.1 Main principles

In Figure 2.1 an area containing four radar stations (reporting posts A - D) is indicated. Each station has a normal radar antenna and normal plan position indicator (PPI) displays for the data acquired by the active radar.

At an intermediate stage in the normal radar receiver, an output is fed to a strobe reporting station (SRS). In case of jamming the jamming directions will be presented on a cathode ray tube displaying amplitude versus azimuth (AVA). An operator selects the proper direction and transmits semi-automatically the direction information to a central strobe receiver (CSR) usually colocated with one of the radar stations, where all jamming directions are automatically displayed from proper geographic origins on a triangulation table. By studying intersections an operator identifies the jamming target positions and feeds positional data into an integrated active/passive data system.

Under quiet conditions aircraft within radar range will be detected by the active radar. When jamming takes place, quiet aircraft outside jammed sectors may still be detected by the active radar system. Jamming aircraft will be located by the passive system. All acquired target positions will be displayed by the same system.

Each strobe reporting station has the capability of transmitting up to ten discrete directions.

The entire system is transistorized, and modular printed circuit card modules have been used throughout. All circuits are "worst case" designed for operation within an ambient temperature range between -26°C and +55°C.

2.2 Strobe reporting station (SRS)

Figure 2.2 depicts a strobe reporting station, and in Figure 2.3 are shown the main blocks composing the stations. The various blocks will be briefly discussed below in Sections 2.2.1 - 2.2.5, and the principles of operation outlined in Section 2.2.7. Section 2.2.6 describes training methods using simulation.

2.2.1 Direction finding receiver

When a radar antenna scans a jamming target, the received jamming strength will vary in accordance with the polar diagram of the antenna as plotted on a vertical cone having a half cone angle β equal to the complement of the aircraft elevation angle α, see Figure 2.4.

Some parameters for L-band radars in Norway are as given in Table 2.1. The figures for the average sidelobe levels are loosely estimated to be about 10 dB below isotropic gain.

On a normal plan position indicator (PPI) the scanning spot is brightened whenever the received signal exceeds a given threshold. Figure 2.5 shows four examples of PPI presentations in the presence of a single jammer of various strength. If the PPI operator knows for certain that there is only one jammer present, he can use his display for direction finding by reducing the receiver gain. When there are more than one jammer present, the PPI presentation is, however, so crude that the operator is faced with an impossible task in evaluating the number of jammers and their directions.

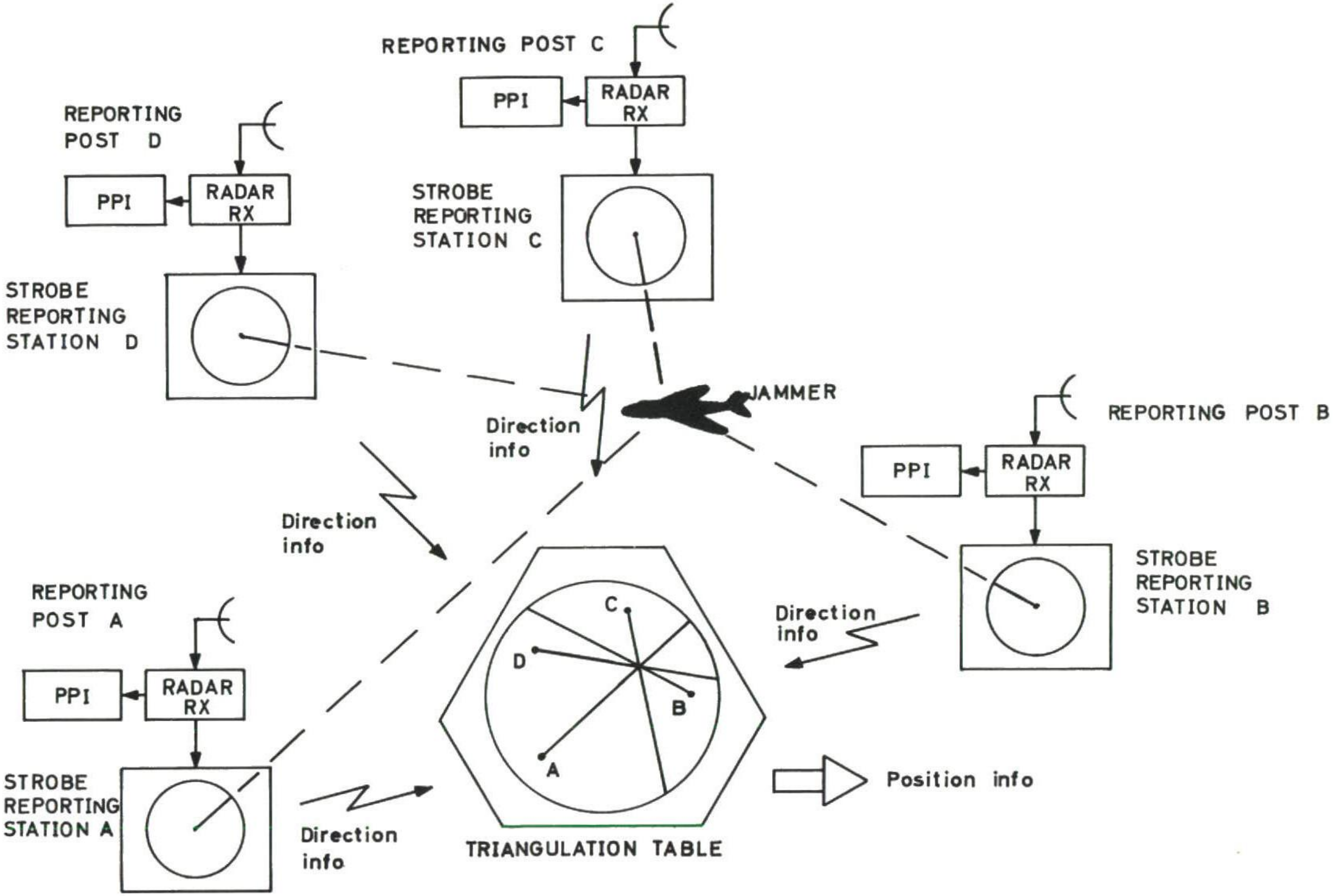


Figure 2.1 Triangulation principle

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Figure 2.2 Strobe reporting station SRS-1

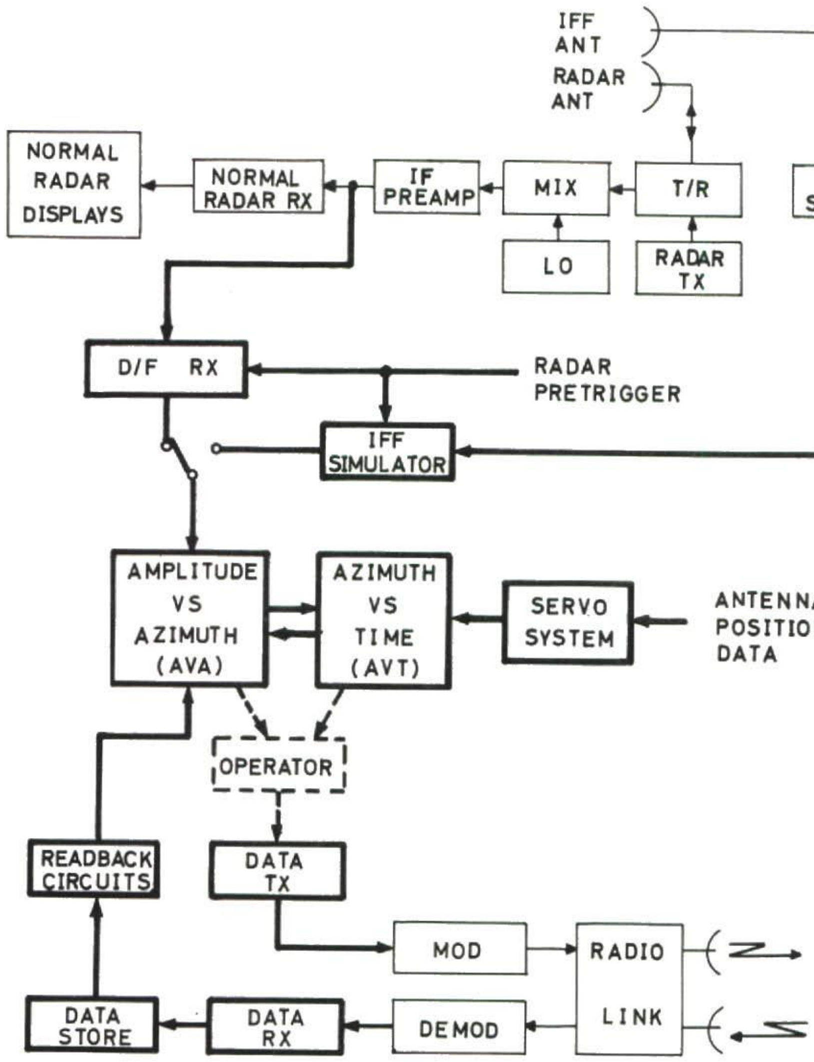
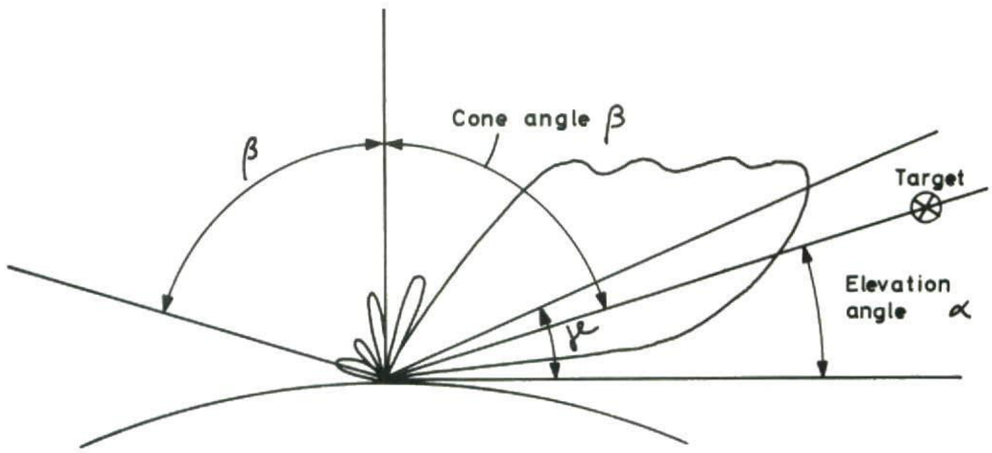


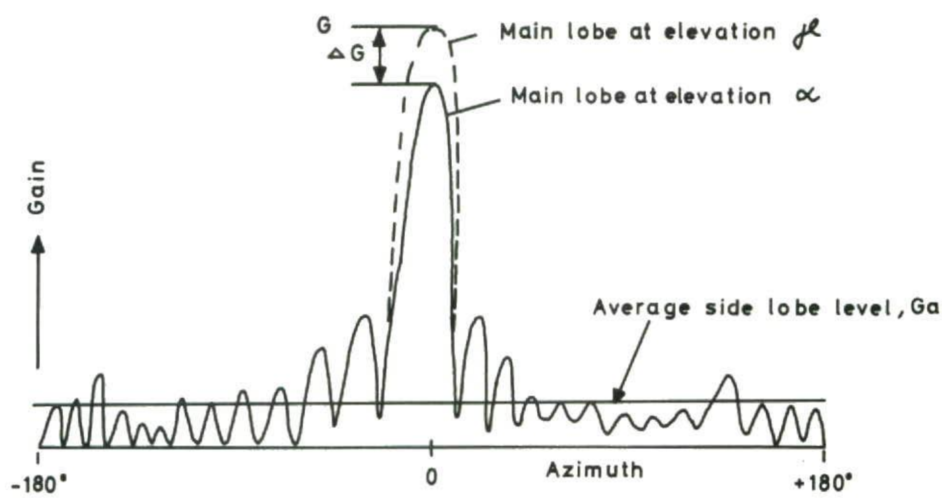
Figure 2.3 Block diagram of strobe reporting station SRS-1

	AN/FPS-8	S-247 S-266
Main lobe isotropic gain G	30.5 dB	36 dB
Side lobe level $G - G_{ns}$		$\geq$24 dB
Back radiation level $G - G_b$		$\approx$60 dB
Average sidelobe level $G - G_a$	40 dB	46 dB
Main lobe width at 3 dB points	2.5°	1.1°

Table 2.1 Main L-band antenna parameters



a) Vertical cover diagram



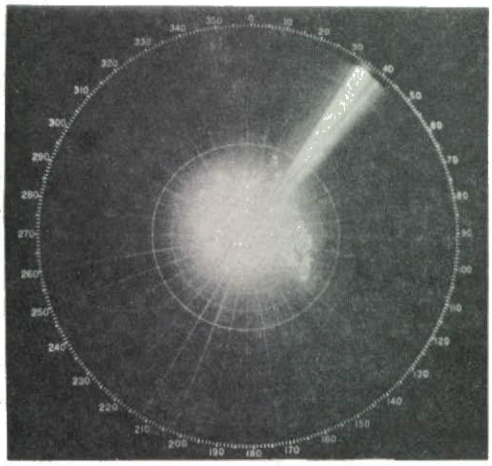
b) Polar diagram as observed on cone

Figure 2.4 Polar diagram

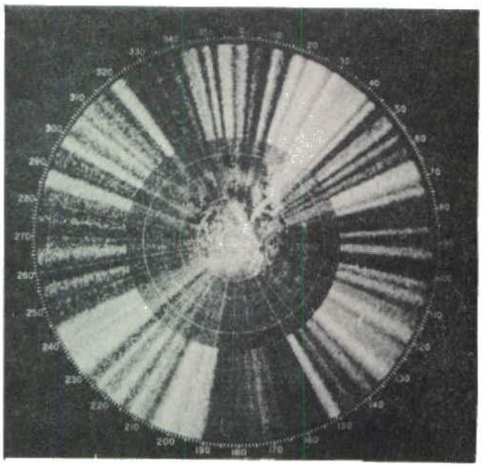
A better, and probably the best, solution is to have a display presenting the jamming strength versus azimuth as indicated in Figure 2.6. In this case one preserves the basic resolution capability provided by the radar antenna. Such a presentation must be essentially logarithmic in order that the resolution capability shall be independent of jamming strength.

The direction finding receiver in Figure 2.3 is shown in more detail in Figure 2.7. The jamming signal is picked up by the radar antenna and is fed to the DAF input through the first radar IF preamplifier. It is next attenuated to provide a convenient working level and then amplified in a gated preamplifier. After logarithmic detection, the output is smoothed in an integrating circuit.

As an example Figure 2.7 gives some essential parameters for the S-247 and S-266 L-band radars. The equivalent input noise level (receiver noise) can be calculated as



a)



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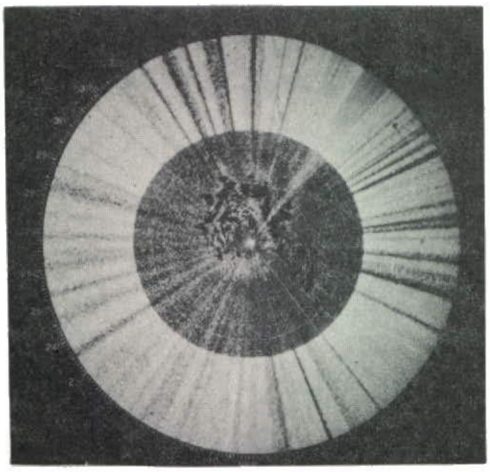
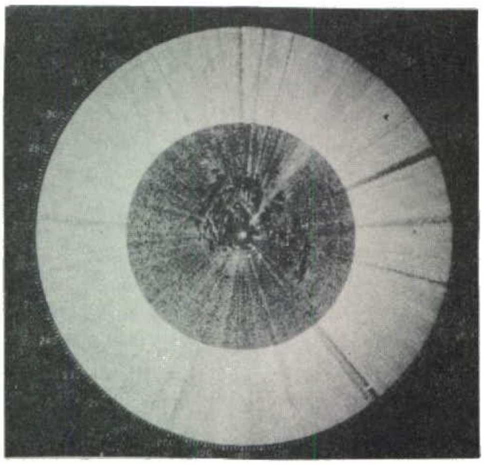


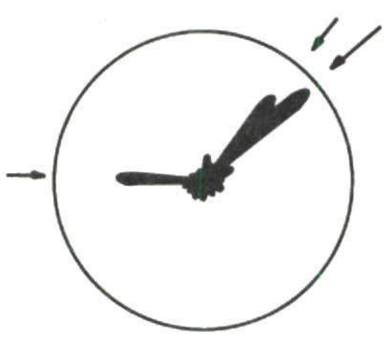
c)



d)

Figure 2.5 Effect on PPI of a single airborne jammer at various distances
Note: MTI used in pictures b-d.

a) One jammer



b) Three jammers

Figure 2.6 Amplitude versus azimuth display of jammers

$$P_{i,n} = 1.1 \cdot 10^{-14}\ W \quad (\approx -110\ dBm)$$

The maximum unlimited signal output level of the IF preamplifier (valve amplifier) is approximately

$$P_{o,s} \approx 1\ W \quad (= 30\ dBm)$$

which corresponds to an input signal level

$$P_{i,s} \approx 10^{-7}\ W \quad (= -40\ dBm)$$

or some 70 dB above the equivalent receiver input noise level.

This leads to the following expression for the maximum unsaturating jamming power density

$$p_j G_j \leq 0.55\ R^2 \qquad (2.1)$$

where p_j = jamming power intensity (W/Mc/s)
G_j = jamming antenna gain
R = jamming distance (nm)

Some practical figures are given in Table 2.2.

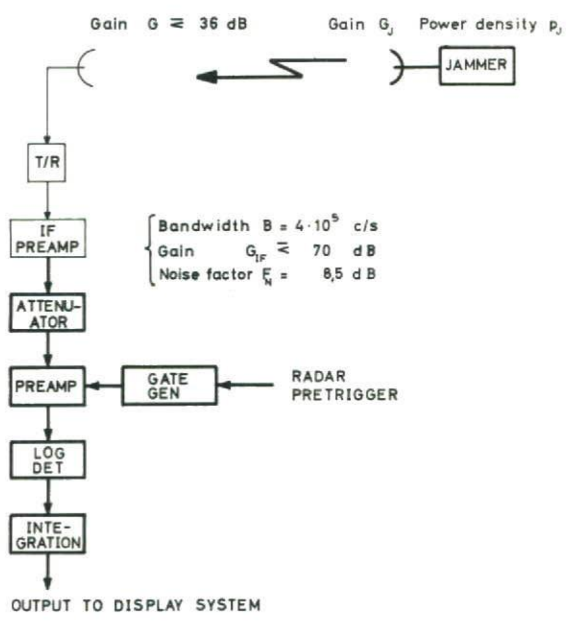


Figure 2.7 Block diagram of SRS direction finding receiver

During each radar sweep strong ground clutter responses occur as indicated in Figure 2.8. Typical ground clutter ranges for Norwegian sites are up to 40 nautical miles and in some cases up to 90 nautical miles. These responses must be prevented from reaching the logarithmic detector, as otherwise the average ground clutter strength would be superimposed on the desired polar diagram pattern. The preamplifier is therefore gated off in synchronism with the radar trigger during the initial part of each radar sweep.

The logarithmic detector consists of eight IF amplifying stages. Detection takes place in each stage and the eight detector outputs are added. The detector is essentially logarithmic over a 50 dB input range.

To prevent amplitude modulation of the jamming power from obscuring the jamming polar diagram, the detector output is integrated by an RC network of time constant about 10 ms. Modulation frequencies above about 20 c/s will therefore not essentially influence the polar diagram patterns.

Jamming range (nm)	10	20	30	50
Jamming intensity x Jamming antenna gain (W/Mc/s)	55	220	505	1375

Table 2.2 Maximum unsaturating jamming power intensity (Radar sets S-247 and S-266)

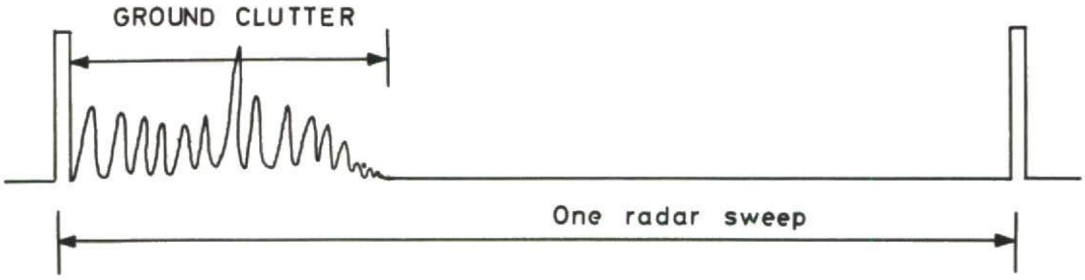


Figure 2.8 Ground clutter region

2.2.2 Display system

Figure 2.9 shows the main blocks of the display system.

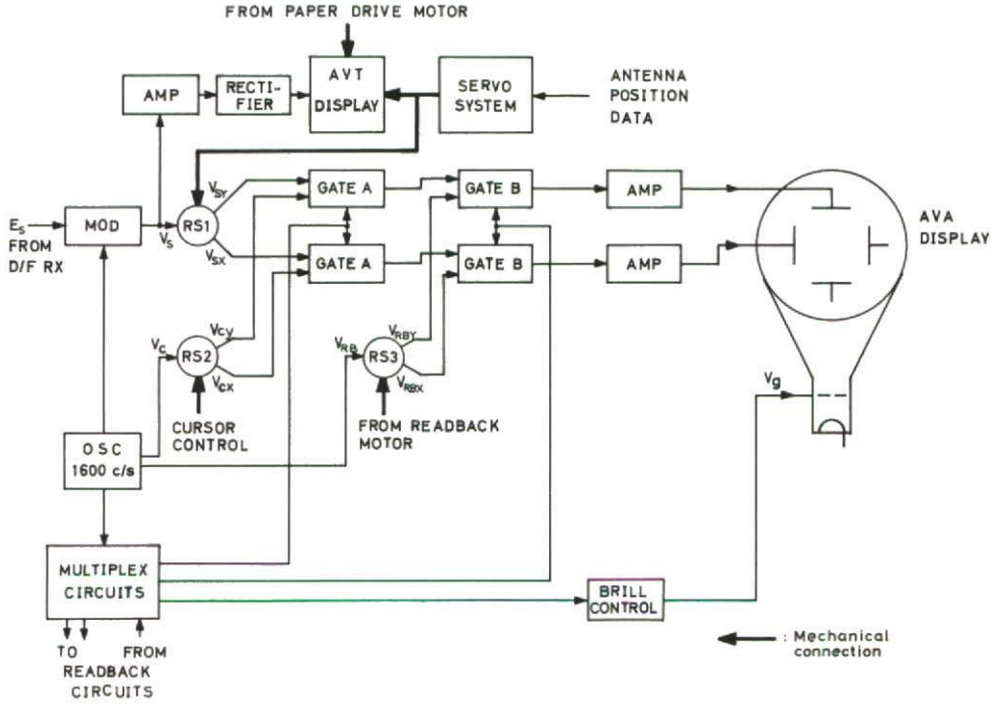


Figure 2.9 Block diagram of SRS display system

The DC signal from the direction finding receiver is fed to a modulator, the output of which is a 1600 c/s sine wave of amplitude proportional to the DC input signal. The sine wave is fed to an amplifier followed by a rectifier and thereafter to the recording mechanism of an 11" Alden recorder (AVT display). The recorder consists of a single turn helical wire wound on a cylinder, the rotation of which is slaved to the antenna movement by means of a servo system. The helix runs underneath the recording electrochemical paper. Above the paper is a straight knife, and as the helix rotates one obtains through the paper a contact point between knife and helix moving linearly from left to right. During operation the paper will be darkened in proportion to the applied electric signal and will display jamming strength as intensity modulation versus azimuth as shown in Figure 2.10.

Mechanically ganged to the servo system is also a resolver RS1. The input is fed from the signal sine wave and it provides two sine wave outputs of amplitudes proportional to sin φ and cos φ respectively, where φ is the antenna azimuth angle.

Each output is fed through two gates and an output amplifier to one set of deflection plates on a long persistence cathode ray tube. Without blanking the CRT would therefore display a straight line through the CRT centre at an angle φ, the length of the line being proportional to the logarithm of the antenna input signal, see Figure 2.11. By means of blanking pulses V_g derived from multiplexing circuits, the display of one half of the line is suppressed. When the antenna rotates, the CRT paints the polar diagram, making the CRT an amplitude versus azimuth (AVA) display.

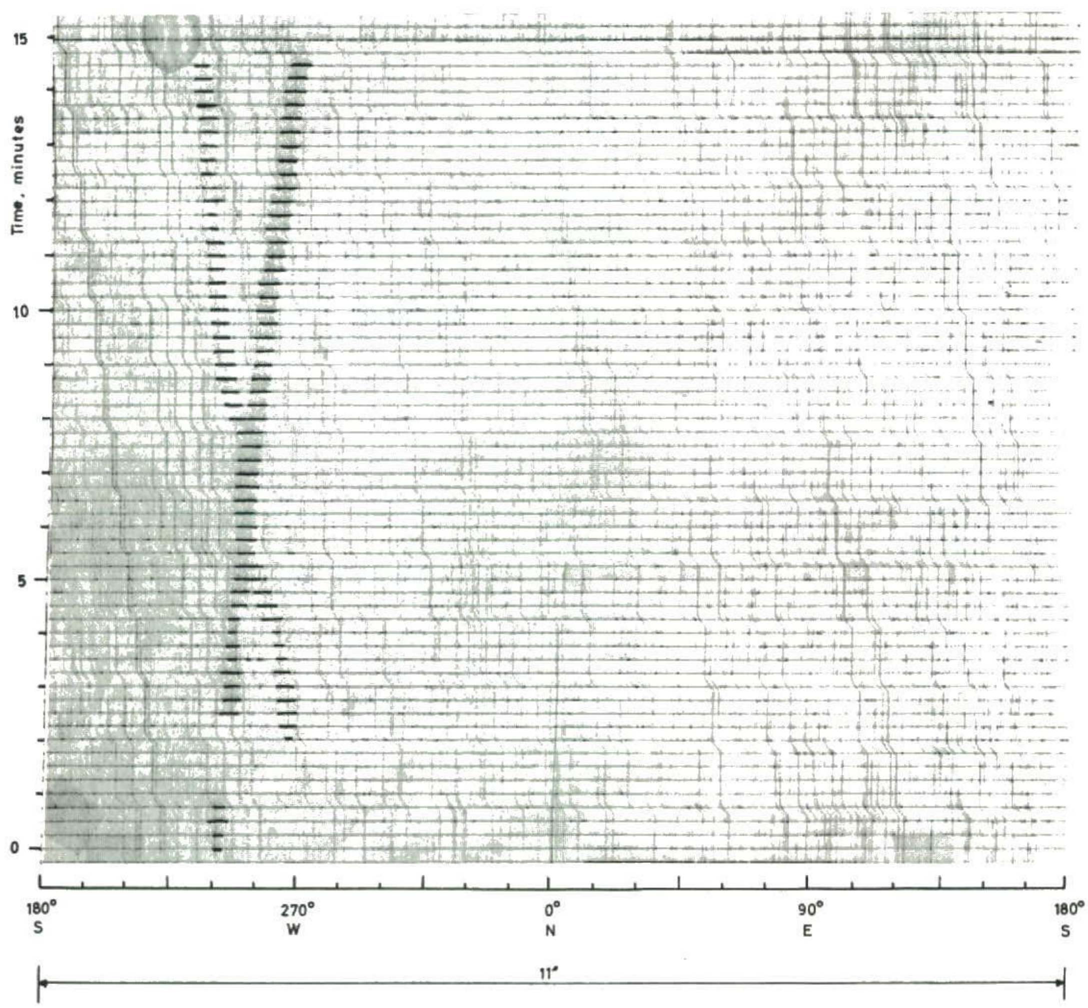


Figure 2.10 Azimuth versus time recording of intercepting fighters (IFF simulation)

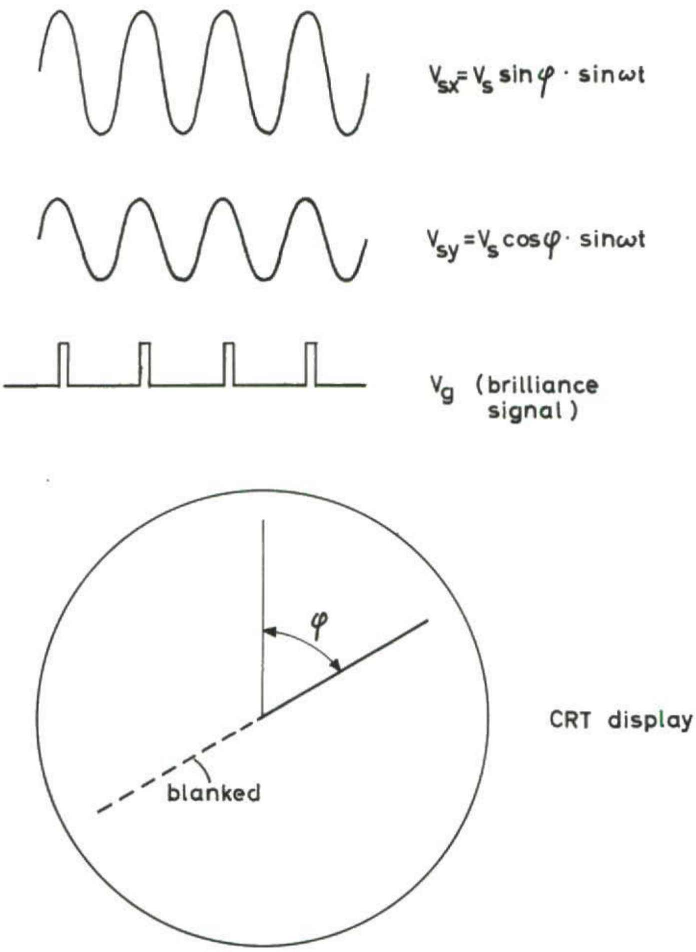


Figure 2.11 Display method

Another output of the oscillator feeds resolver RS2 with a constant amplitude waveform V_c. The outputs V_{cx} and V_{cy} are fed to second inputs of gates A. Gates A are controlled from the multiplex circuits, in such a manner that the V_s and V_c signals are alternately permitted through the gates in a certain time sequence. When gates A are open for the V_c signals, the CRT displays a cursor of constant length at an angle determined by the position of resolver RS2.

Under normal operation gates A switch between the signal V_s and the cursor V_c every 5 ms (making 100 complete cycles per second).

The cursor resolver RS2 is controlled by a handwheel, or by means of pedals. The operator can thus orientate the cursor in any desired direction on the CRT.

The brightness level of the cursor can be controlled independently of the signal brightness. RS2 is mechanically ganged to a digital disc encoder which will be discussed in Section 2.2.3.

A third resolver RS3 is also fed from the oscillator, and the resolver rotor is driven by a synchronous motor. Its outputs are normally blocked in gates B. Whenever the orientation of the resolver rotor coincides with positions in a local store (see Section 2.2.5) pulses from the multiplexing circuits open gates B for readback signals, and simultaneously block signals arriving from gates A. Constant length strobes will therefore appear at their appropriate angles whenever RS3 is in certain orientations. The amplitude is normally adjusted such that the readback strobes are slightly longer than the cursor strobe.

2.2.3 Data transmitter

Mechanically ganged to resolver RS2 in Figure 2.9 is an analog-to-digital shaft encoder (ADE), Figure 2.12.

Nine digits are used to represent the position of the resolver rotor angle, which again directly represents the angle of the cursor on the cathode ray tube, giving altogether $2^9 = 512$ increments throughout the range 0 - 360°. The angle is thus quantized in increments of $360/517 = 0.703^\circ$ which gives an rms quantizing error of $0.73/\sqrt{12} = 0.2^\circ$.

The encoder is of the so-called V-scan type, employing a double set of brushes, and a special information readout unit is required to convert the encoder output to nine binary digits $\varphi 1$ - $\varphi 9$.

The particular combination 000 000 000 is used as an erase message (see below), and is not permitted as an angle message. An "all zero" converter has therefore been introduced converting an all zero combination of the ADE into 000 000 001. All other combinations will remain unmodified.

Two sets of ten push-buttons are provided. When an information button, say No 4, is pressed, the following events take place:

A pulse flips a flip-flop lighting a lamp located inside information button No 4 (if button No 4 has been used previously, the lamp is lit beforehand). The binary angle information is transferred to a shift register together with a five digit address (A1 - A5) designating the number of the button pressed. A time sequence generator starts shifting the register information out in a certain sequence. This output is combined with a code frame and fed to the line modulator (ref Figure 2.3).

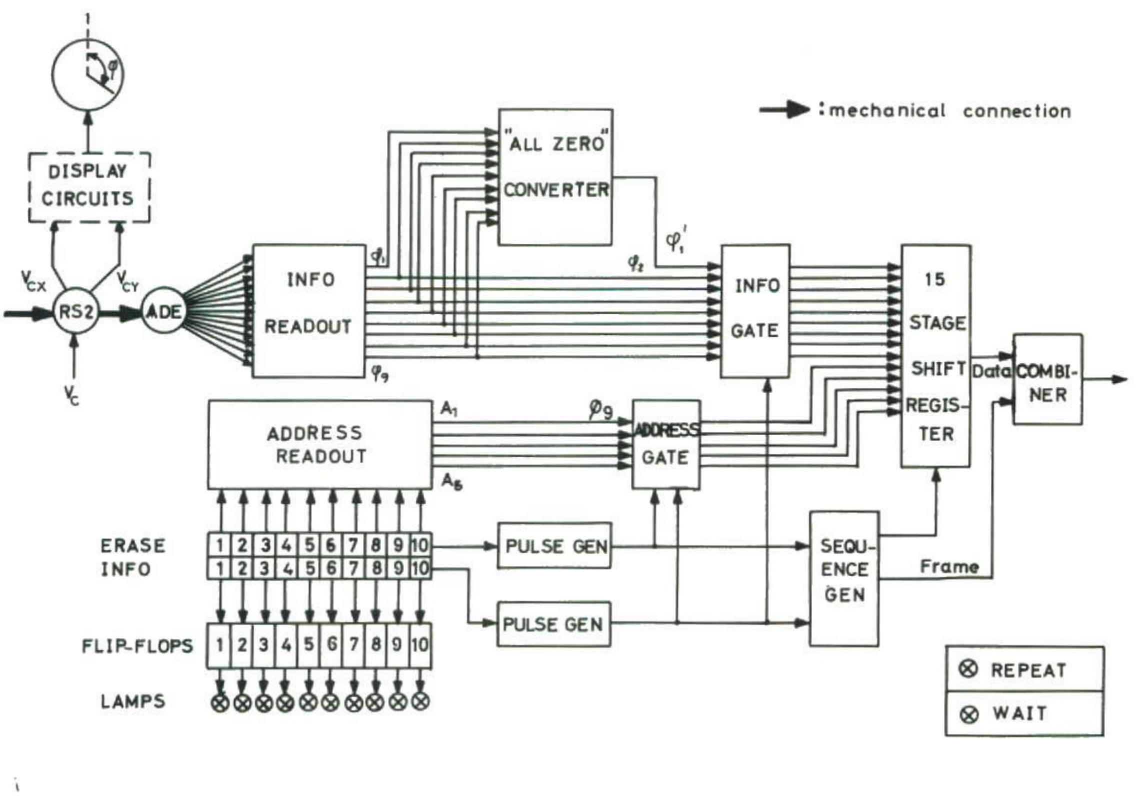


Figure 2.12 Block diagram of SRS data transmitter

If instead erase button No 4 had been pressed, a pulse would have reset the corresponding flip-flop, turning off the lamp. The information gate would have received no trigger pulse, and therefore an all zero combination would have replaced the $\varphi 1$ - $\varphi 9$ information, having the effect that the information previously transmitted via button No 4 would have been erased. The other operations would proceed as above.

Whenever a button is pressed, an arrest circuit (not shown in Figure 2.12) is initiated while the message is being transmitted. During this time a yellow sign showing WAIT is lit. If the operator presses another button while the WAIT sign is illuminated, the last message will be inhibited, and a red sign labelled REPEAT is lit, indicating to the operator that he must repeat the last message.

As code is used the international five-element start/stop teleprinter code, ref Figure 2.13. Each character is composed of a start pulse (a space pulse of 20 ms duration), five pulses of 20 ms each which may each be either a ONE (Mark) or a ZERO (Space), and a stop pulse (Mark) lasting 30 ms.

Three characters are used, ref Figure 2.14. The first character contains the address (i e No of button pressed) in a three-out-of-five code, i e out of the five digits three are always ONE's.

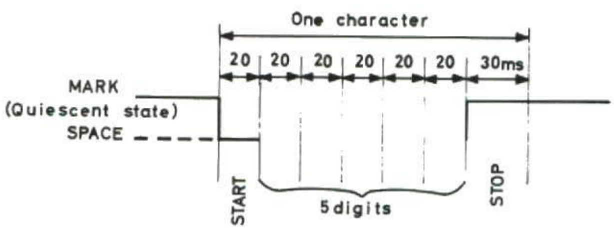
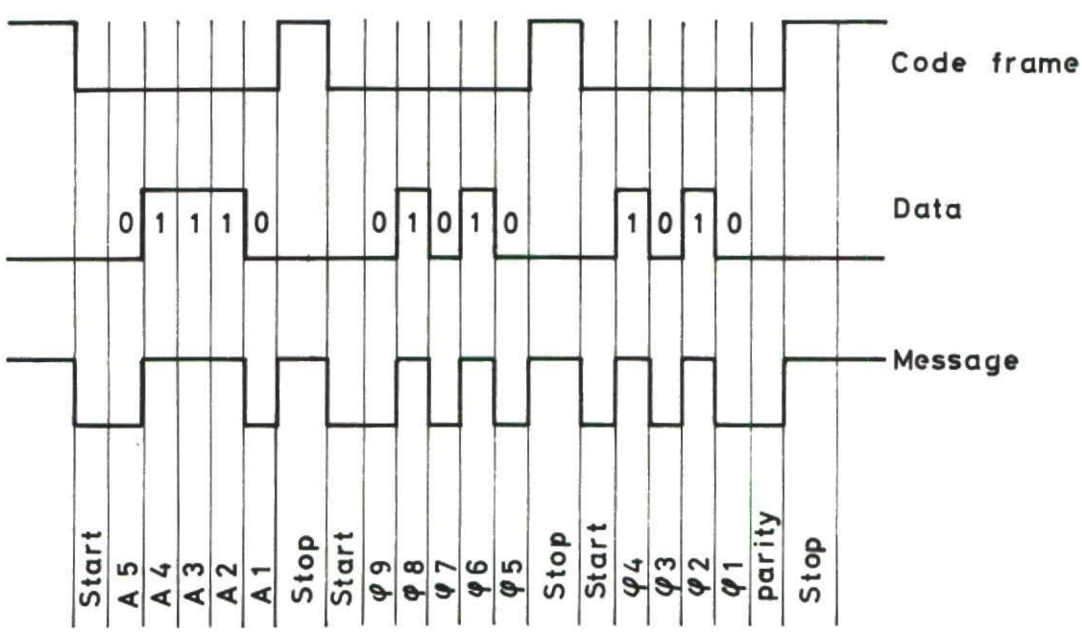


Figure 2.13 Teleprinter code



Message: Address: 01110 (≡ button No 4)

Angle : 010101010 ($= 170$ increments $= 170/512 \cdot 360 = 119.5^{\circ}$)

Parity : 0

Figure 2.14 Typical message

Button No	Address code				
	A5	A4	A3	A2	A1
1	0	0	1	1	1
2	0	1	0	1	1
3	0	1	1	0	1
4	0	1	1	1	0
5	1	0	0	1	1
6	1	0	1	0	1
7	1	0	1	1	0
8	1	1	0	0	1
9	1	1	0	1	0
10	1	1	1	0	0

Table 2.3 Address code convention

The convention chosen (ref Table 2.3) provides a protected code which is used for error detection as described in Section 2.2.4.

The following character contains the five most significant angle digits $\varphi 9$ - $\varphi 5$, and the third character contains the remaining four digits.

The last digit position is used for parity checking. During transmission the number of ONE's is counted. If the angle information is found to contain an odd number of mark elements, a ONE is added at the end of the message. If the number is even, a ZERO is added. This feature is used for first order angle error detection at the receiving end.

A complete message takes 450 ms. With ten buttons an ideal operator would require 4.5 seconds for a full updating. One antenna revolution takes 10 - 15 seconds, and it is seen that the limiting operational speed is governed by the radar antenna (and the operator) and not by the code selected.

Due to the curvature of the earth, the local North directions will not appear parallel when presented on the central triangulation table. In the experimental system the analog-digital shaft encoders are therefore adjusted in such a manner that the digital information employs the North direction at the centre as a reference.

2.2.4 Data receiver and store

The messages from the strobe reporting station are transmitted on a normal teleprinter channel to the central strobe receiver for central display. For check purposes the messages are also fed in closed loop on a return channel back to the strobe reporting station, ref Figure 2.3.

Figure 2.15 presents a simplified block diagram of the receiving system. After proper demodulation the received teleprinter signals are fed to a pulse length discriminator (PLD) which identifies the first start pulse if its duration exceeds 10 ms and initiates a train of pulses in a sequence control unit, ref Figure 2.16. A shift pulse is fed to a 15 bit shift register at the beginning of each data pulse. At the centre of each data pulse a pulse is fed to a gate preceding the shift system, sampling the input signal and setting the shift register input stage accordingly. The data contained in the input signal will thus be sampled at the centre of each pulse, and the sampled information will be shifted from left to right in the shift register.

During the first character the number of ONE's is counted in an address checking

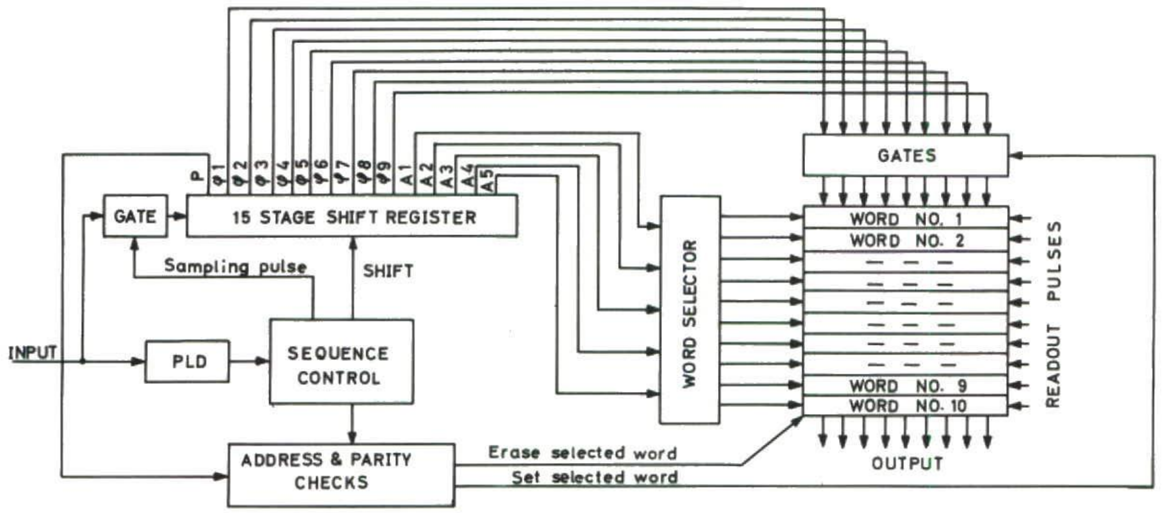


Figure 2.15 Block diagram of SRS data receiver and store

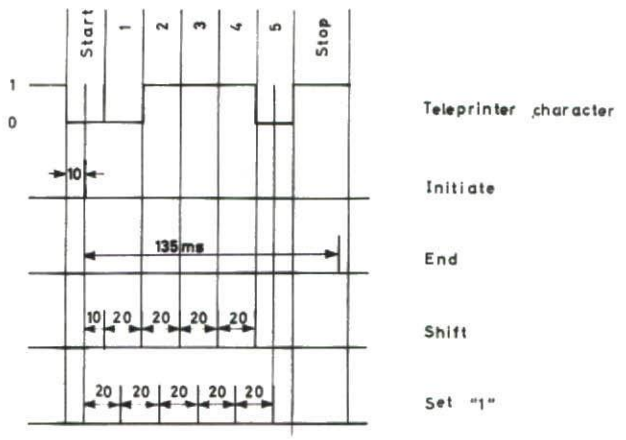


Figure 2.16 Data receiver sequence

circuit. If the number is different from three, indicating that the address character is incorrect, the address checking circuit is automatically reset.

If the address character is approved, the sequence is allowed to proceed if the next character contains a correct start pulse, otherwise the system is reset. A new pulse train is generated as above, and at the end of the second character shift register stages 1 - 10 will be filled with the received information.

If the third teleprinter start pulse is lacking, the control and checking circuits are reset. Otherwise the process continues in a manner similar to that for the second character.

At the conclusion of the third (and last) character, the date contained in the shift register will be located as shown in Figure 2.15. The number of ONE's contained in the last two characters has been continuously counted. If the number is odd, the angle information must be incorrect and the system is reset. If the number is even, an erase pulse is first fed to the store word selected by the word selector shown in the figure. Immediately afterwards a set of gates is opened, furnishing the new information to the selected word position.

The word positions in the store are labelled in accordance with the push-buttons described in Section 2.2.3.

The store words can be selected and read out by means of readout signals as indicated.

2.2.5 Readback circuits

In order to provide the operator with facilities to check whether errors have occured in the transmission path, and also to make it easy for him to decide when previously transmitted directions require updating, the strobe information stored in his local store is displayed on the cathode ray tube. The principles used for readback are shown in Figure 2.17.

From the multiplexing circuit (ref Figure 2.9) a 400 c/s waveform is derived which through an amplifier drives a motor M3 having a synchronous speed of 8000 rpm. Through a gearbox resolver RS3 is rotated at a speed of 187.5 rpm. The resolver primary is fed with a 1600 c/s sine wave, and with the speed chosen it takes $512 = 2^9$ full 1600 c/s cycles to complete a 360° rotation.

A 9-bit counter is simultaneously driven by 1600 c/s counting pulses. The state of the counter at any given instance will therefore in digital form be a true representation of the corresponding RS3 orientation at the same moment.

After every counting pulse, each locally stored word is selected in sequence and compared with the state of the counter. If a full coincidence between the counter and a word is found, a trigger pulse is fed back to the multiplexing circuit, giving rise to a control pulse which blocks the other inputs to gates B and opens gates B for one cycle of the RS3 signal. Every stored word will thus be displayed 187.5 times per minute, or approximately three times per second. With the convention chosen a store combination 000 000 000 is taken to represent "no information", and not a North direction. Empty word positions are therefore not presented as readback strobes.

In order to provide a correct reference, a North pulse is provided to reset the counter. The reference pulse is obtained by means of a light source, three rotating discs mechanically ganged to the resolver rotor, and a photocell.

Each disc is provided with a small hole. The discs rotate at different speeds, and all three holes will be in line only when the resolver rotor is in the North position.

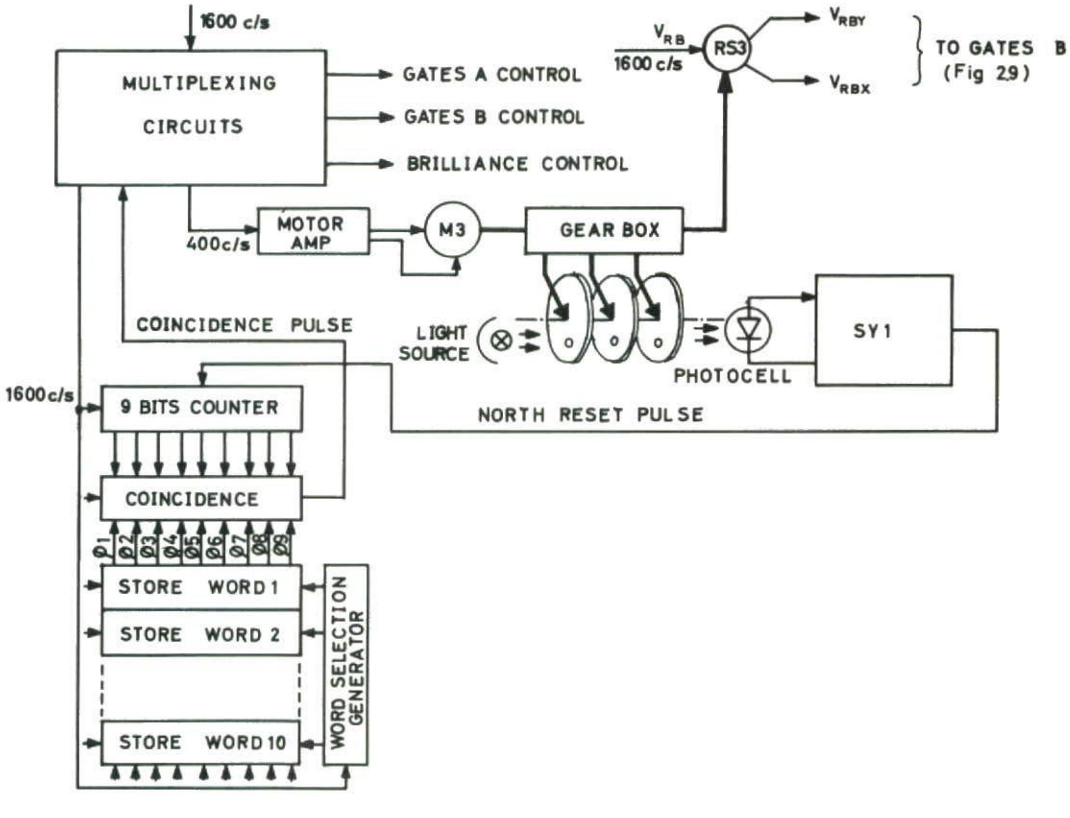


Figure 2.17 Block diagram of SRS readback system

2.2.6 Simulation schemes

Three schemes for training the strobe reporting centre are available:

a) Jamming simulation

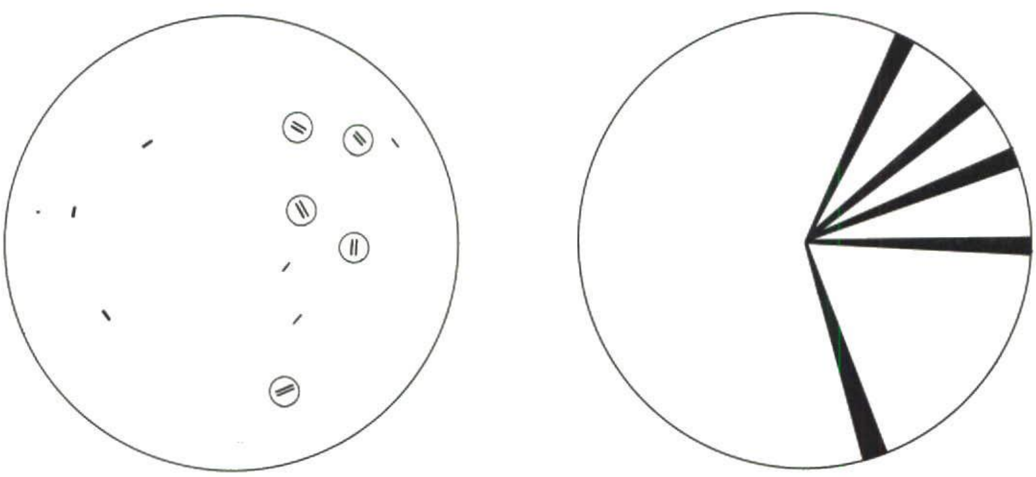
By means of small jamming simulators of types Lukkøye and Dalila, which are available, various complex polar diagram displays (as shown in Figure 2.6) can be set up on the amplitude versus azimuth display. It is also possible to add the jamming from a small airborne jammer Luna to the picture.

b) IFF simulation

In Figure 2.3 a simulator connected to the IFF system is indicated. When the switch is turned to IFF simulation, IFF mode 1 is automatically requested. In the simulator every IFF return turns on a flip-flop circuit which is in turn switched off by the following radar pretrigger. By suitable circuitry a DC output pulse is obtained lasting as long as IFF returns are present. This pulse is then used to modulate the display system, thereby providing IFF strobes, ref Figure 2.18.

c) System training programs

The strobe reporting station can be connected to any system training program equipment which is geared to the antenna rotation and provides unlimited jamming signals on an IF or a DC level.



a) Normal PPI picture (IFF returns encircled)

b) IFF returns strobed

Figure 2.18 IFF responses used for jamming simulation

2.2.7 Operation

When jamming occurs, the operator is faced with a combination of antenna polar diagrams on the cathode ray tube, Figure 2.19. He decides from experience which lobes are true main lobes representing directions to jammers. Starting from North working clockwise, he aligns his cursor with the centre of the first lobe and presses information button No 1. The button is thereby lit, and the selected direction is transmitted to the central strobe receiver and returned. If the received message is unmutilated by noise, it will be approved by the receiving equipment, and a readback strobe will appear in the direction of the cursor. If correct readback does not occur, the operator repeats the operation. He next proceeds to

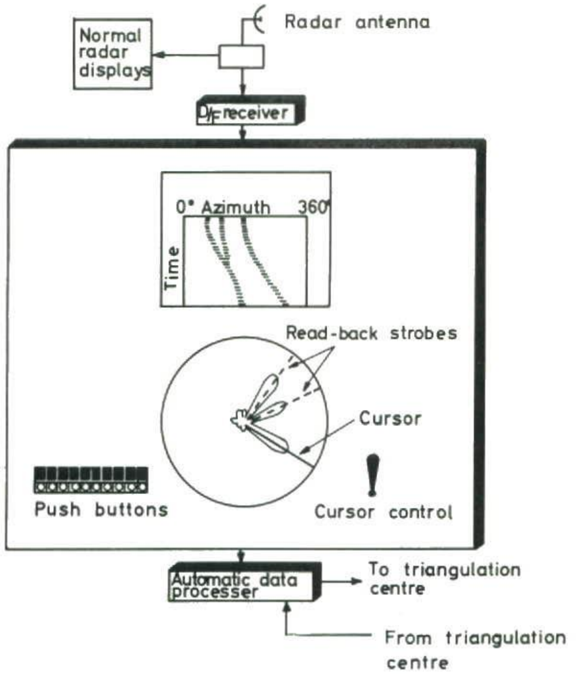


Figure 2.19 Strobe reporting station, operation

the second main lobe, the readback strobe remaining at its original position. He then repeats the procedure, employing button No 2, and a second readback strobe appears.

In a similar manner all main directions are selected.

As time passes the directions of the main lobes will alter in accordance with the movement of the jamming aircraft. Whenever the operator notices a discrepancy between a given lobe and the direction information previously inserted, he aligns his cursor with the new direction and presses the same button as was previously used for the strobe. The readback strobe immediately moves to the new direction, indicating that proper updating has taken place.

When a jamming strobe disappears the operator presses the corresponding erase button, thereby removing the readback strobe. The light in the appropriate information button is extinguished, indicating that the button is free.

2.2.8 Test facilities

Various test facilities are located underneath a lid on the operator's desk. Indicator lamps present the following information:

- Digital angle and address
- Data flow out of transmitter
- Data flow into receiver
- Data contained in each store position

In addition, certain test routines can be selected. A central voltmeter is used to measure essential DC voltages.

When a fault occurs, the control desk facilities are used for an approximate location of the fault, and in some cases even the faulty card can be identified.

For detailed fault finding, test points are available at the outer end of each printed circuit card. These test points are accessible when the side covers of the cabinet are removed.

Normal maintenance procedure will be to locate the faulty card and have it replaced with a card from a local card library. Defective cards will usually be maintained centrally.

The cards have a mechanical indexing system, making it physically impossible to insert a card in a wrong position.

2.3 Central strobe receiver (CSR)

The central strobe receiving and data processing equipment is shown in Figure 2.20 and the triangulation table in Figure 2.21. Figure 2.22 gives a simplified block diagram of the equipment.

2.3.1 Strobe receivers and stores

The CSR receives strobe messages from one local and three remote strobe reporting stations (SRS) over normal teleprinter channels, each message comprising three teleprinter characters. The received information is fed to local receivers (RxA - RxD) in Figure 2.22, and also back to the originating stations for checking purposes.

The receivers and stores are identical to the ones described in Section 2.2.4, to which reference is made.

2.3.2 Digital sine table and digital-to-analog converters

Each store contains up to ten digital angles consisting of nine digits in a straight binary code. For display purposes the angles must be converted into analog sine and cosine voltages.

In order to determine the sine and cosine of any angle between 0° and 360° a sine table covering only 0 - 90° suffices, according to the usual trigonometric rules

$$0^\circ < \varphi < 90^\circ \qquad \begin{cases} \sin\varphi = +\sin\varphi \\ \cos\varphi = +\sin(90^\circ - \varphi) \end{cases}$$

$$90^\circ < \varphi < 180^\circ \qquad \begin{cases} \sin\varphi = +\sin(180^\circ - \varphi) \\ \cos\varphi = -\sin(\varphi - 90^\circ) \end{cases}$$

$$180^\circ < \varphi < 270^\circ \qquad \begin{cases} \sin\varphi = -\sin(\varphi - 180^\circ) \\ \cos\varphi = -\sin(270^\circ - \varphi) \end{cases}$$

$$270^\circ < \varphi < 360^\circ \qquad \begin{cases} \sin\varphi = -\sin(360^\circ - \varphi) \\ \cos\varphi = +\sin(\varphi - 270^\circ) \end{cases}$$

In the present case the 360° angle is determined by $2^9 = 512$ increments, each increment representing 0.703°. A table giving $\sin\varphi$ versus φ in increments, including only φ values between 0 - 128 increments may therefore be used to determine all sine and cosine values between 0 - 512 increments if logical rules similar to those above are used.

The sine table in Figure 2.22 is made according to the above principles. The table consists of 128 main ferrite cores. Each core represents a certain angle, and is selected by a set of input wires. It has also eight output wires representing the digital sine value of the particular angle. When the input wires are pulsed, output pulses occur on certain of the output wires corresponding to the digital sine value.

For a given angle the binary sine and cosine values are selected in turn. The outputs are then fed to digital-to-analog converters delivering the proper analog voltages to the triangulation display.

A multiplexing equipment is fed with clock pulses from the main distributing equipment of the station. All ten word positions of store A are sampled and displayed in turn, then the words of store B are sampled, and so forth. If a word contains the angle 000 000 000, this is interpreted by the sine table as an erase message, and a blanking pulse is generated preventing its display.

A keyboard control panel provides selective strobe erasure facilities. When a given push-button is pressed, the readout of the corresponding store word is suppressed and replaced by a 000 000 000 combination, whereby the strobe is blanked.

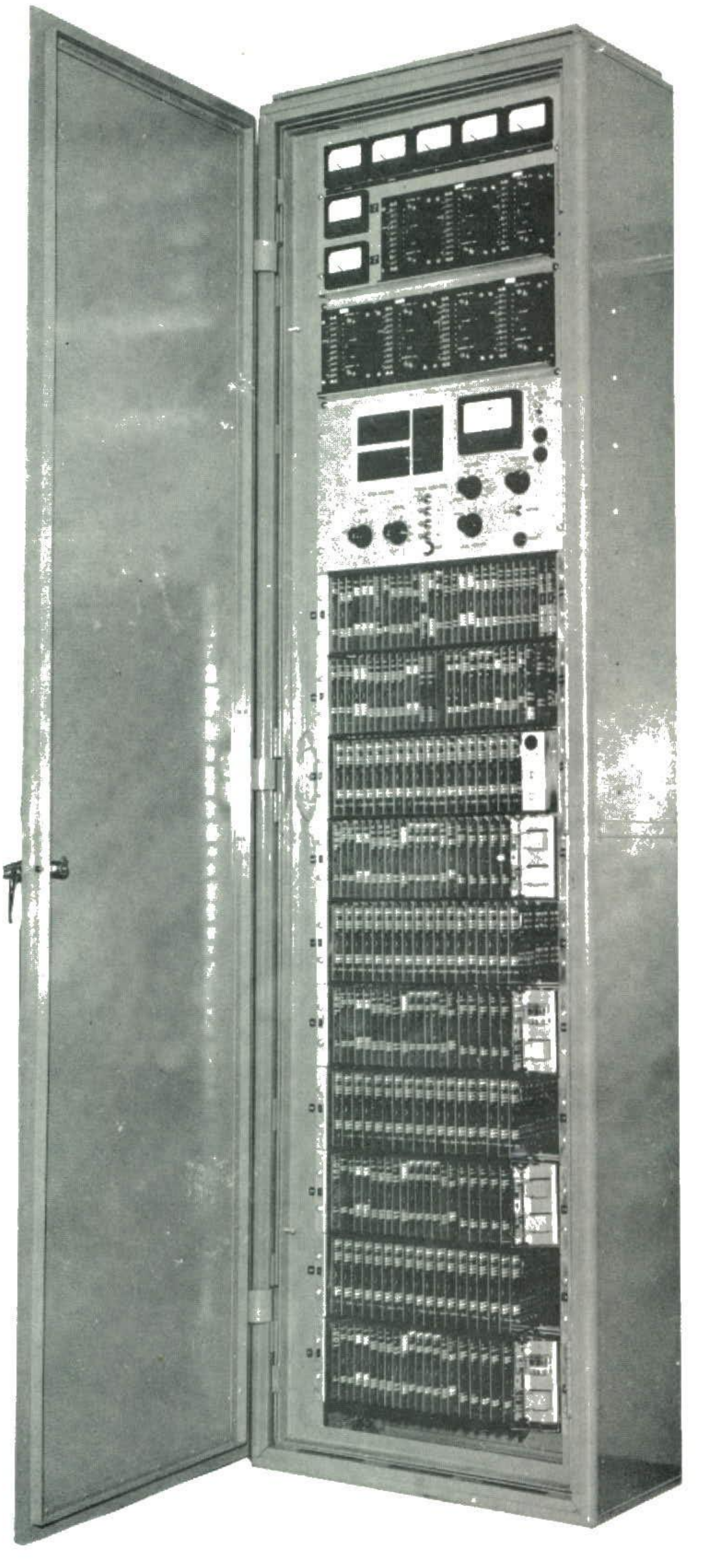


Figure 2.20 Central strobe receiving equipment CSR-1

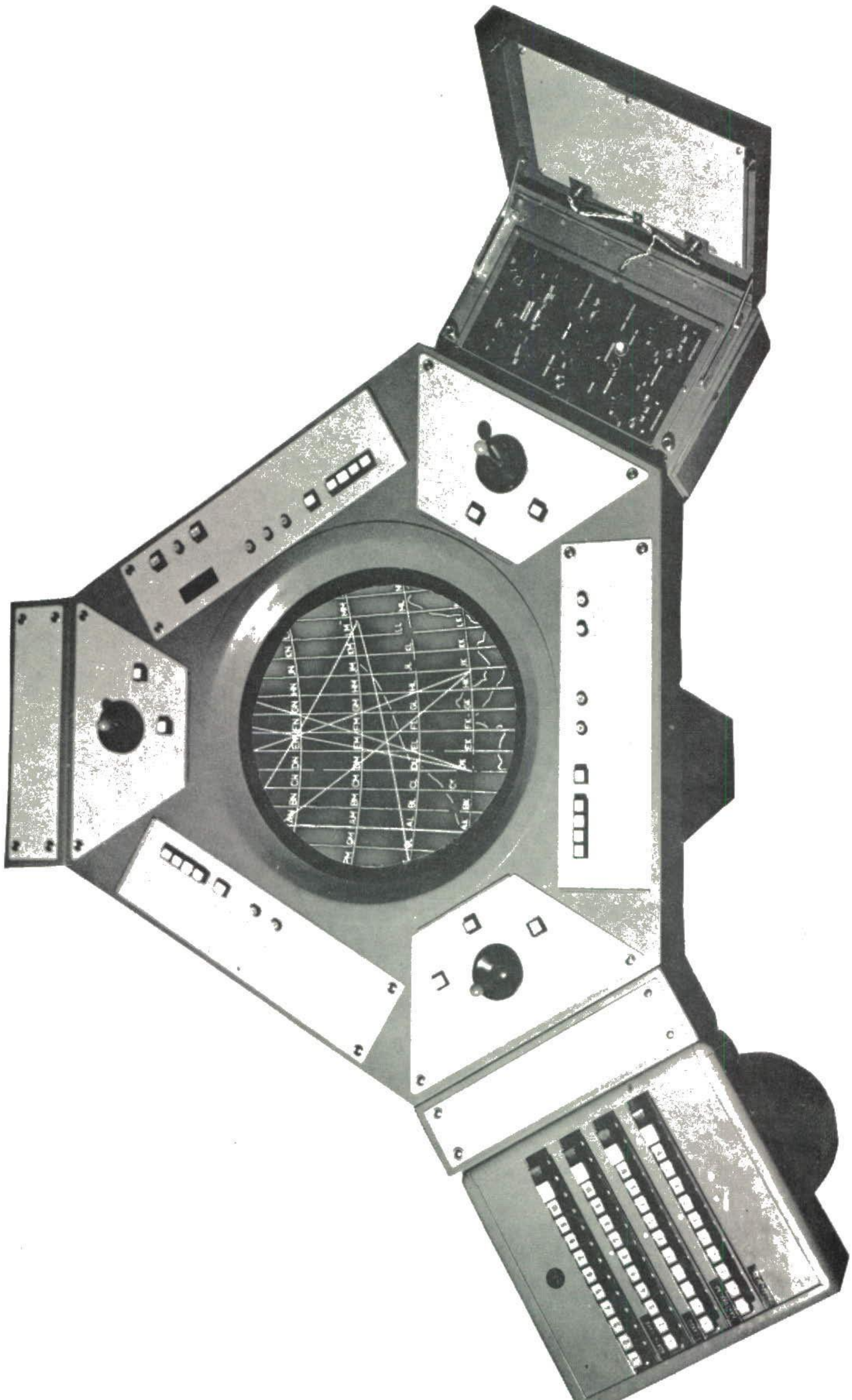


Figure 2.21 Triangulation table

All strobes must be presented on the triangulation table from their appropriate geographical origins. This is accomplished by an origin coordinate selector which is synchronized with the word selection pulses.

The sampling rate, governed by the main distributing equipment, is 22 full cycles per second.

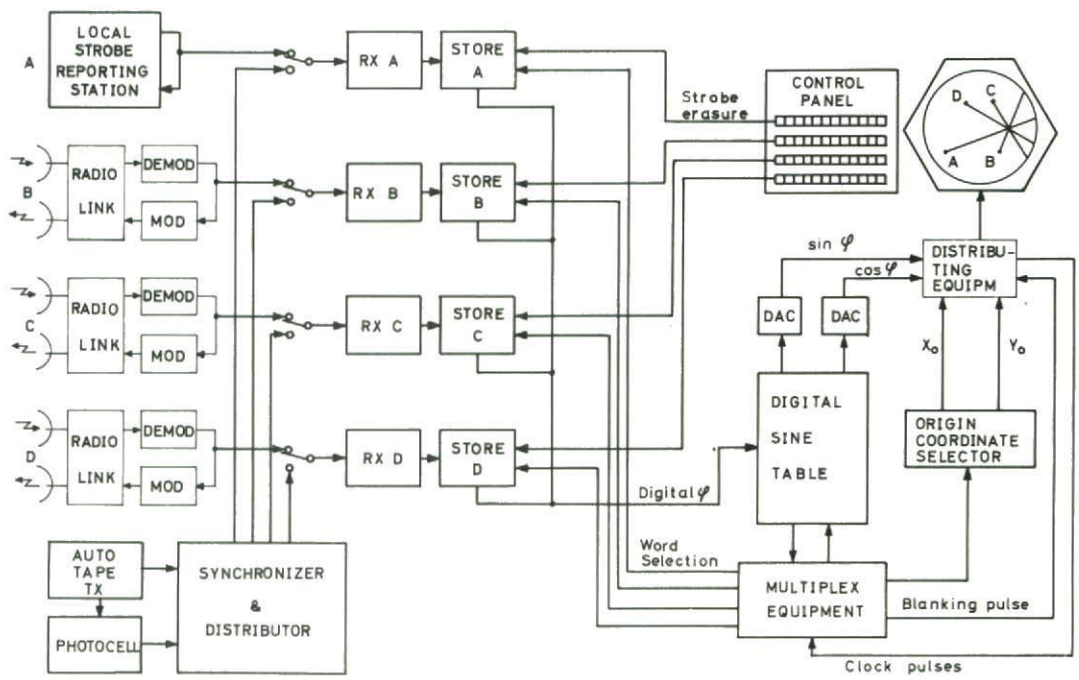


Figure 2.22 Block diagram of triangulation centre

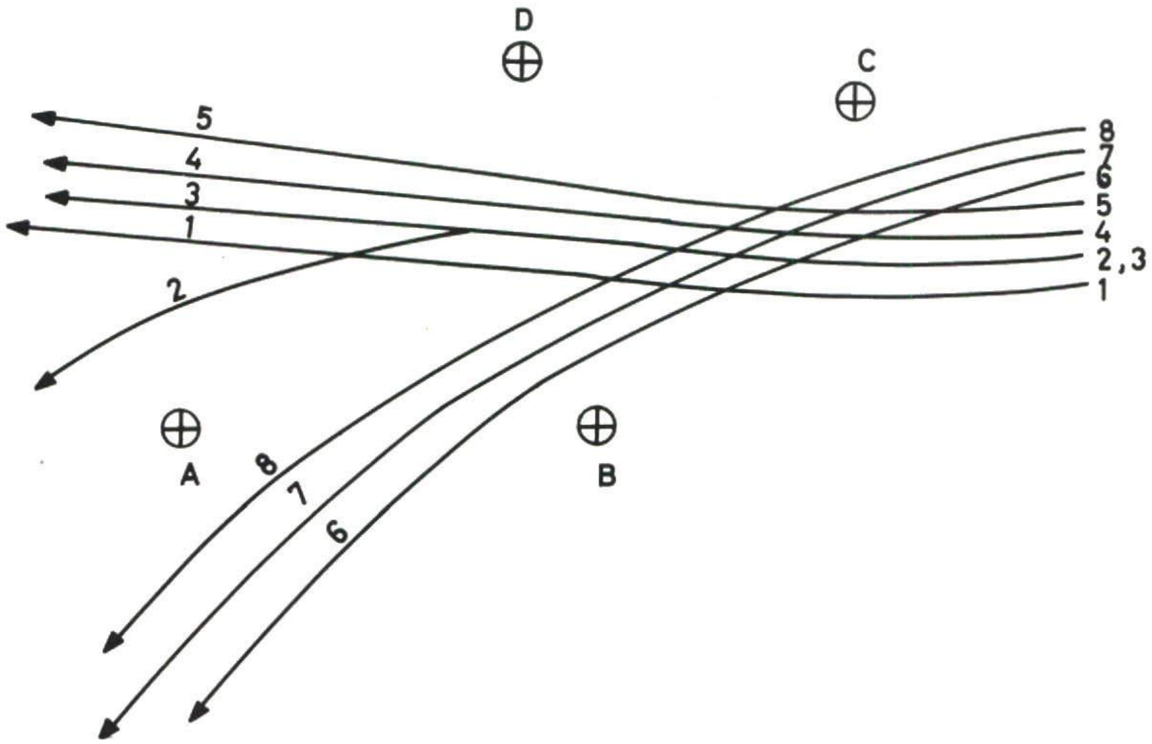
2.3.3 Teleprinter simulation

Because of the code used, simulation can be exercised by means of an automatic tape transmitter reading a suitable tape. An exercise is processed in the following manner:

On a map prepared in radar coordinates, see Figure 2.23, up to eight tracks are drawn, with no restraints on the individual flight paths chosen. The different track speeds are then specified. The assumed system accuracy, including the operator's skill, is stated in terms of root mean square direction finding error. In addition, the ranges of the strobe reporting stations A - D are given, including sectors of reduced range.

The entire information is then fed to the electronic computer of the Norwegian Defence Research Establishment, together with the following set of instructions:

> Start at time $t = 0$. Punch address No 1 of the DAF address code (ref Table 2.3).
>
> Compute the directions from station A to all targets within specified range, adding specified rms errors. Select the smallest resulting angle, add a parity bit and punch the result on tape.
>
> Proceed to B, C and D and repeat the process, always selecting the smallest angle and using address No 1.
>
> Proceed to A, punch address No 2, select the second smallest angle and punch out the result in the same manner as above.
>
> Proceed to B, C and D and repeat the process.



Track	Speed mph	Starting time min	Stopping time min	Additional data
1	750	0	40	
2	500	15	60	
3	750	0	40	
4	750	0	40	
5	750	0	40	
6	600	20	50	
7	600	30	60	
8	600	20	50	

Station	Horizon range miles	Blind sector		
		From	To	Range, miles
A	250	30°	60°	50
B	300	320°	340°	20
C	200			
D	250			

Operator and system inaccuracy: 0.3° rms

Figure 2.23 Map exercise (fictive example)

This process is repeated until all eight tracks have been dealt with. Whenever for any station all tracks within range are processed, erase messages replace the angle information for the tracks out of range.

A complete cycle takes 14.4 seconds (32 messages, each comprising 3 characters of 0.15 seconds duration), which is close to the time taken by one antenna revolution (15 seconds in North Norway).

The entire process is therefore repeated for each 14.4 second interval, until a stop order is issued.

It will be seen that the computer uses the same rules as a strobe reporting operator would apply, not being able to make associations with strobes obtained from other stations.

The entire map exercise is contained on one single tape. When the tape is fed from the automatic tape transmitter (Figure 2.22) a photocell circuit maintains track of the running number of teleprinter characters and through special distributor circuits routes the messages to the proper receivers. The receivers may if desired be switched individually to the tape simulator, with the remaining receivers connected for normal operation. This scheme is useful for combination with other training programs.

2.3.4 Triangulation table and system integration

As a triangulation table, Figure 2.21, is used a long persistence 40 cm early warning plan position indicator, which forms part of the normal radar display system of a semi-automatic control and reporting centre. The required modifications have been carried out by the manufacturer (N V Philips Telecommunicatie Industrie, Hilversum, The Netherlands) on a special contract.

Figure 2.24 shows the principal functions of the triangulation display. Under quiet conditions it is operated as a normal early warning indicator displaying active radar data. When the early warning supervisor presses a button, its role is instantly changed over to become that of a triangulation table.

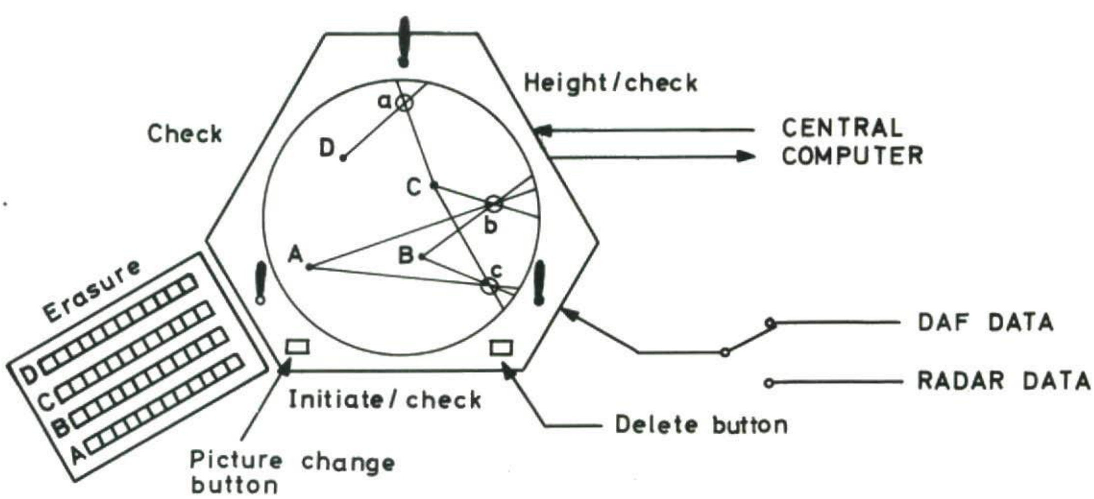


Figure 2.24 Triangulation table, principal controls

The entire triangulated picture is displayed 22 times a second. In the example shown three targets (a - c) are present. Target a is located by stations C and D only, whereas b and c are both located by A, B and C.

In order to permit selective display of strobes, the operator has at his disposal four sets of 12 push-buttons, each set serving strobes from one strobe reporting station. A set of buttons is shown in Figure 2.25. Buttons 1 - 10 control individual strobes, the strobes being usually numbered with increasing North angle. When a button is pressed, the corresponding strobe disappears. When the button is pushed a second time, the strobe reappears.

Button No 11 overrides buttons 1 - 10. If button No 11 is pushed, all strobes appear. If button No 12 is pushed, all strobes disappear. Button 11 and 12 are mechanically interlocked.

Whenever a button is activated, the button is internally illuminated, as a reminder to the operator. Buttons 1 - 10 are amber, 11 is white, and 12 is red.

The central control and reporting station housing the triangulation centre is at present operating in a manual mode, i e track telling is done orally. Telling is done in Georef grid references. For this purpose the operator is provided with a push-button to present an electronic video map on the display, using the afterglow for telling.

Three joysticks are available. They can all be used for marking and/or crosstelling purposes.

One joystick is used for height azication if the supervisor so decides. The operator can therefore employ the height-finder for investigating selected intersections to obtain active radar data if the height-finder frequency is not jammed. By this means the height-finder is in fact used in a surveillance role. In order for an enemy to blind the active radar system, he is therefore required to jam also the height-finder which is typically some 20 - 30 dB more resistant to jamming than is the search radar.

In the semi-automatic mode, which will be available by Fall 1964, display is done by intervention of a central computer and store. In this mode, telling is performed by means of the joysticks which are allocated as shown in Figure 2.24. The main joystick will normally be used for initiating new tracks, but can also be used for updating (checking) old tracks. A second joystick is used for updating, and the third joystick is used for manual height azication (when the supervisor so decides), or updating.

Initiated tracks are fed to the computer for further distribution and display. Once a track has been updated, the computer will provide rate-aiding back to the triangulation display.

Triangulation requires the use of special logical rules to select the correct intersections. The operator will sometimes make mistakes, which can only be detected by himself. He has therefore available a delete button with which he can remove tracks he himself has initiated. (This button is inoperative when the table is switched to the normal radar role).

The integrated system is shown in Figure 2.26. The numbers in brackets indicate the number of identical or near identical consoles.

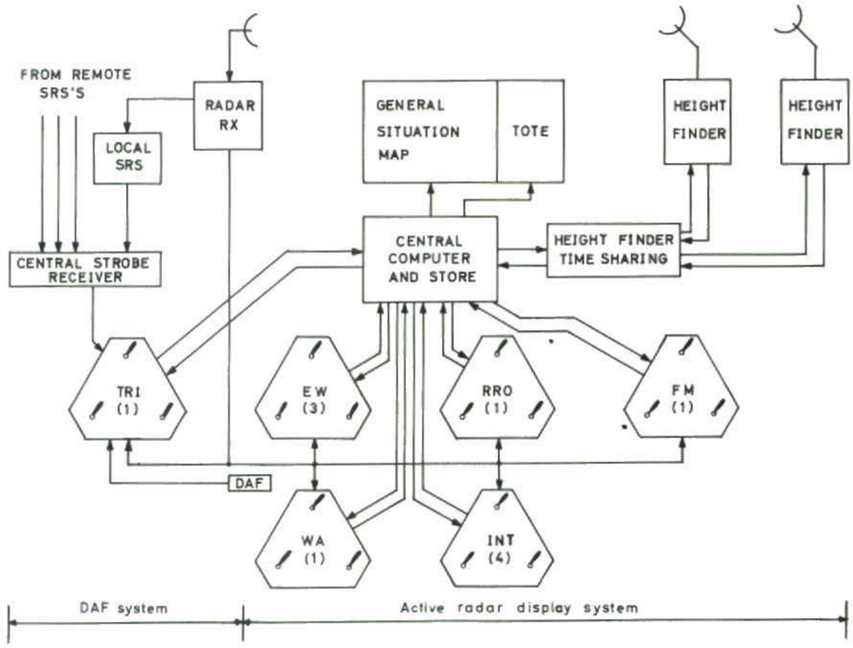
All tracks initiated by the triangulation operator will appear on the general situation map with normal symbols, the only difference being that a special colour symbol is used (flashing white), ref Figure 2.27. The other colour symbols used are:

White	- unidentified tracks
Red	- allocated hostiles
Flashing red	- unallocated hostiles
Bright green	- intercepting fighters
Dark green	- other friendly tracks

All triangulated tracks appear as synthetic markers on all other displays. They can thus be used by the early warning operators in assisting them in looking for

1	2	3	4	5	6	7	8	9	10	LIGHT ALL	ERASE ALL

Figure 2.25 Strobe erasure controls



TRI - Triangulation table
EW - Early warning
RRO - Raid recognition officer
FM - Fighter marshal
WA - Weapon allocator
INT - Intercept control

Figure 2.26 Active/passive integrated system

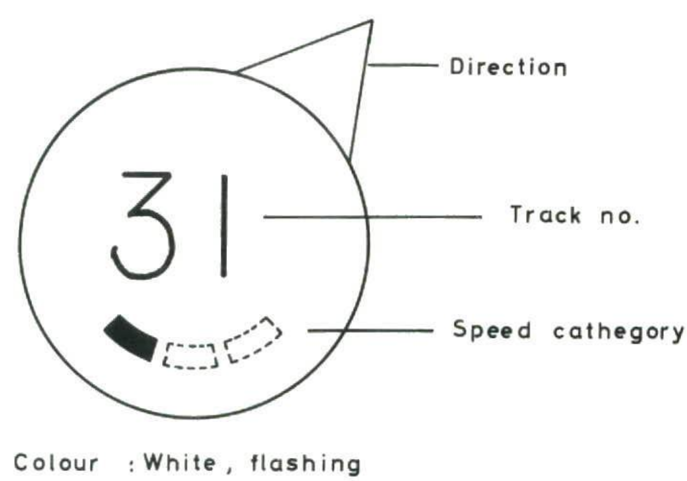


Figure 2.27 General situation map - display symbol

possible active returns, and by the weapon allocator and intercept controllers for possible interceptions.

One height-finder will always be routine controlled by the store. Height information (if available) will appear on the tote table beside the general situation map. The other height finder may, at the supervisor's discretion, be allocated for manual azication.

Manning of the triangulation table can be continuously adjusted according to the circumstances. Under quiet conditions the table is operated as an active radar display. When jamming occurs, the supervisor converts to triangulation operation. If the jamming is light, one operator can manage the situation. If the jamming is serious, little data is obtained from the active radar, and operators can be transferred to assist the triangulation operator.

2.3.5 Test facilities

The central strobe receiving cabinet is equipped with a control panel for checking the main operations of the system.

By means of switches any stored word can be selected and displayed in binary form, thereby checking the performance of the receivers and stores. When a button is pressed, the word, reduced by one increment, is transferred to the store input register and displayed. Other indicators show the digital sine (or cosine) of the word previously displayed. Whenever the button is pressed, the angle is reduced by one increment. By stepping the angle it is thus possible to check every combination of the digital sine table.

If a switch is turned, special angle test patterns are fed to the digital sine table for display on the triangulation table.

A central voltmeter can select all crucial DC voltages.

When a fault occurs, the approximate position of the fault is found by means of the control panel. The defective card is next identified by measurements on the card test points which are directly accessible.

2.4 Main characteristics

2.4.1 Strobe reporting station SRS-1 (including IFF simulator)

Input frequency	: Radar IF frequency (13.5 or 30 Mc/s)
Equivalent input saturating power	: 0 - 120 dB in 10 dB steps
Input attenuator range	: 100 W/Mc/s jammer at 15 nm range
Receiver dynamic range	: 45 dB (logarithmic)
Receiver IF bandwidth	: 500 kc/s
Receiver video time constant	: 10 ms
Max number of individual strobes	: 10
Angle quantization step	: 0.703°
Duration of one strobe transmission	: 0.45 s
Data link	: 50 baud teleprinter channel (simplex or duplex)
Permissible data link element error	: $5 \cdot 10^{-3}$ (for duplex operation)
Number of printed circuit cards	: 99
Power	: 220 V AC ± 10%, 200 W

Ambient temperature range	: -27° C to +55° C
Overall width	: 67 cm (26.5")
Overall depth	: 105 cm (41.5")
Overall height	: 190 cm (75")

2.4.2 Central strobe receiver CSR-1 (including tape simulator cards)

Number of strobe receivers	: 4
Display rate	: 880 strobes per second
Coordinate accuracy	: ± 0.25 nm
Number of printed circuit cards	: 214
Power	: 220 V AC ± 10%, 400 W
Ambient temperature range	: -27° C to +55° C
Overall width	: 90 cm (35.5")
Overall depth	: 50 cm (20")
Overall height	: 215 cm (7')

2.4.3 Triangulation table

N V Philips Telecommunicatie Industrie, Netherlands, horizontal early warning plan position indicator display unit, type 8GM214/02 (Modified).

Screen diameter	: 40 cm (16")
Afterglow	: ≈30 s
Calibrated range scales	: 0 - 80 nm 0 - 160 nm 0 - 240 nm 0 - 320 nm
Off-centering	: 0 - 240 nm, any direction
Max range for triangulation	: 560 nm
Range markers	: Coarse - 40 nm Fine - 10 nm
Angle markers	: Coarse - 30° : Fine - 10°
Video map	: Coarse and fine
Overall width	: 120 cm (47.5")
Overall depth	: 85 cm (33.5")
Overall height	: 80 cm (31.5")

2.4.4 Strobe erasure panel

Number of individual strobe controls	: 4 x 10
Number of station blanking controls	: 4
Number of station unblanking controls	: 4
Overall width	: 36 cm (14")
Overall depth	: 30 cm (12")
Overall height	: 80 cm (31.5")

3 EVALUATION

3.1 Introduction

Evaluation of a passive detection system close to the NATO border to the east imposes several problems since, for security reasons, airborne jamming against several radar stations in the area has not so far been permitted. Recourse has therefore been taken to more indirect means for assessment of the DAF system performance.

For the DAF system coverage against targets at various altitudes, all key data are available from measurements made in connection with the active radar system. Without real targets and means to determine their exact positions, however, the system positional accuracy cannot be directly measured. Instead, the error sources which contribute towards the overall inaccuracy have been studied individually, and the resulting positional errors have next been determined by computation. Some of the basic inaccuracies had to be estimated rather than measured.

To determine the capability of the triangulation table and its operators in detecting and following discrete targets under various raid conditions, numerous tape simulated map exercises have been carried out. For these exercises near-realistic synthetic data and updating speeds have been used.

Airborne exercises have also been used to a limited extent. A spot frequency jammer has on several occasions been flown in the DAF area, being tracked by jamming strobes from one station and IFF simulated strobes from the other stations. In addition, fighters have frequently been triangulated by means of IFF strobes, and a few interception exercises have been successfully carried out.

The evaluation program was started in late Autumn 1963, but was discontinued when a main power failure rendered the main radar site inoperative. During Winter 1963/64 one of the key strobe reporting stations was inaccessible due to heavy snow which blocked the main road. New tests were started in April 1964, and were carried out under great difficulties as the road between the main site and the housing area some 8 miles away had to be closed during the thawing of ice in the ground.

For the above reasons the evaluation program has not been as extensive as might be desired, and the emphasis had to be put on the key parameters of the DAF system, leaving out details which, however important, had to be given a lower priority.

3.2 Sites installed

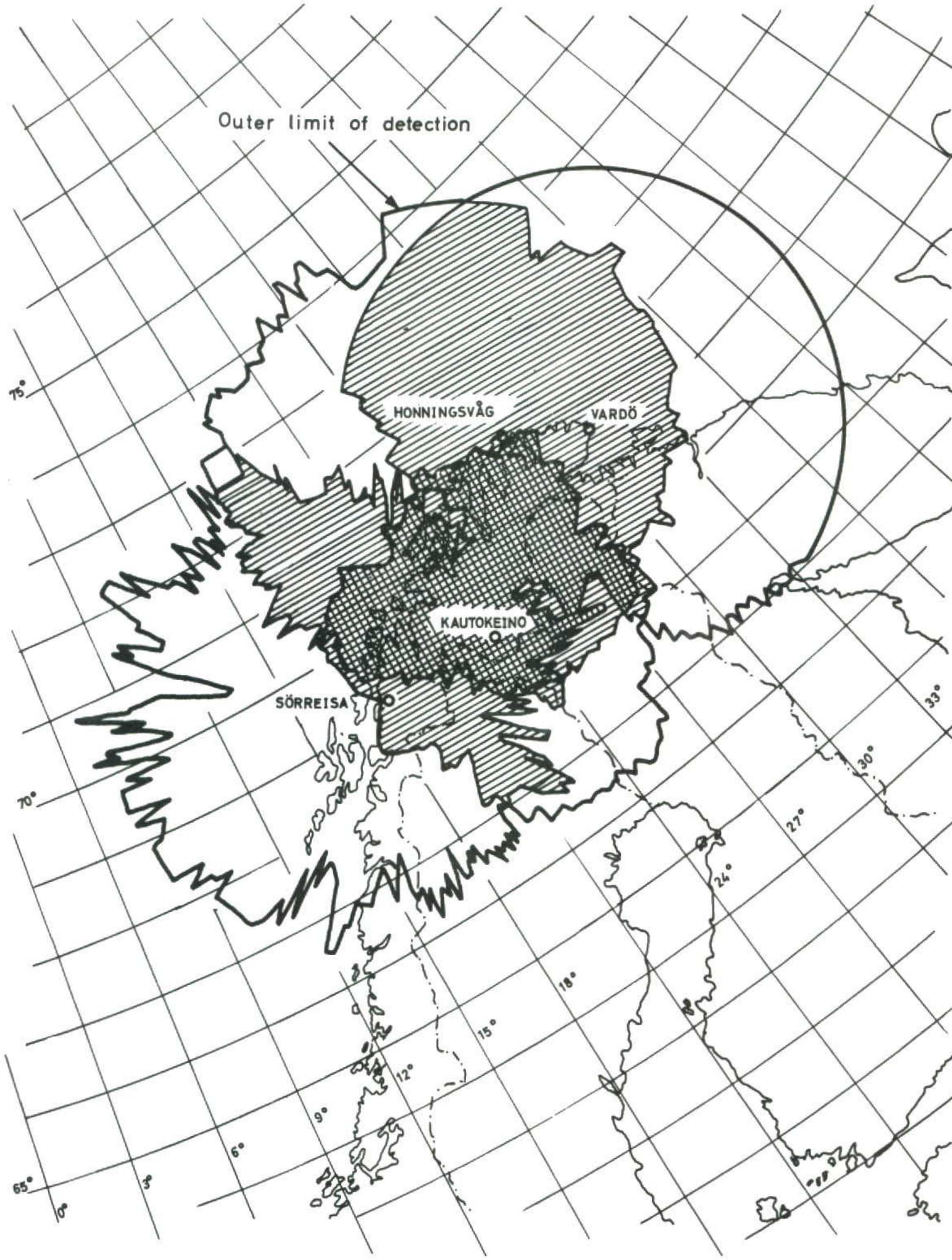
The DAF system was installed at the sites listed in Table 3.1. At each site the SRS installation and cabling were completed and the equipment made operational in less than two days. The CSR and triangulation table installation required two days.

The Sørreisa CRC operations room is located inside a mountain 25 miles west of Bardufoss airport. A one mile funicular railroad inside the mountain connects the operations room with the radar head.

Kautokeino RP is located in wooden buildings adjacent to the Lapp village of Kautokeino on the Finnmark plains, 80 miles south of Alta airport. During Winter the road between Alta and Kautokeino is usually closed, the only access being by snowmobile or reindeer sledge.

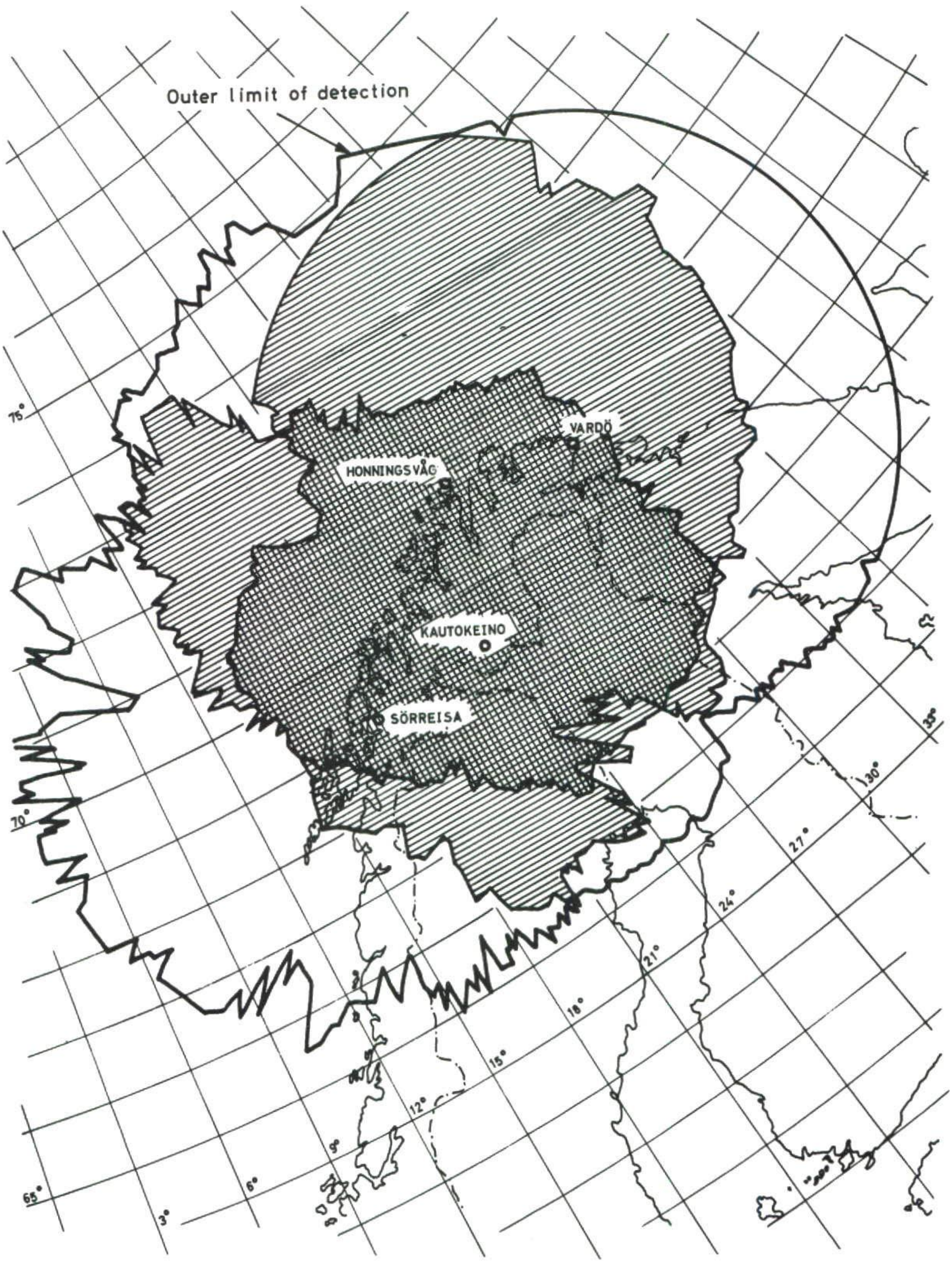
Vardø RP is located in the town of Vardø on an island in the East Sea. The harbour is served by a coastal steamer.

Honningsvåg RP is located on a mountain near North Cape. Access from the fishing village of Honningsvåg to the radar site is by means of an overhead cable driven carriage. The harbour of Honningsvåg is regularly served by a coastal steamer.



Covered by two stations
Covered by three or four stations

Figure 3.2 DAF coverage, altitude 20 000 ft



Covered by two stations
Covered by three or four stations

Figure 3.3 DAF coverage, altitude 40 000 ft

3.4 Area of coverage

In order for a target to be located by any passive detection system, it must be within range of at least two stations. The areas so defined for the DAF network are shown in Figures 3.2 - 3.3, for 20 000 ft and 40 000 ft altitude respectively. The diagrams are based upon measurements of the radar horizon under normal atmospheric conditions. The necessary data have been provided by the Royal Norwegian Air Force.

It has been assumed that a potential aggressor may know the location of the radar sites, and therefore also possibly possesses a fair knowledge of their horizon ranges. The active radar ranges against targets at various aspect angles are probably not known in sufficient detail. It is therefore expected that he will start jamming close to the horizon of the first radar station approached. A weak barrage jammer will at that range be detectable from the radar station concerned, whereas a strong jammer may also be detected by other radar stations even if it is below their horizons. The cover diagrams in Figures 3.2 - 3.3 conservatively assume that weak jammers will be employed.

3.5 Triangulation inaccuracy due to angular errors

An inaccuracy in location occurs as a result of inaccurate direction finding as indicated in Figure 3.4. A target at position P is direction found by stations A and B. Due to angular errors $\Delta\varphi_A$ and $\Delta\varphi_B$ the apparent position is at point P', and a miss distance r results.

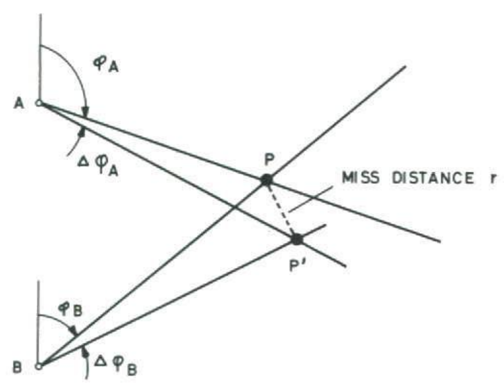


Figure 3.4 Position error due to angular error

Each angular error is made up from the following contributions, which will be discussed separately:

a) Error due to finite antenna beamwidth

b) Operator inaccuracy

c) Analog-to-digital angle quantizing error

d) Triangulation display quantizing error

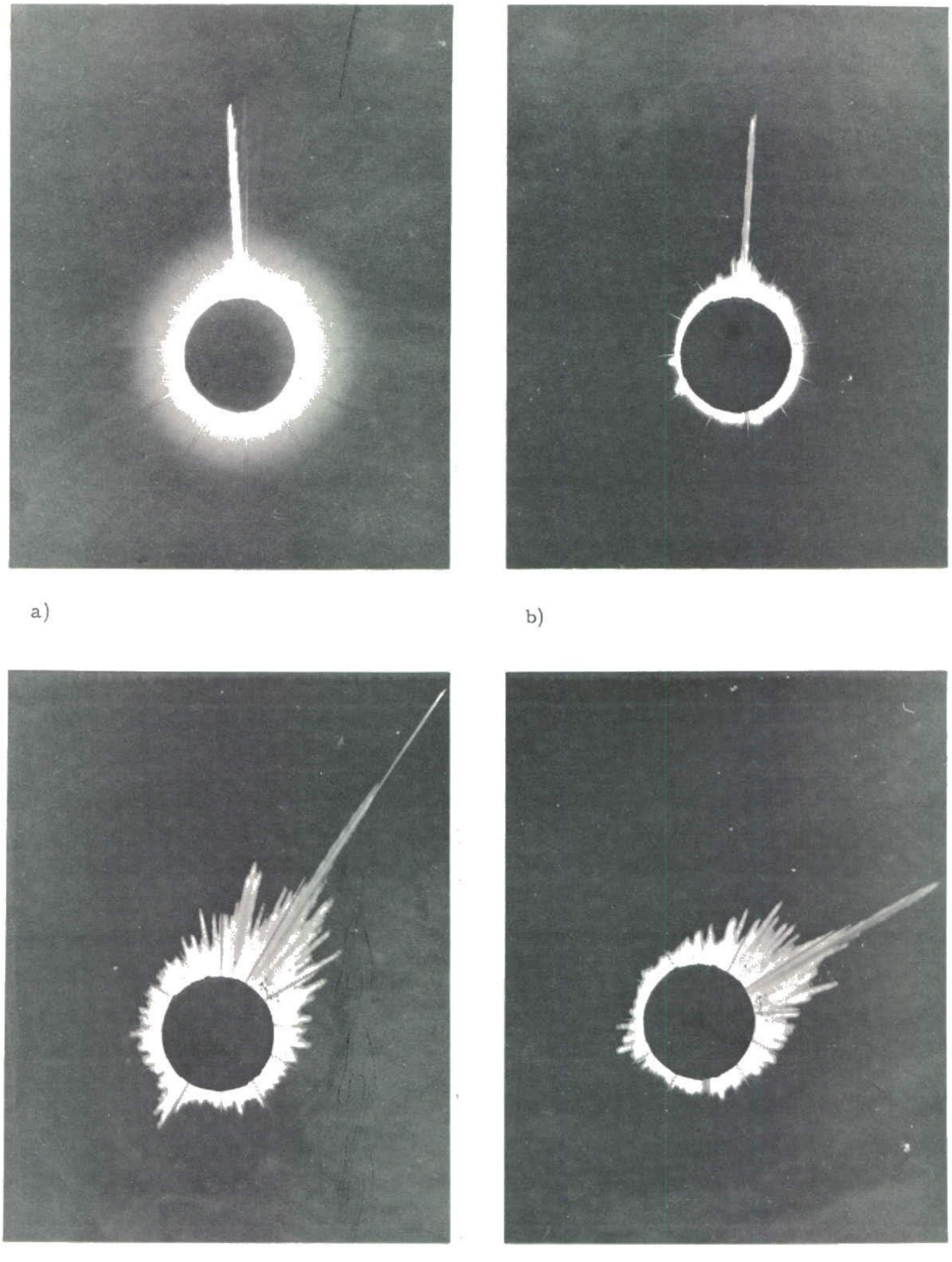
3.5.1 Error due to finite antenna beamwidth

Figure 3.5 shows four examples of an amplitude versus azimuth (AVA) display in the case of an airborne jammer circling around the station.

From the AVA display the operator decides by inspection of the peak the direction to the jammer. His inaccuracy in this assessment is determined by the antenna beamwidth and the display sampling rate. The latter rate is 50 c/s, giving a quantizing step of 0.48^o for four antenna revolutions per minute, or a root mean square error of 0.14^o which is negligible. The error due to the finite beamwidth may for narrow beam antennas reasonably be estimated to have a root mean square value $\sigma_1 = b/4$, where b equals the beamwidth between half power points. This assumption permits 5% of the observations to fall outside the half power points.

3.5.2 Operator error

Having first visually located the peak on the AVA display, the operator aligns his cursor with the selected direction. His accuracy in doing so depends on his skill



a) b)

c) d)

Note: In c, a cursor strobe is present

Figure 3.5 AVA displays of airborne jammers and the cursor definition. The error is small and an accurate measurement of the error is not possible. As an example, in Figure 3.5c where the discrepancy between the cursor strobe and the polar diagram peak is less than 0.5° the error is clearly visible. From close observation of several operators, it appears that errors outside $\pm 0.5^{\circ}$ rarely occur. Permitting 5% of the errors to fall outside $\pm 0.5^{\circ}$, and assuming a normal distribution function, the operator root mean square error is put equal to $\sigma_2 = 0.25^{\circ}$.

3.5.3 Analog-to-digital quantizing error

In the transmitted message the angle is quantized in increments of $360^{\circ}/512 = 0.703^{\circ}$. This introduces a quantizing root mean square error $\sigma_3 = 0.203^{\circ}$.

3.5.4 Triangulation centre quantizing error

At the triangulation centre each quantized angle is fed to the digital sine table, where the sine and cosine of the first quadrant angle are quantized in increments of $1/256 = 0.0039$. The resulting root mean square error in terms of angular displacement on the display equals $\sigma_4 = 0.065^{\circ}$.

3.5.5 Combined angle error

The angular error contributions are gathered in Table 3.2. Assuming the various errors to be independent, and the resultant error distribution to follow a normal distribution law, the total root mean square error as found by quadratic addition of the individual contributions is:

For AN/FPS-8 : 0.705° For S-266 : 0.427°

The corresponding error functions are shown in Figure 3.6.

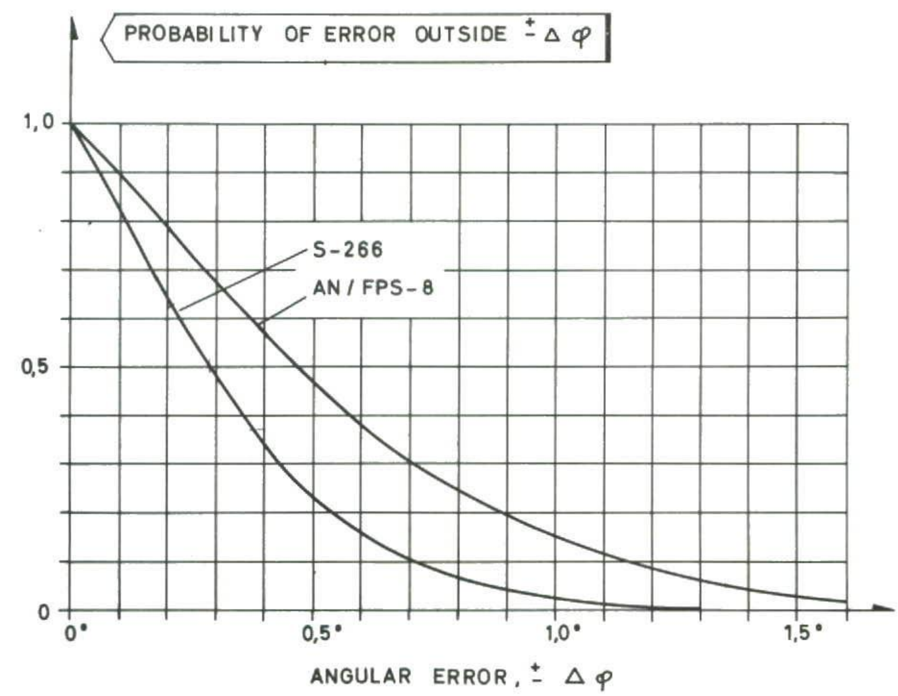


Figure 3.6 The error function $W = \frac{2}{\sqrt{2\pi}\,\sigma} \int_{\Delta\varphi}^{\infty} e^{-\frac{x^2}{2\sigma^2}} dx$

with $\sigma = 0.43^{\circ}$ (S-266) and $\sigma = 0.70^{\circ}$ (AN/FPS-8)

Error source	Symbol	AN/FPS-8	S-266
Antenna beamwidth	σ_1	0.625°	0.275°
Operator	σ_2	0.250°	0.250°
Analog-to-digital conversion	σ_3	0.203°	0.203°
Sine/cosine conversion	σ_4	0.065°	0.065°
Total rms error	σ	0.705°	0.427°

Table 3.2 Root mean square angular errors

3.5.6 Radius of uncertainty

A computation program has been carried out to determine the radius of uncertainty (miss distance) resulting from the angular errors. For details of the program, reference (1) should be consulted.

In Figure 3.7, which applies to triangulation by Sørreisa and Kautokeino or Vardø and Honningsvåg, are shown loci for a target which with a probability W = 50% for a single fix will be decided to lie inside a circle of radius R, centered about the true target position. The assumed error angle equals the geometric mean of the individual errors of the two stations.

Corresponding curves for other station combinations are given in Figures 3.8 - 3.10.

Figure 3.11 illustrates for one station combination the effect of varying the probability W that the target is decided to fall inside a circle of specified radius (in the example R = 6 nm)

3.6 Inaccuracy due to aircraft movement

Consider a jammer moving along the course P_1 - P_4 as shown in Figure 3.12. A strobe reporting station can sample its direction only once per antenna revolution, which in North Norway represents a sampling interval of 15 seconds.

The antennas rotate asynchronously, and two stations may therefore directionfind the target at different times. In Figure 3.12a, the jammer may thus be direction-found by A first time when it is in position P_2 (strobe A') and next time when it is at P_4 (strobe A''), during which interval the aircraft has moved a distance vT, where v is aircraft speed and T is the sampling interval. The same target may be direction-found by B when in positions P_1 (strobe B') and P_3 (strobe B'').

On the triangulation display, strobes A' and B' combine to give the apparent position Q_1 during the interval when the aircraft moves from P_2 to P_3. As the aircraft moves from P_3 to P_4, strobes A' and B'' give the apparent position Q_2, and so forth. The aircraft thus apparently moves in discrete steps along a zig-zag path Q_1-Q_2-Q_3- etc. A typical plot is shown in Figure 3.12b.

The excursions perpendicular to the flight path have a time average equal to zero. The mean error in the direction of the flight path is $\frac{1}{2}$vT, which for a Mach 1 aircraft corresponds to 1.25 nm. The quoted figures apply irrespective of the flight path location relative to the strobe reporting stations.

The root mean square of the total error is a function of path direction and location. In the diagrams presented in Figures 3.13 - 3.16 have been assumed a random aircraft course and a random phase relationship between the various antenna rotations. No smoothing or operator prediction has been taken into account, and the curves therefore represent a worst case. For details, the appropriate reference should be consulted (2).

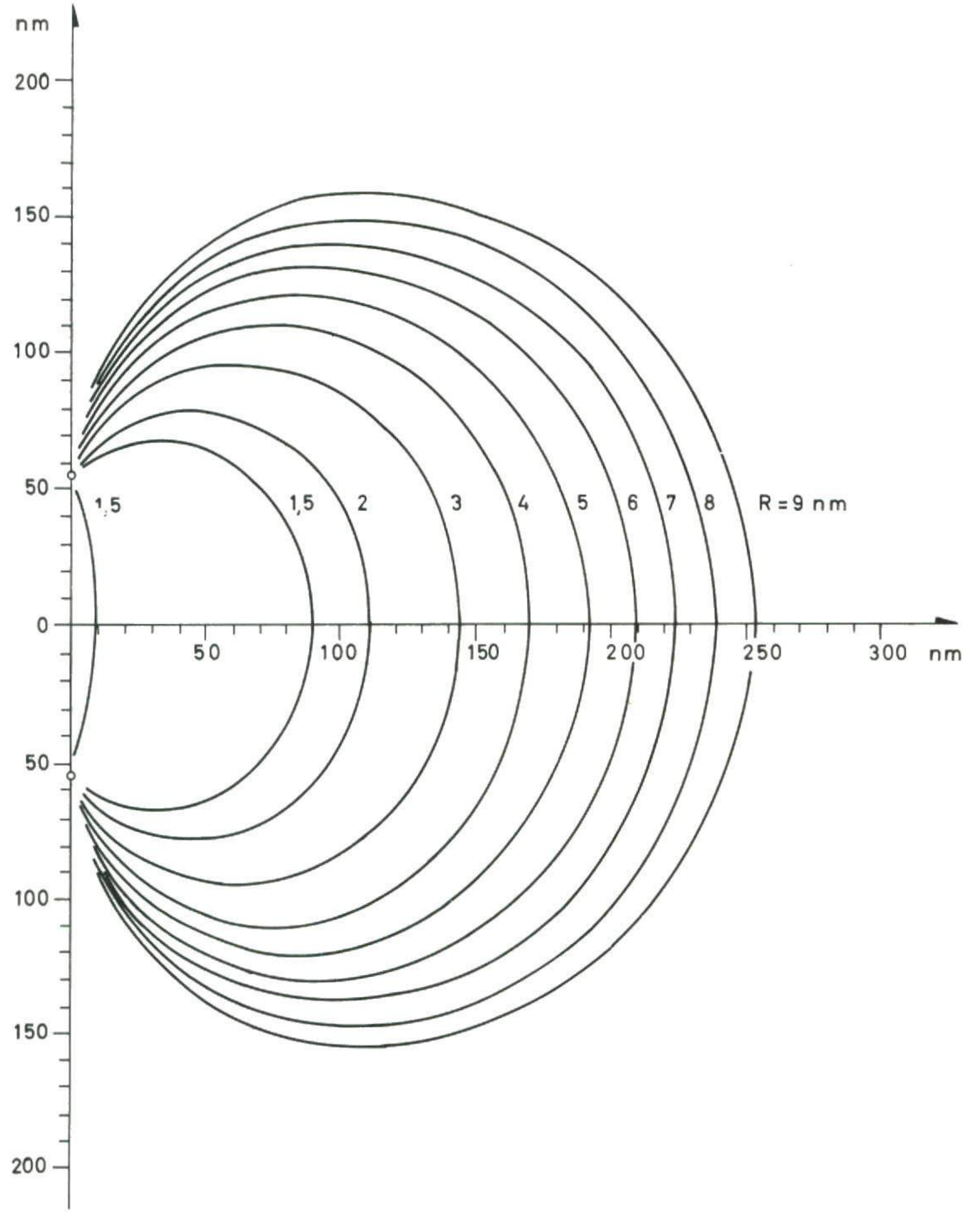


Figure 3.7 Position error due to angular error

W = 50%, Baseline = 108 nm, $\sigma = 0.60^{\circ}$
Stations: Sørreisa and Kautokeino, or
Vardø and Honningsvåg

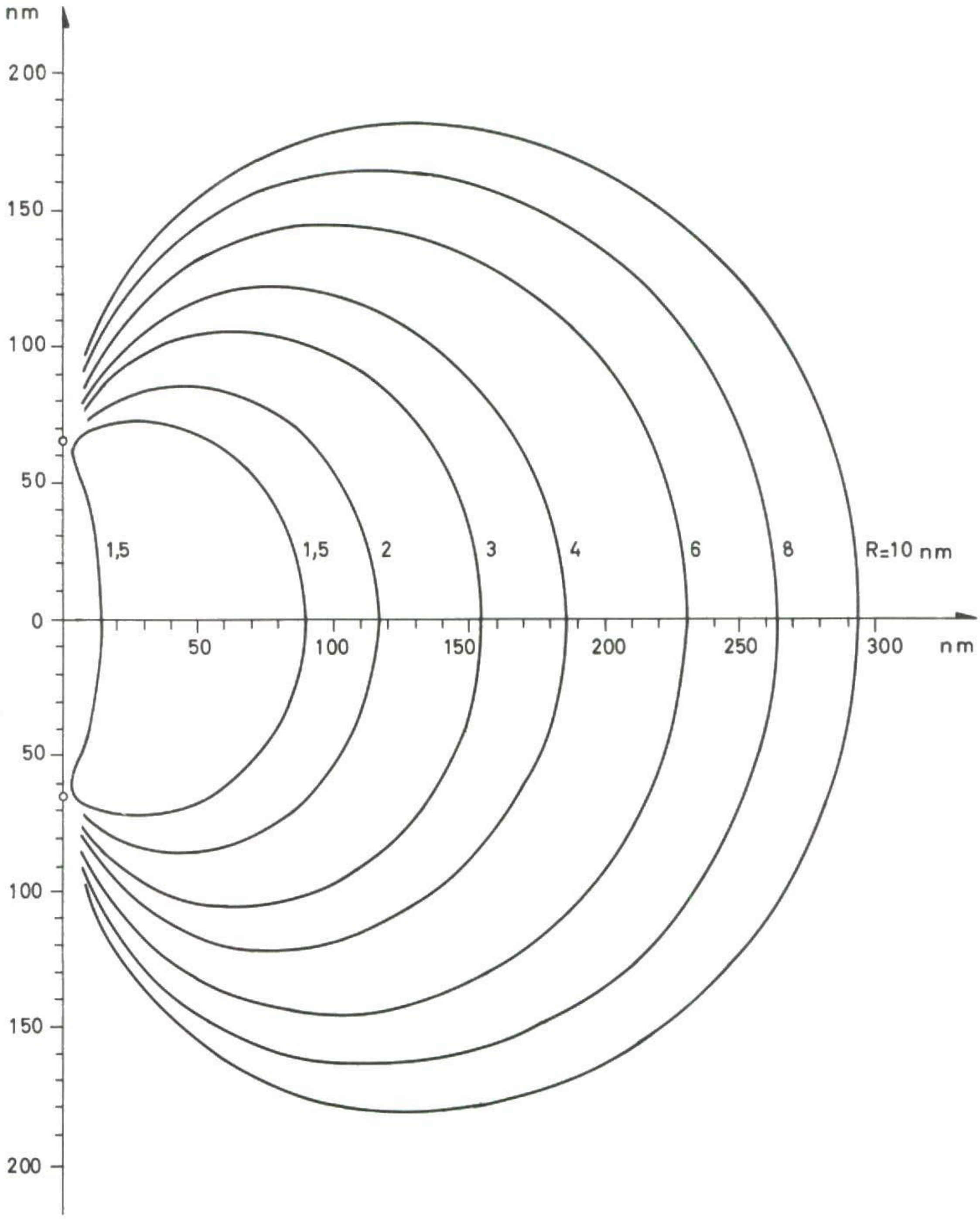


Figure 3.8 Position error due to angular error
W = 50%, Baseline = 131 nm, $\sigma = 0.60^{\circ}$
Stations: Kautokeino and Honningsvåg

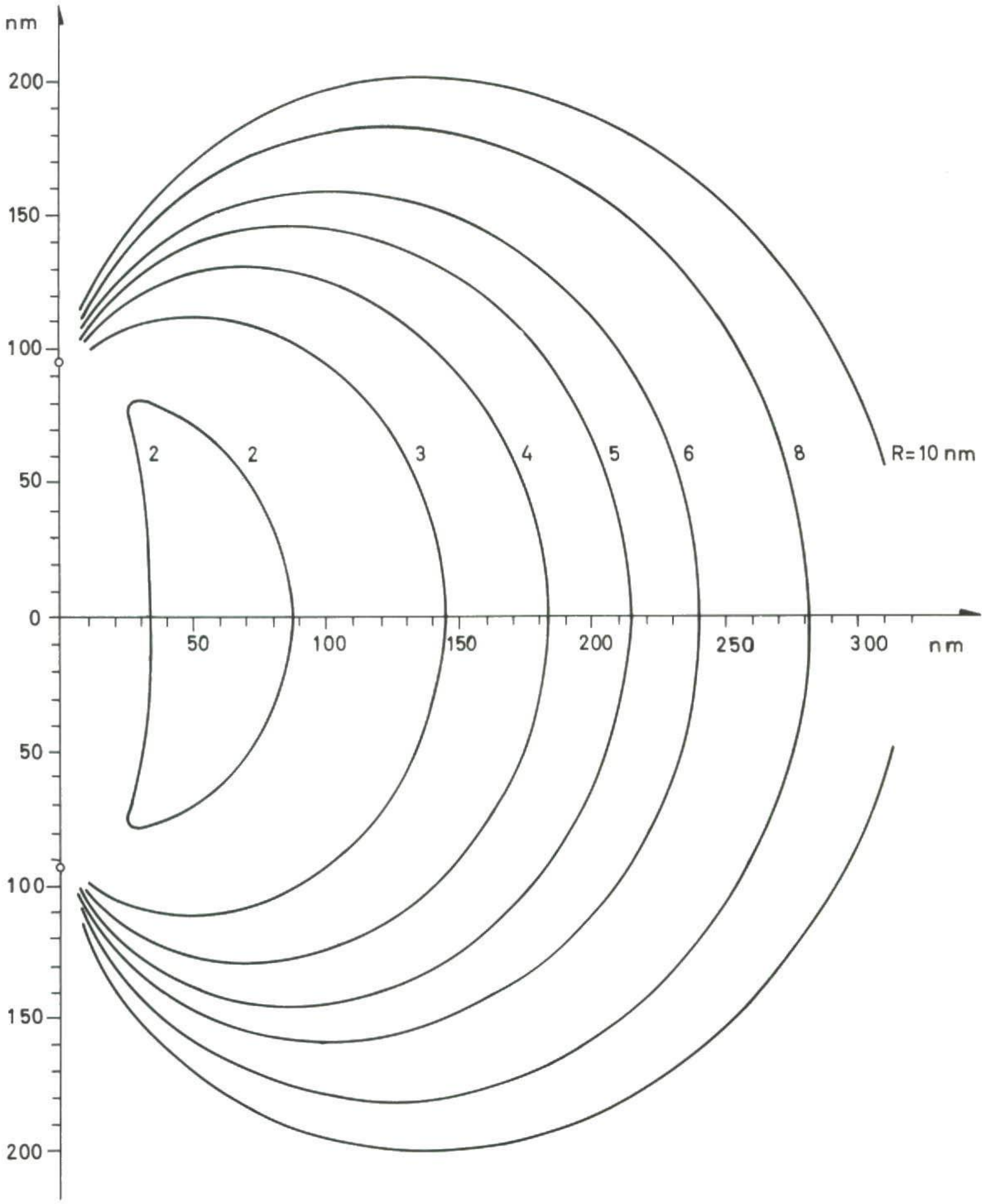


Figure 3.9 Position error due to angular error
W = 50%, Baseline = 187 nm, $\sigma = 0.75^{o}$
Stations: Kautokeino and Vardø

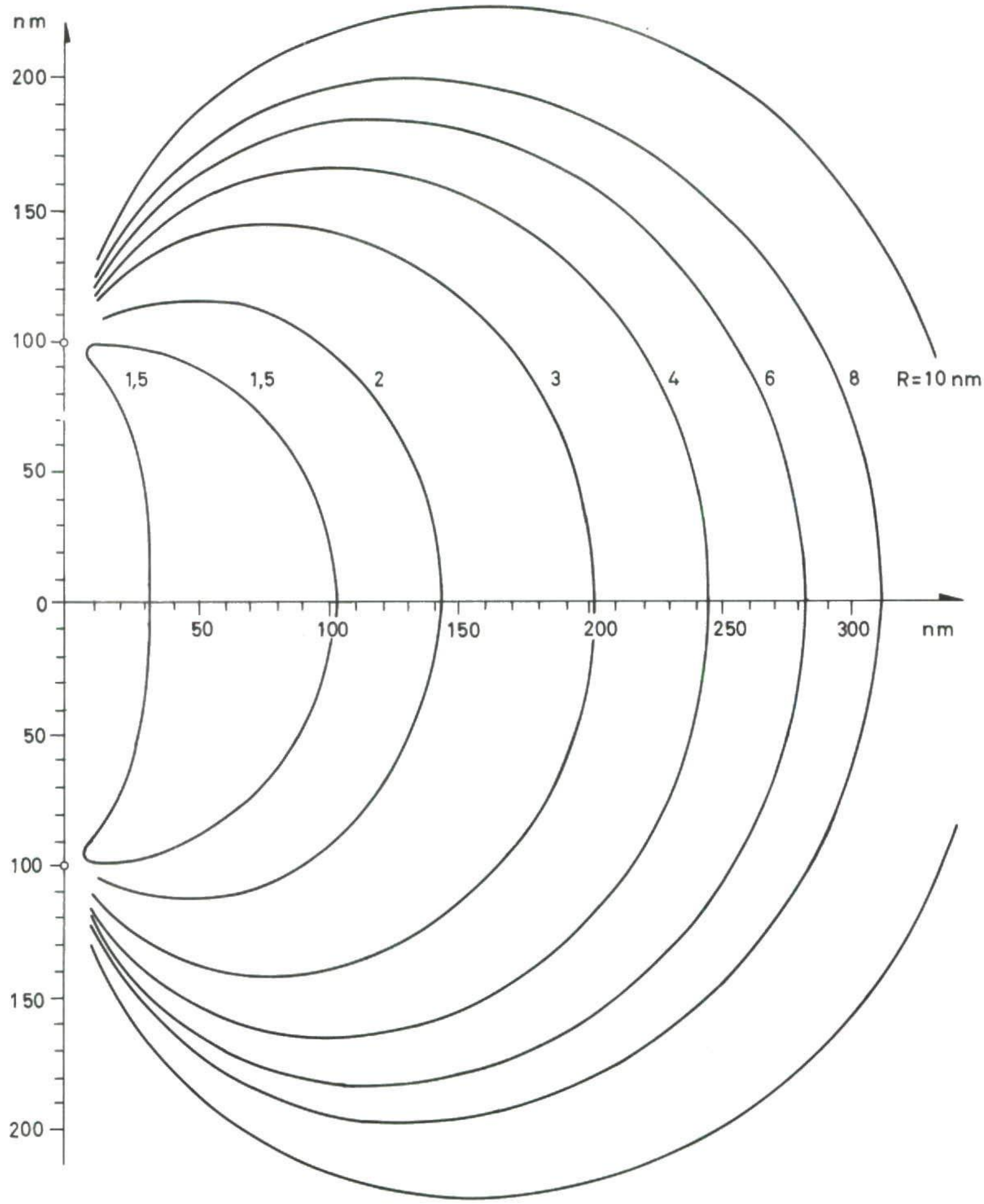


Figure 3.10 Position error due to angular error
W = 50%, Baseline = 199 nm, $\sigma = 0.50°$
Stations: Sørreisa and Honningsvåg

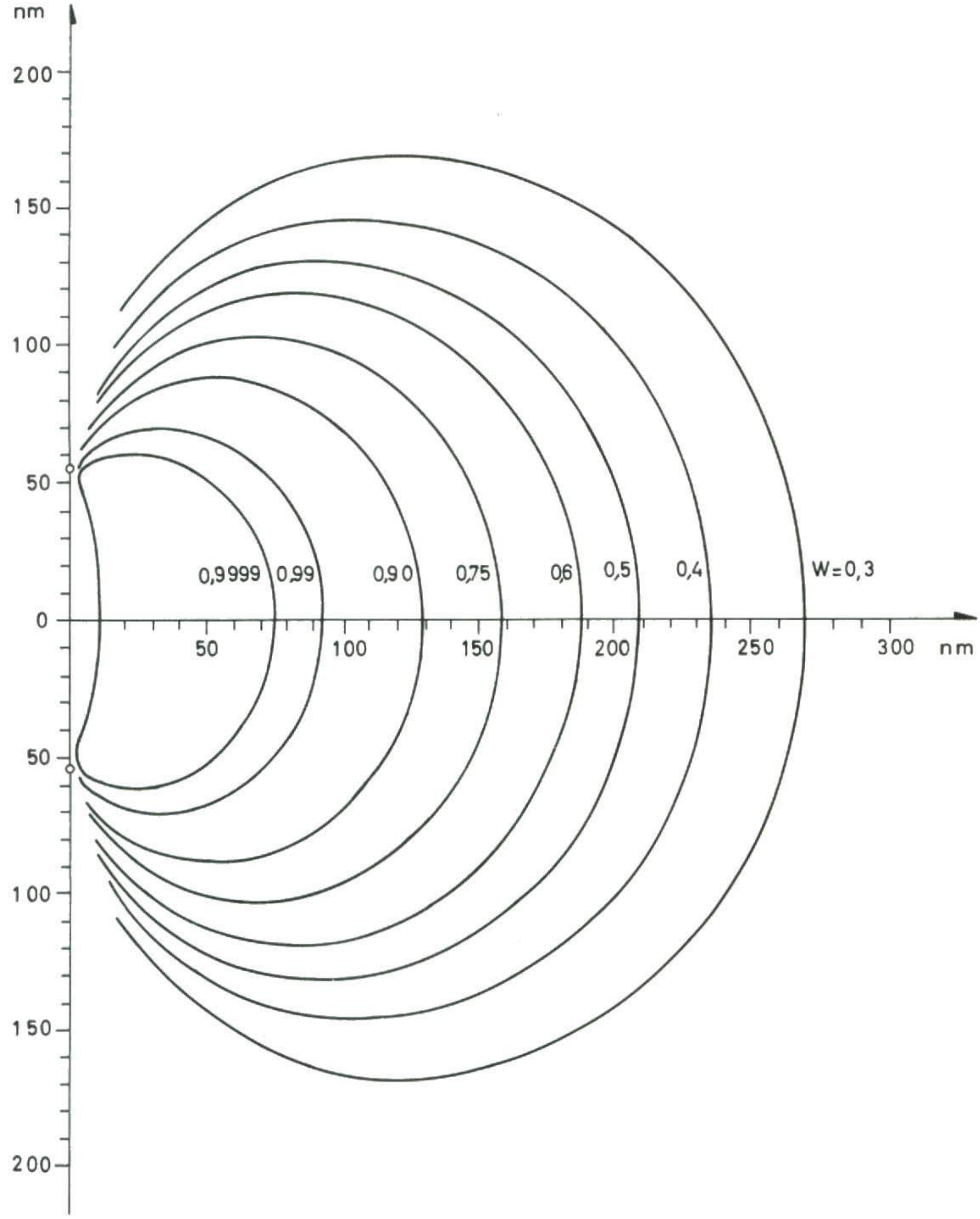
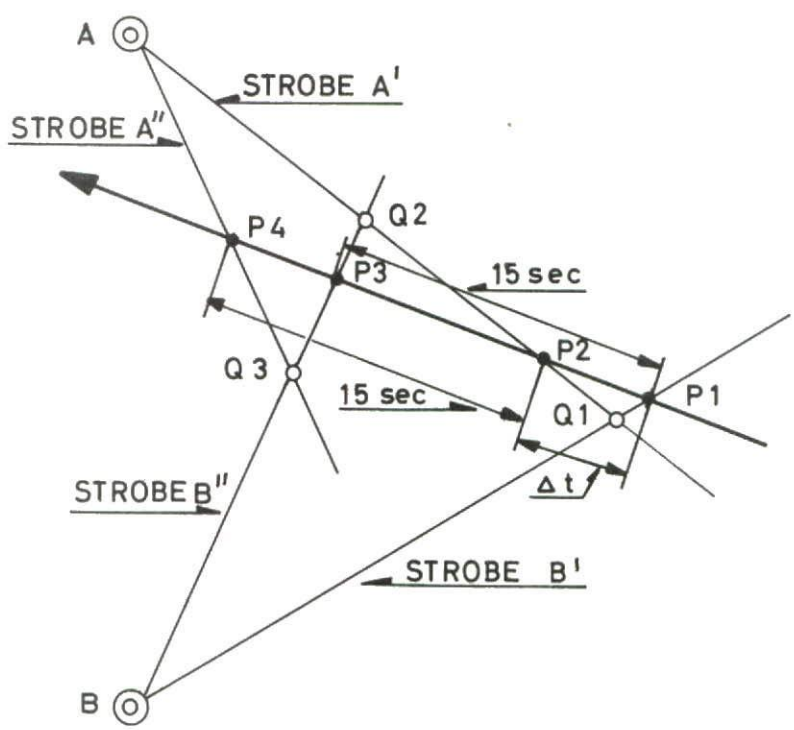
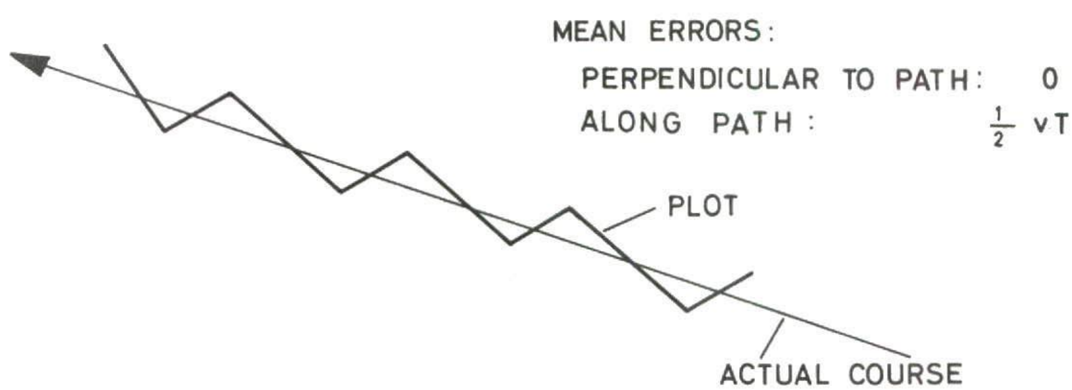


Figure 3.11 Probability W of target being inside a circle of radius R = 6 nm

Baseline = 108 nm, $\sigma = 0.60^{o}$
Stations: Sørreisa and Kautokeino, or
Vardø and Honningsvåg



a. DETAILS OF PLOT



b. TYPICAL PLOT

Figure 3.12 Effect of aircraft movement

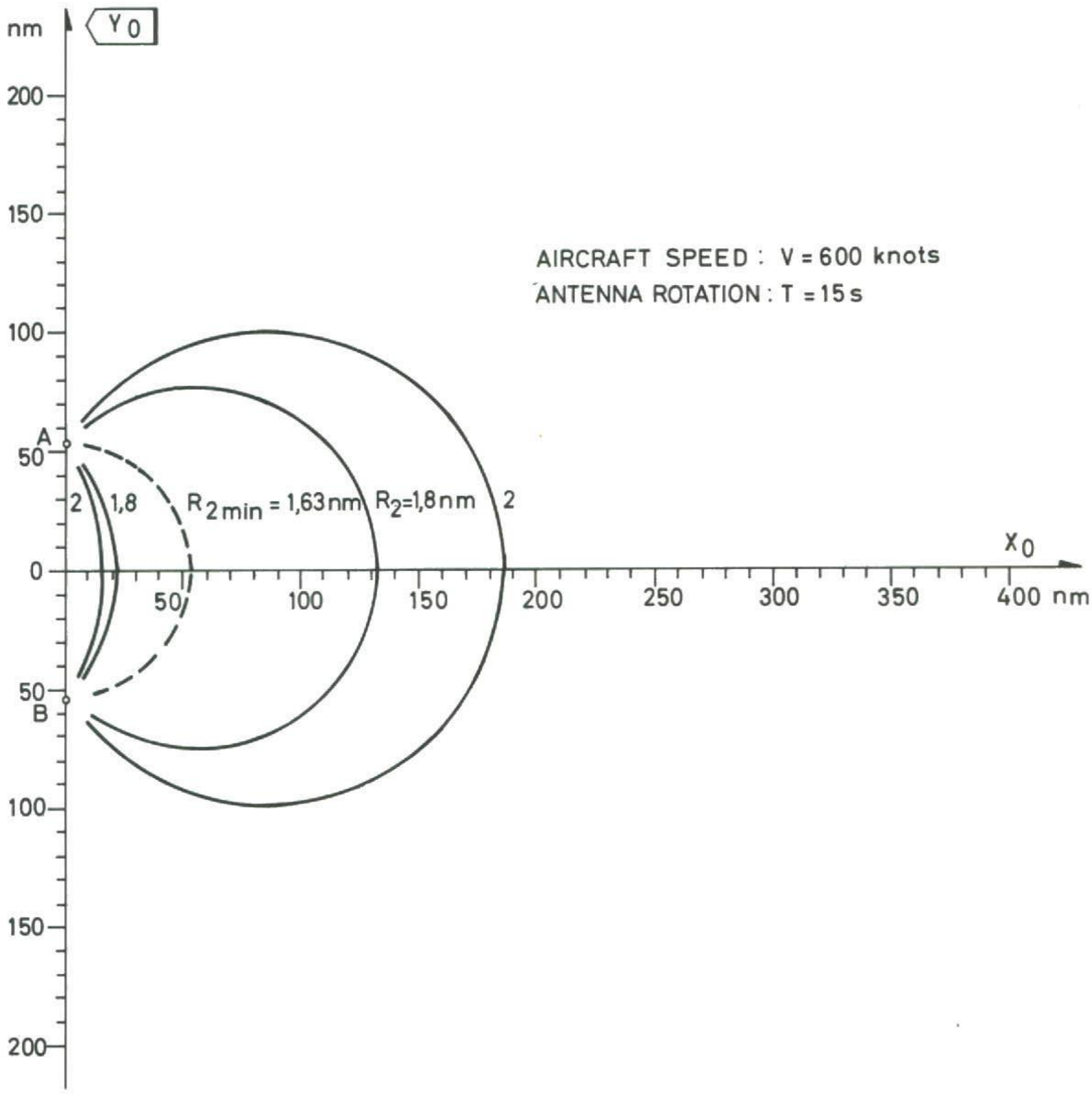


Figure 3.13 Root mean square position error due to aircraft movement
Stations: Sørreisa and Kautokeino, or
Vardø and Honningsvåg

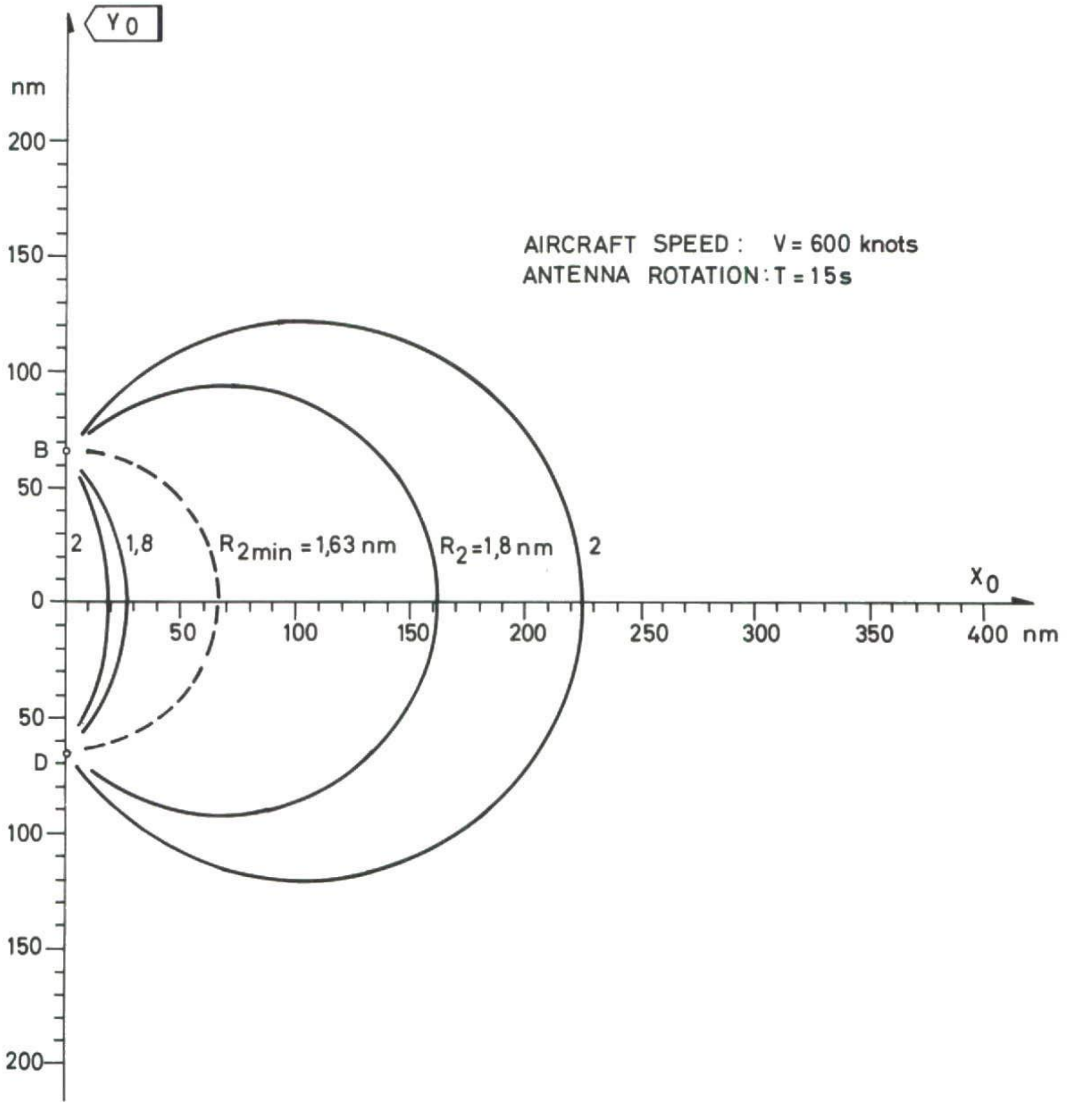


Figure 3.14 Root mean square position error due to aircraft movement
Stations: Kautokeino and Honningsvåg

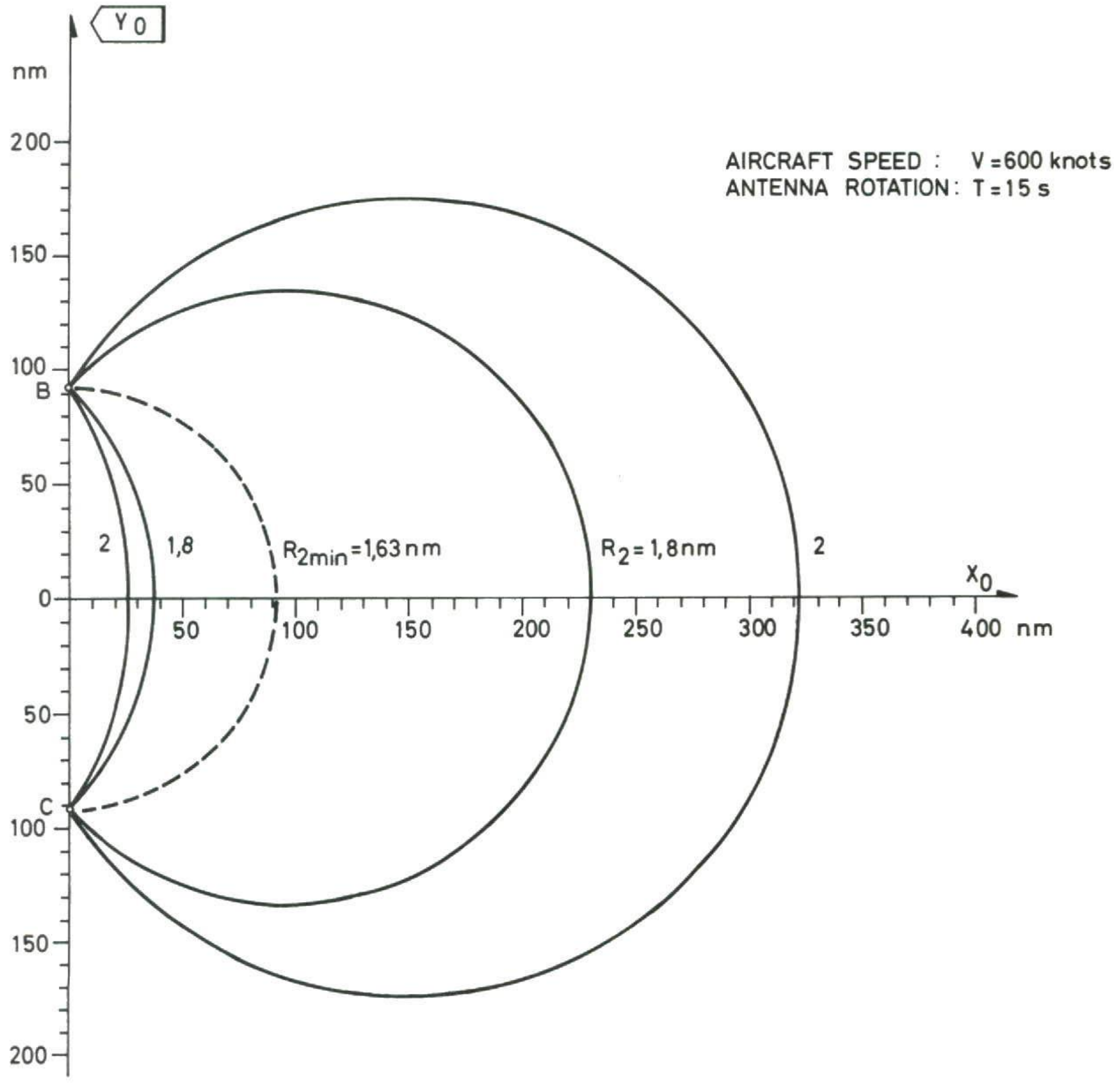


Figure 3.15 Root mean square position error due to aircraft movement
Stations: Kautokeino and Vardø

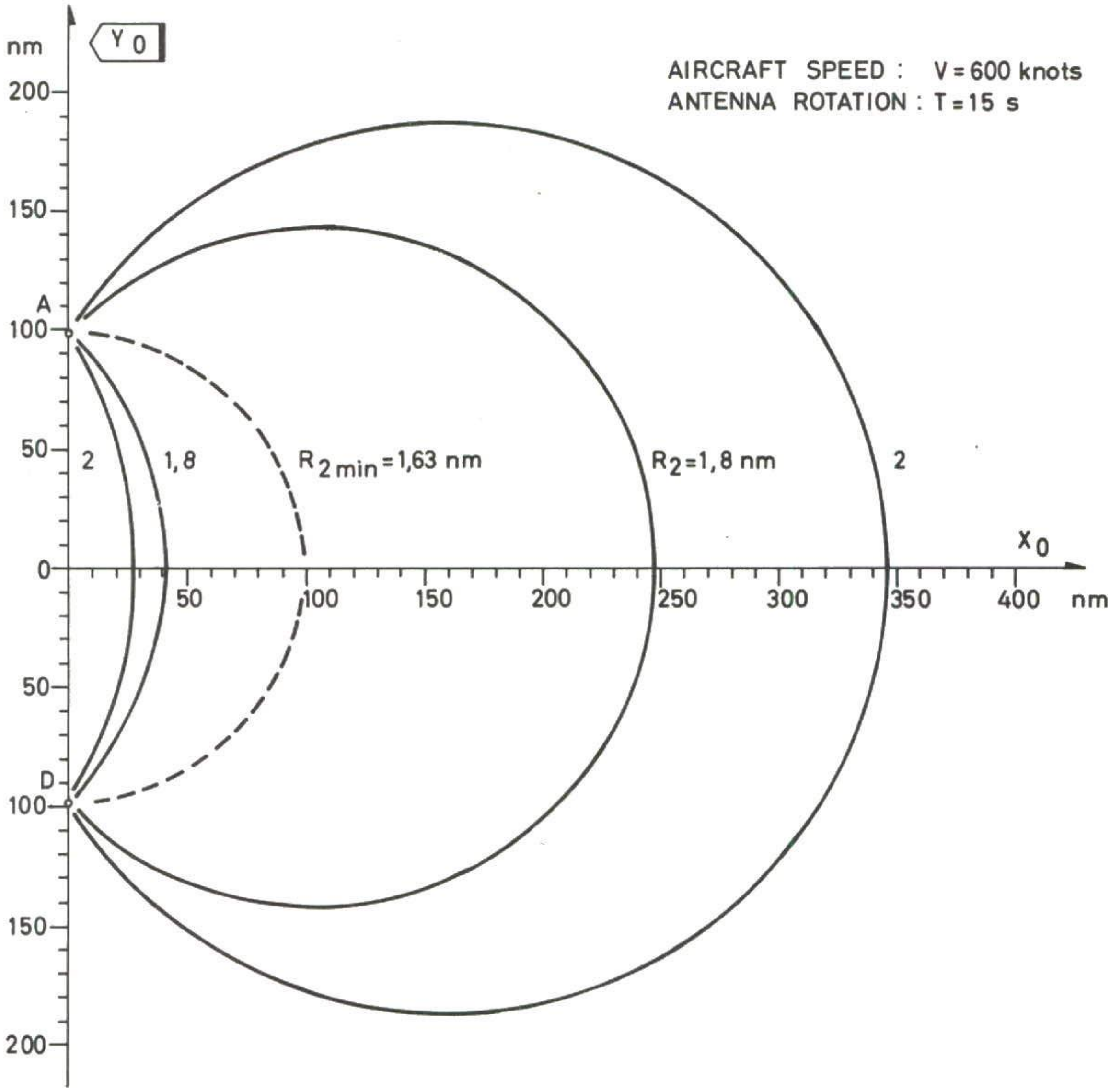


Figure 3.16 Root mean square position error due to aircraft movement
Stations: Sørreisa and Honningsvåg

3.7 Inaccuracy due to operator updating speed

The operator updates a strobe whenever there is a noticeable discrepancy between the jamming direction and the strobe information previously transmitted. For aircraft flying on a nearly radial course or for distant aircraft frequent updating is not needed. Updating for every antenna revolution is only required for aircraft flying rather close to the strobe reporting stations.

To assess the operator updating speed the following experiments were carried out: A readback strobe pattern was set up, with strobe No 1 at 10°, No 2 at 20°, etc ending with strobe No 10 at 100°. All targets were then deemed to appear 10° in advance, and the strobes were updated starting with No 1, which was set at 0°. Strobe No 2 was initiated on the afterglow of the previous strobe No 1, strobe No 3 on the afterglow of No 2, and so forth. When strobe No 10 was updated, all strobes were again transferred 10° counterclockwise, and the process was repeated. All strobes were required to appear exactly on the afterglow of the previous strobe, and whenever there was an error of one increment or more, a correction was made.

For each operator the time required for every ten updatings was recorded. Results for a completely inexperienced operator are presented in Figure 3.17. The exercise shows no signs of fatigue; a learning process rather is indicated. The inexperienced operator demonstrated a time average of 1.8 seconds per strobe. For experienced operators the updating time was below 1 second per strobe.

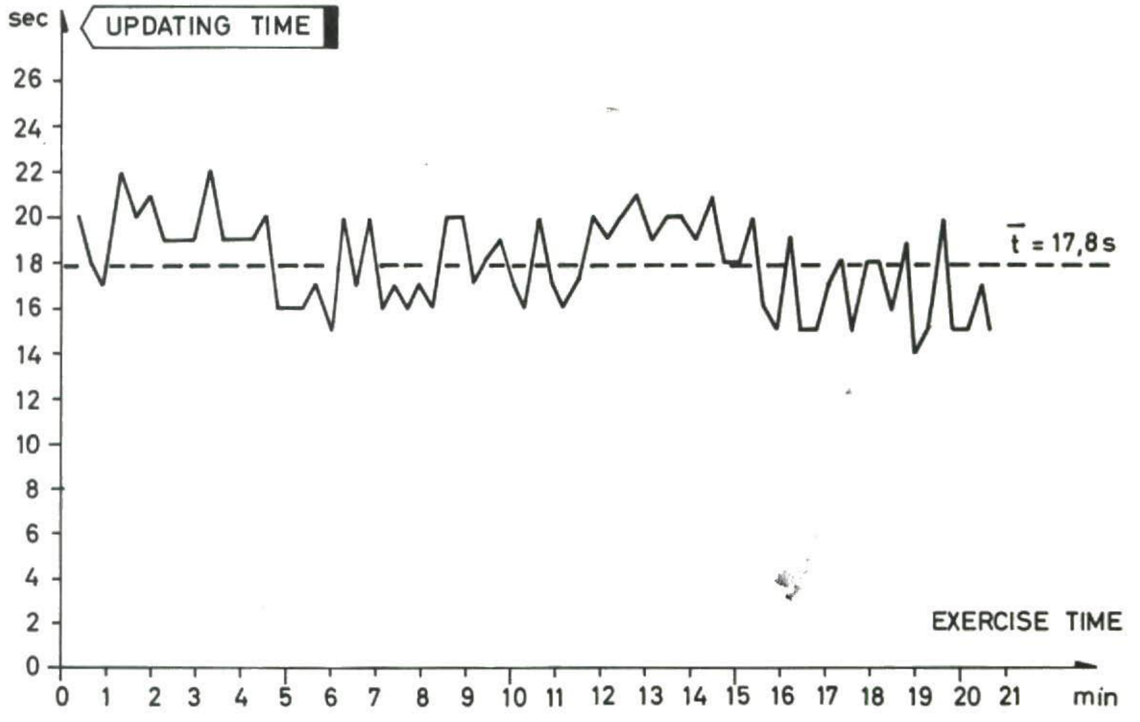


Figure 3.17 Updating time for 10 strobes as a function of exercise time for an inexperienced operator

For realistic flights it is therefore easy for the operator to perform all required updatings during one antenna revolution period.

The updating time adds to the inaccuracy discussed in Section 3.6 an amount corresponding to the aircraft movement in 1 - 2 seconds. This amount is only a small fraction of a mile and may therefore be disregarded.

3.8 Error due to the curvature of the earth

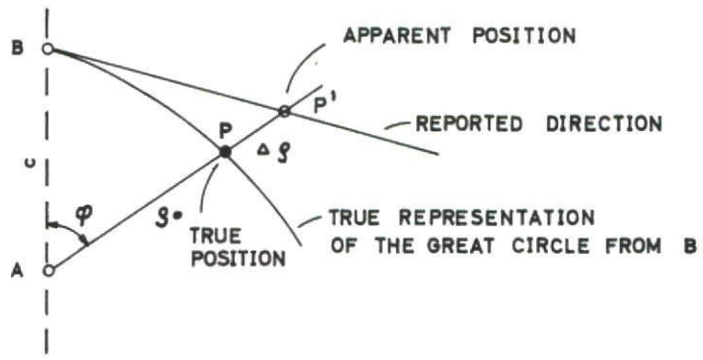


Figure 3. 18 Error due to the curvature of the earth

Assume that in Figure 3. 18 a jammer located at position P is direction-found by stations A and B, A being the triangulation centre. The great circle path through A and P is in A's radar coordinates represented by a straight line. Likewise, the great circle path B-P is represented on B's display as a straight line. The angle between the latter line and the North direction is now transmitted to A, and there displayed as a straight line, giving an intersection at point P'. The true great circle path through B-P would, however, be represented by a curved line in A's radar coordinates. A radial error $\Delta\rho$ therefore results on the triangulation table.

The target is thus by passive means decided to be in position P', whereas it would be located in position P by the active radar.

In Figure 3.19 the radial error has been calculated for a typical base line of 100 nm for targets at two different altitudes. A standard atmosphere has been assumed.

The error can be compensated for by suitable overlays on the triangulation table if found necessary.

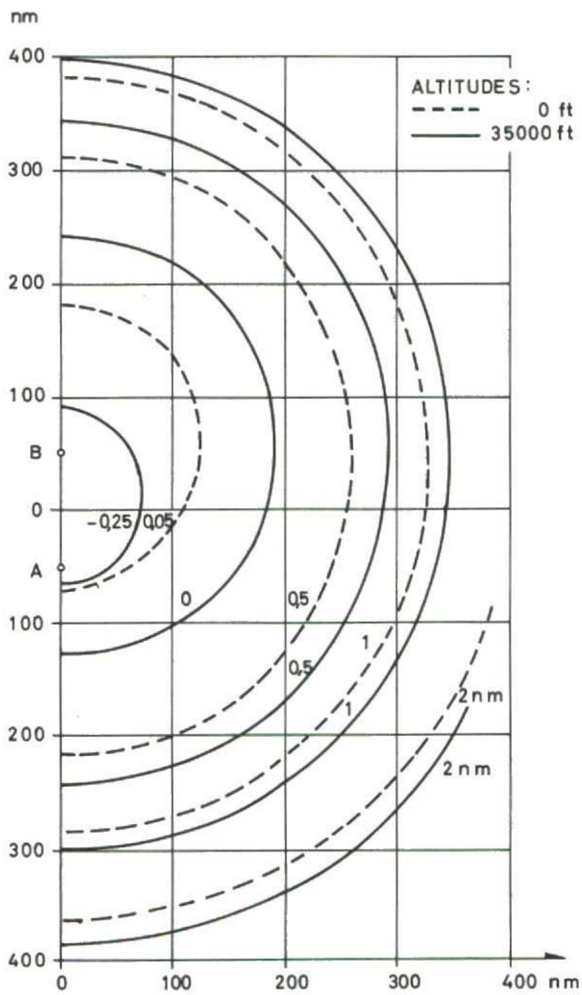


Figure 3. 19 Loci of radial error due to the curvature of the earth
Baseline = 100 nm

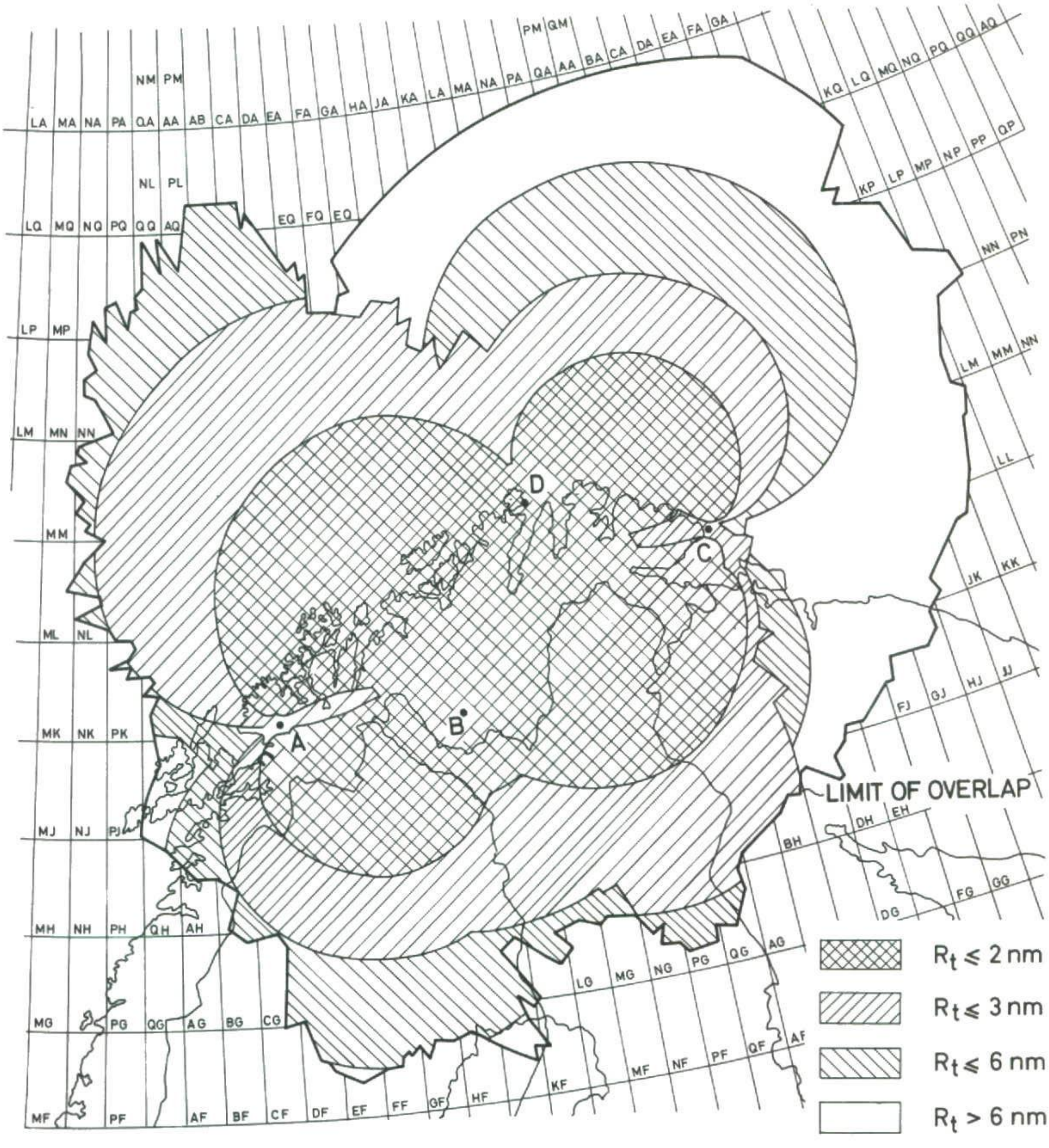


Figure 3.20 Resultant radius of uncertainty

Probability W = 50%
Target velocity = 600 mph
Altitude = 40 000 ft

3.9 Total position error

The predominant errors discussed in Sections 3.5 - 3.8 are:

a) Positional error due to angular errors

b) Positional error due to aircraft movement

c) Radial error due to the earth's curvature

Using standard statistical rules, the errors have been combined, and are presented in Figure 3.20 for Mach 1 targets at 40 000 ft altitude. It has been assumed that the triangulation operator in cases of more than two intersections per target employs those which intersect at the least acute angle. If operator prediction and smoothing are used, the expected accuracy is better than indicated.

3.10 Flight tests

As discussed in Section 3.1, means have not been available for actual measurements employing airborne barrage jammers, and the results given in Figure 3.20 can therefore for the time being not be experimentally verified.

As a check, flight tests have, however, been carried out using IFF responses of quiet targets to simulate jamming. In Figure 3.21 a typical AVA display of IFF strobes (from five targets) is shown. The IFF antenna has a beamwidth of approximately 5°, and therefore gives a much poorer resolution than the radar antenna.

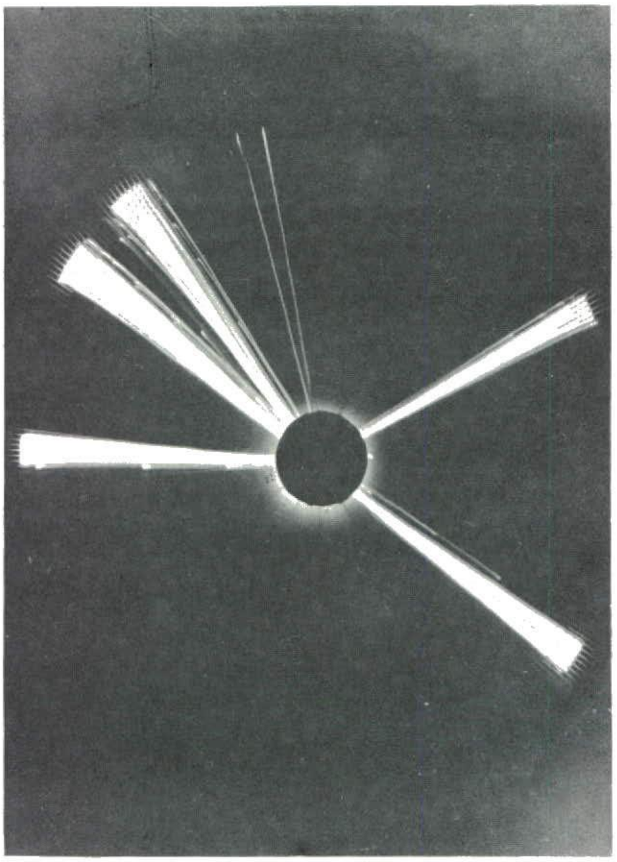


Figure 3.21 Typical AVA display of IFF strobes
No of targets: 5

An example of an interception exercise is shown in Figure 3.22. As target and fighter were employed two F-104G's. The target was squawking IFF mode 1, whereas the fighter was quiet. The fighter used its inertial navigation system for its own navigation, and was only told triangulated data for the target position. The target was successfully intercepted twice.

During the south-west path of the target, the triangulated position was for every antenna revolution directly compared with the skin paint as observed on the triangulation table. The results as given in Figure 3.21 essentially support the curves in Figure 3.20 when due allowance is made for the wider antenna beamwidth.

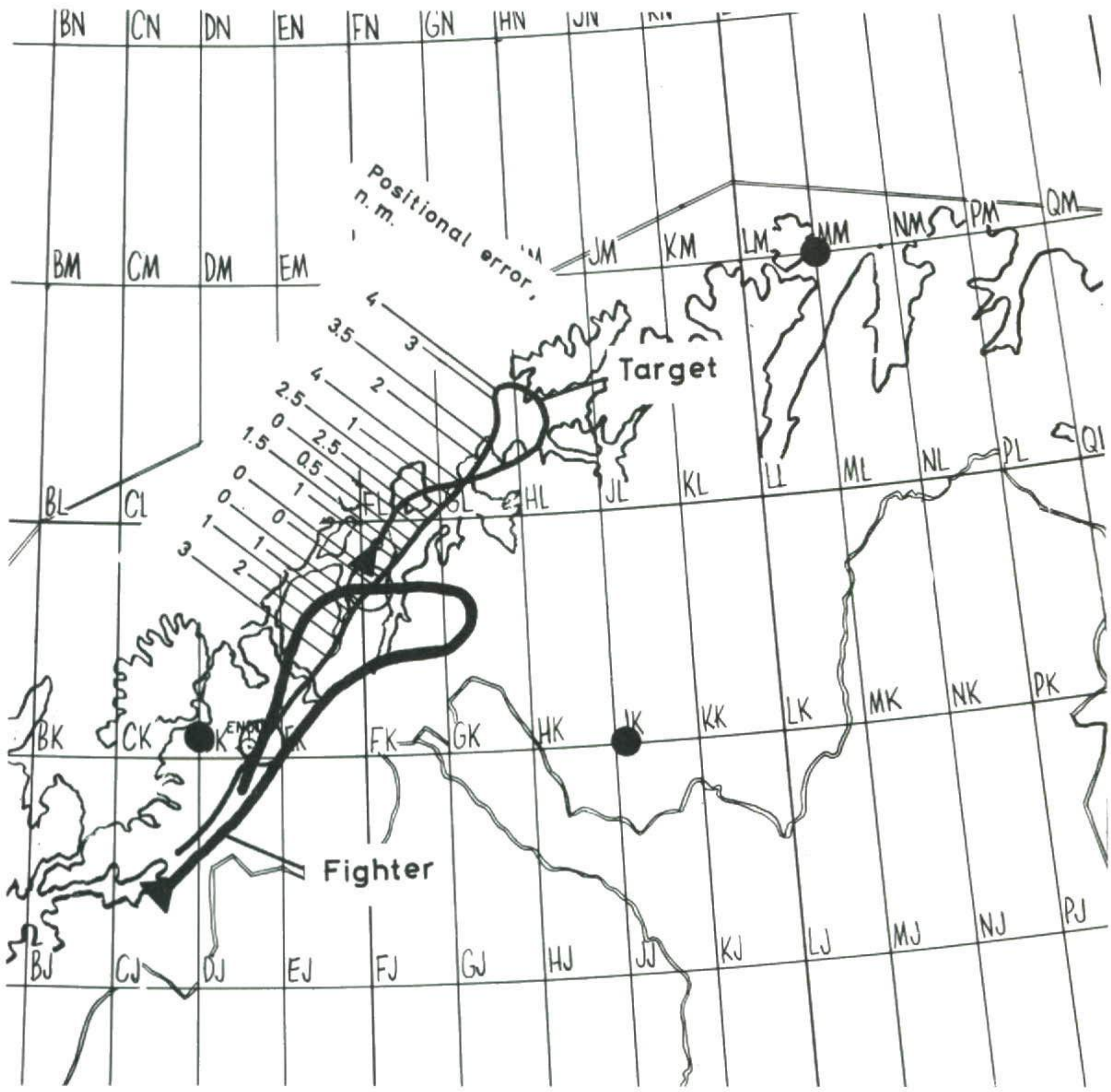


Figure 3.22 Interception exercise using IFF strobes for locating the target

Elevations: Target 28 000 ft, fighter 30 000 ft. Target velocity: 650 mph. Aircraft: Two F-104G's.

3.11 Tape simulated map exercises

For the purpose of evaluating the performance of the triangulation operators several map exercises were prepared and converted to teleprinter tape programs as described in Section 2.3.3. Strobe updating was in real time, and random errors were added to the strobe angles to simulate strobe reporting operator inaccuracies.

The triangulation table was manned by three regular operators. The operators were briefed beforehand on the principles of triangulation and had taken part in a few simulated exercises employing tape programs and IFF flights.

The operators had no prior knowledge of the exercise programs. As the semi-automatic CRC equipment will not be operative until late Summer 1964, telling was done aurally in Georef coordinates, and recorded on magnetic tape which was later used for final plotting. All plots reproduced in the present report are unedited.

Due to the Georef telling procedure, positions are quantized in sixths of a degree, which for North Norway corresponds to 6 nm in the north-south direction, and slightly less than 3 nm in the east-west direction. As the operator quantizing errors greatly exceed the DAF system inaccuracy, no attempt has been made to calculate the positional errors from the operator telling. Under the circumstances, the important factor to be determined is to what extent the operators correctly detect and follow the tracks, and not the accuracy with which the plots are aurally told. In the semi-automatic mode, telling will be by joystick, and the telling inaccuracies will be greatly reduced.

3.11.1 Legend

The legend used may be explained with reference to Figure 3.23.

Initial target positions are indicated by filled arrows. Target positions for every subsequent 10 minutes flying time are shown with open arrows. When two targets follow the same path, a double arrow is used to indicate the second target positions.

As part of the exercise, certain strobe reporting stations were deemed out, and the corresponding strobes were removed by the supervisor. Such stations are indicated by open circles.

The Georef range at the triangulation centre (colocated with A) is 320 nm. Tracks detected outside the Georef range were usually not told until they came within Georef range.

3.11.2 Normal programs

Results of exercises including probable attack flight paths are given in Figures 3.24 - 3.29.

Figure 3.24 - One fast jamming aircraft (01) is penetrating North Norway under the concealment of jamming from three aircraft flying at low or moderate speeds north of Norway. The altitudes are high, as indicated by the SRS ranges given.

All targets were correctly detected and tracked.

Figure 3.25 - Three fast jamming aircraft penetrate North Norway under the concealment of five other aircraft of slow and moderate speeds.

All targets were correctly detected and tracked.

Figure 3.26 - The exercise is somewhat similar to those shown in Figures 3.24 - 3.25, but the altitudes are lower, indicated by an SRS range of 200 nm.

Tracks 02, 03 and 05 are correctly established from the beginning. Targets 01 and 04 are initially ghost tracked; then the correct intersections are selected.

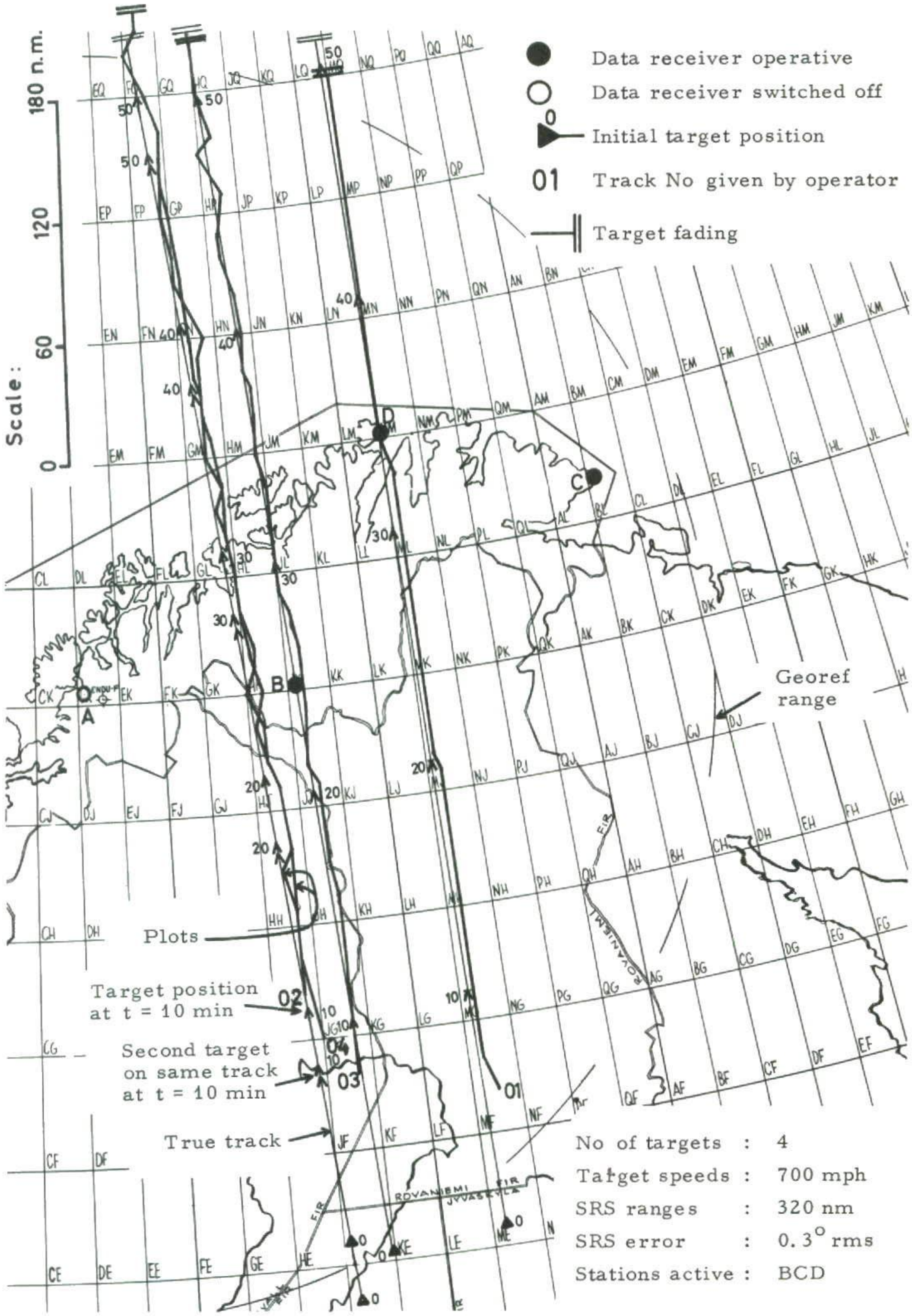


Figure 3.23 Tape simulated exercises, legend

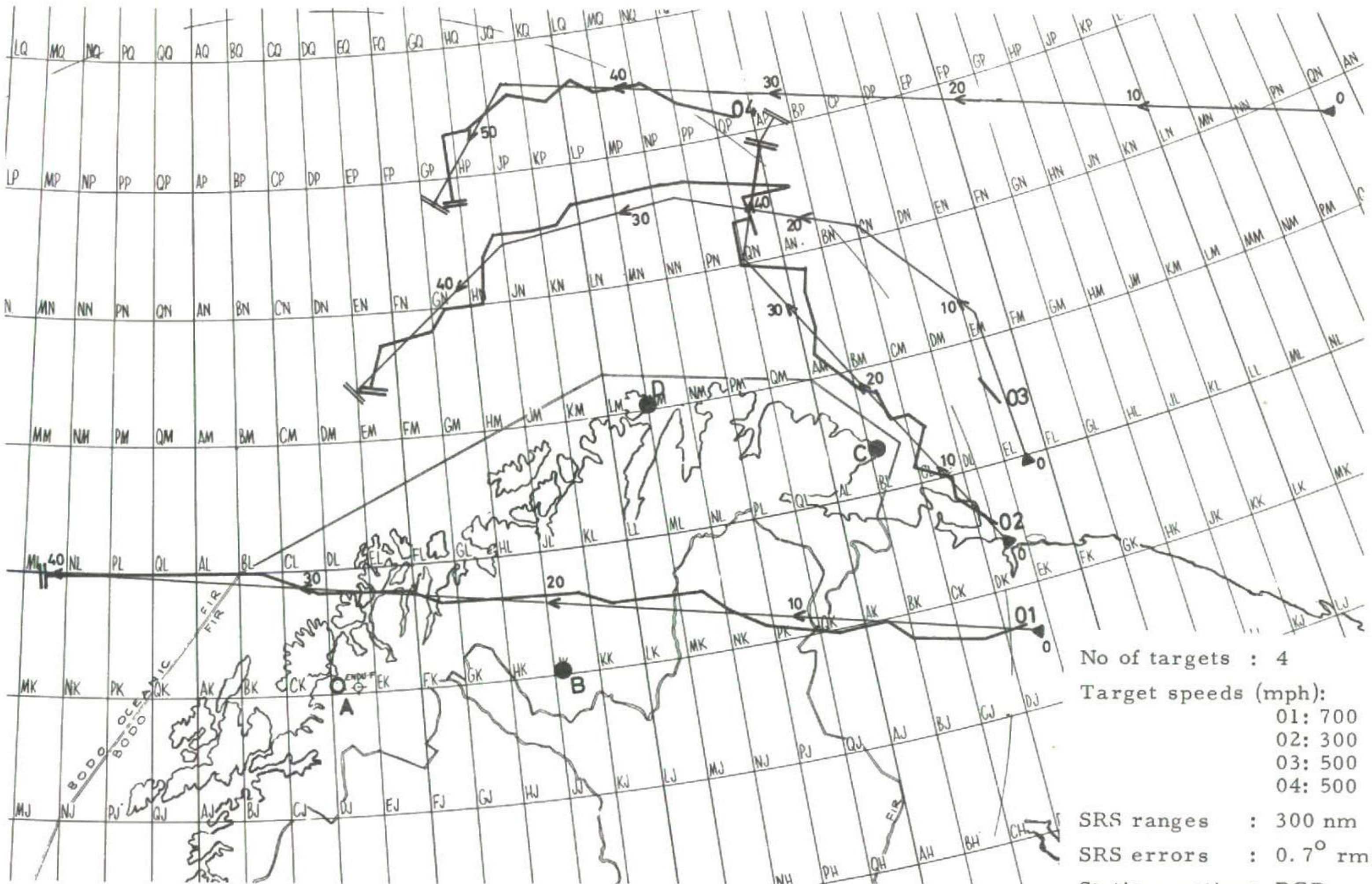


Figure 3.24 Tape simulated exercise

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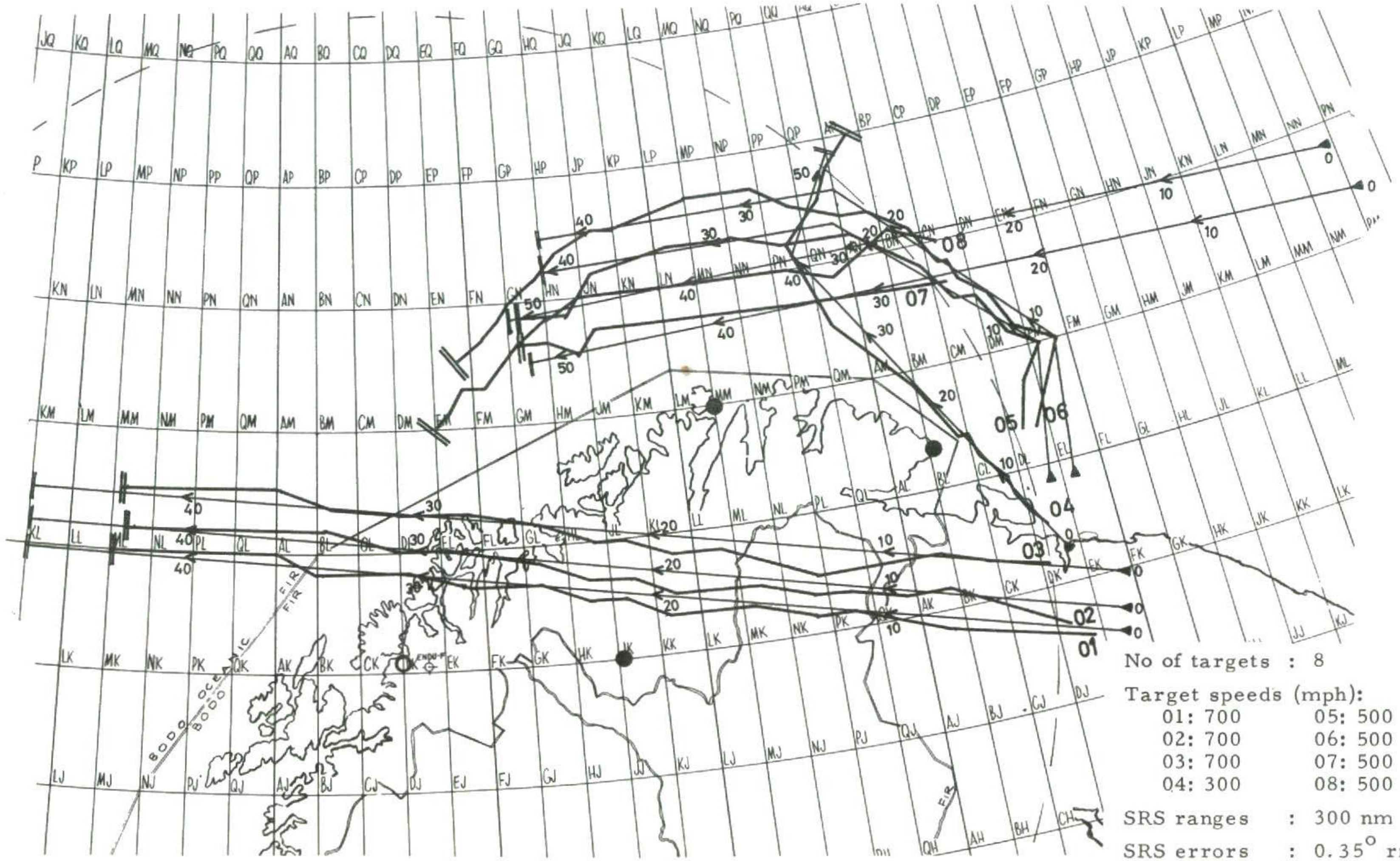

No of targets : 8

Target speeds (mph):

01: 700	05: 500
02: 700	06: 500
03: 700	07: 500
04: 300	08: 500

SRS ranges : 300 nm

SRS errors : 0.35° rms

Stations active: BCD

Figure 3.25 Tape simulated exercise

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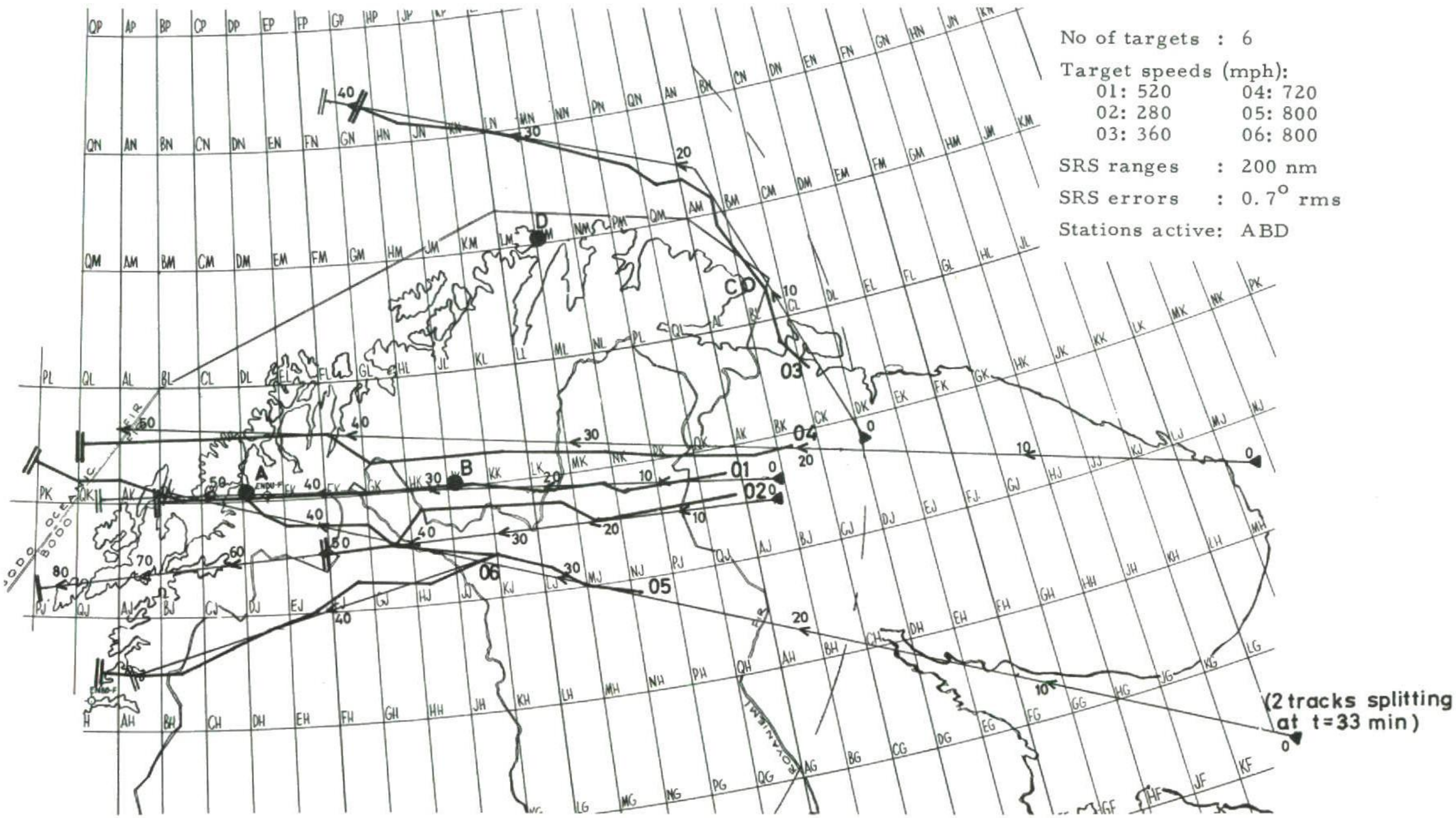
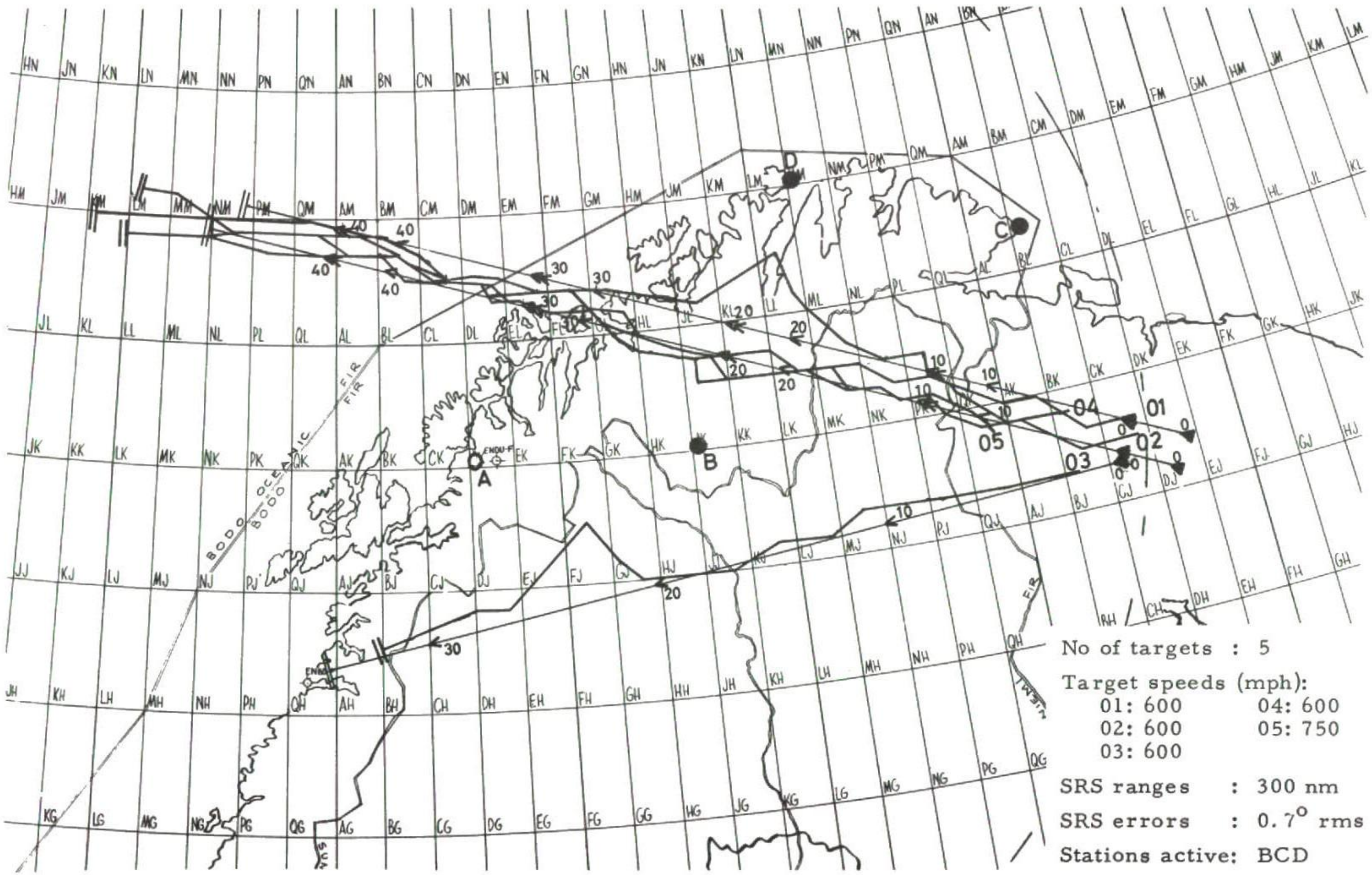


Figure 3.27 Tape simulated exercise

SECRET



No of targets : 5

Target speeds (mph):
01: 600   04: 600
02: 600   05: 750
03: 600

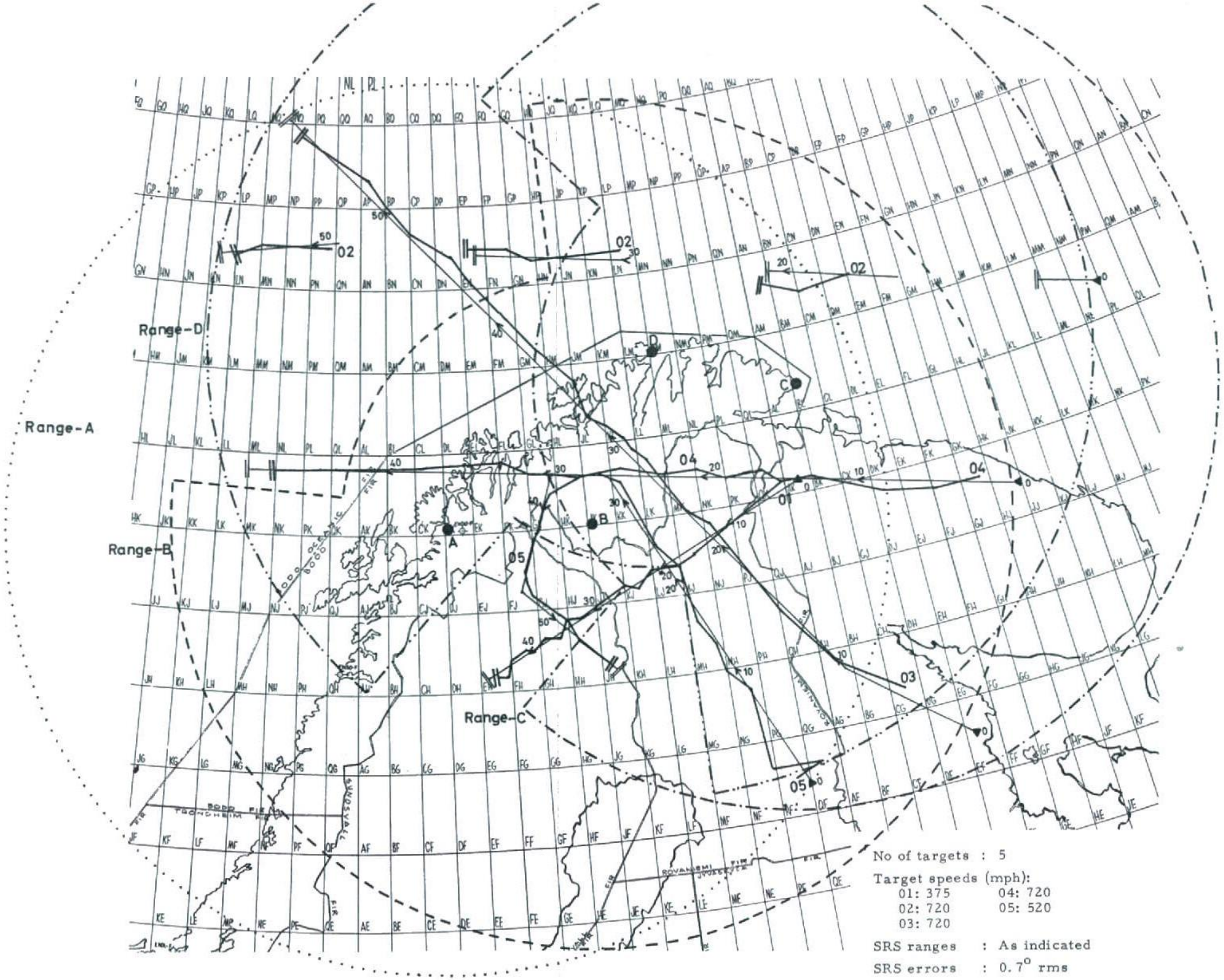
SRS ranges : 300 nm

SRS errors : 0.7^{o} rms

Stations active: BCD

Figure 3.28 Tape simulated exercise

SECRET



No of targets : 5

Target speeds (mph):
01: 375
02: 720
03: 720
04: 720
05: 520

SRS ranges : As indicated

SRS errors : 0.7° rms

Stations active: ABCD

Figure 3.29 Tape simulated exercise

Figure 3.27 - Five aircraft are penetrating North Norway at various velocities, and one flies on a normal route north of Norway. One aircraft breaks off, heading for Bodø.

Tracks 01 - 04 are correctly established within 3 - 5 minutes, and track 05 within 10 minutes. The track splitting 05 - 06 is immediately detected. The slow target 02 is for approximately 20 minutes (from t = 20 to t = 40) ghost tracked on a parallel course.

Figure 3.28 - Four jammers (01, 02, 04, 05) fly in a square formation so arranged to create a number of ghosts difficult to distinguish from real targets. One aircraft (03) breaks off, heading for Bodø. The purpose of the exercise was to confuse the operators by the deghosting of the first four targets, drawing their attention away from target 03. The latter target was, however, immediately detected and tracked. Two of the other targets (01 and 02) were properly detected and tracked, whereas 04 and 05 were ghost-tracked near their true flight paths most of the time.

Note the excursions resulting when some of the targets cross the station base lines (in section LL when baseline BD is crossed, in section FJ when baseline BC is crossed). These excursions would probably not occur with station A operative.

Figure 3.29 - In this exercise a slow aircraft (01) is taking off from an airfield close to the Norwegian border, heading south-west for Trøndelag. Aircraft 02 is flying north of Norway, jamming every alternate 10 minutes. Aircraft 03 flies north-west from a White Sea base. 04 heads straight west from a Kola base. 05 is heading north-west from a southern base and encircles Kautokeino. The strobe reporting stations have sectors of reduced range as shown.

All targets were correctly detected and tracked.

3.11.3 Special exercises

In order to obtain a quantitative measure of the limiting ability of the triangulation operators in detecting and tracking single targets within raids, a chessboard pattern of 5 x 5 squares was designed as shown in Figure 3.30.

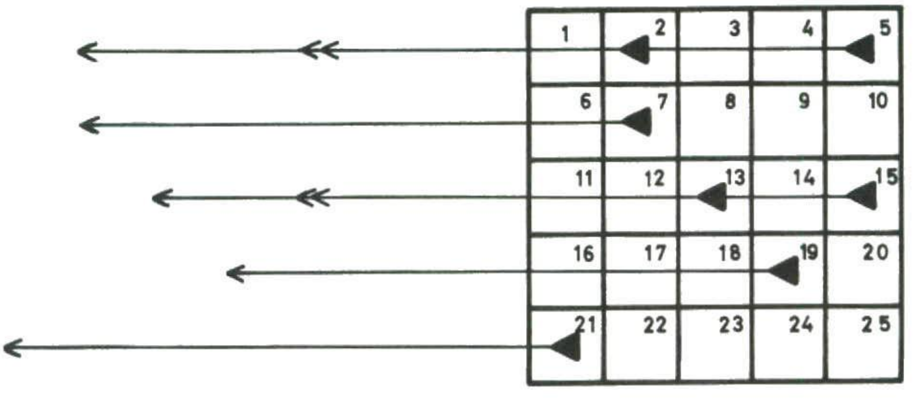


Figure 3.30 Basic flight pattern, and example of exercise with 7 targets
(Random numbers drawn: 13, 5, 19, 7, 2, 21, 15)

For each exercise the side of the basic square was selected as 10, 20 or 30 nm. The number of targets was varied between 4 and 8, and in each case the target locations inside the basic pattern were selected using tables of random numbers.

All targets were programmed to fly along straight and parallel lines at a velocity of 700 mph. In order that the basic patterns should not be recognized by the operators, the exercises were played in random sequence with different main headings, and exercises as previously shown in Figures 3.24 - 3.29 were interlaced. For each exercise, all strobes from one of the four stations were erased.

The exercises were programmed with root mean square angle errors 0.3° and 0.6°. The results obtained showed no significant difference between the two cases, indicating that the system angular resolution (mean rms value $\approx 0.6^{\circ}$) does not set the limiting accuracy and detectability.

In all cases the number of targets and their approximate positions were established within a couple of minutes after a target entered the coverage area of two stations, and the requirements for Early Warning were therefore always met.

Plots for individual targets are shown in Figures 3.31 - 3.45 for an angular error of 0.6° rms.

In order that a track can be reported, it must be within Georef range and also within range of at least two strobe reporting stations. The time lag as measured from the instant the above criteria are both satisfied for a given track until the track is first reported correctly is listed in Table 3.3.

Figure	Unit square nm^2	No of jammers	Time before correct track established, min								Comments
			01	02	03	04	05	06	07	08	
3.31	10x10	4	0	1	4	5	-	-	-	-	
3.32	20x20	4	3	4	3	7	-	-	-	-	
3.33	30x30	4	1	1	3	1	-	-	-	-	
3.34	10x10	5	2	4	7	13	20	-	-	-	03 partly ghost tracked
3.35	20x20	5	1	0	2	1	2	-	-	-	
3.36	30x30	5	0	0	0	1	0	-	-	-	
3.37	10x10	6	1	6	3	9	10	16	-	-	Tracks partly interchanged
3.38	20x20	6	1	1	2	1	3	4	-	-	
3.39	30x30	6	2	1	1	2	5	4	-	-	
3.40	10x10	7	0	3	1	2	4	4	4	-	
3.41	20x20	6	9	13	5	7	3	6	-	-	
3.42	30x30	7	15	30	6	8	3	30	4	-	01 initially ghost tracked
3.43	10x10	8	5	5	2	1	1	3	13	14	08 partly ghost tracked. Other tracks partly interchanged.
3.44	20x20	8	1	0	0	1	0	5	4	3	
3.45	30x30	8	0	3	1	23	16	17	24	∞	01 ghost tracked from t = 30 to t = 40

Table 3.3 Analysis of individual target tracking within raids

3.11.4 Conclusions

As might be expected, the resolving capability of the triangulation system and its operators depends to a great extent upon the target density and the geometric relationship. For instance, in Figure 3.44 the problems are solved within 5 minutes, whereas in Figure 3.45 where the raid combination is in fact more easy, the situation is never fully resolved. The main reason is that in the latter case, due to the geometry, two stations (C and D) have almost parallel strobes when the raid arrives.

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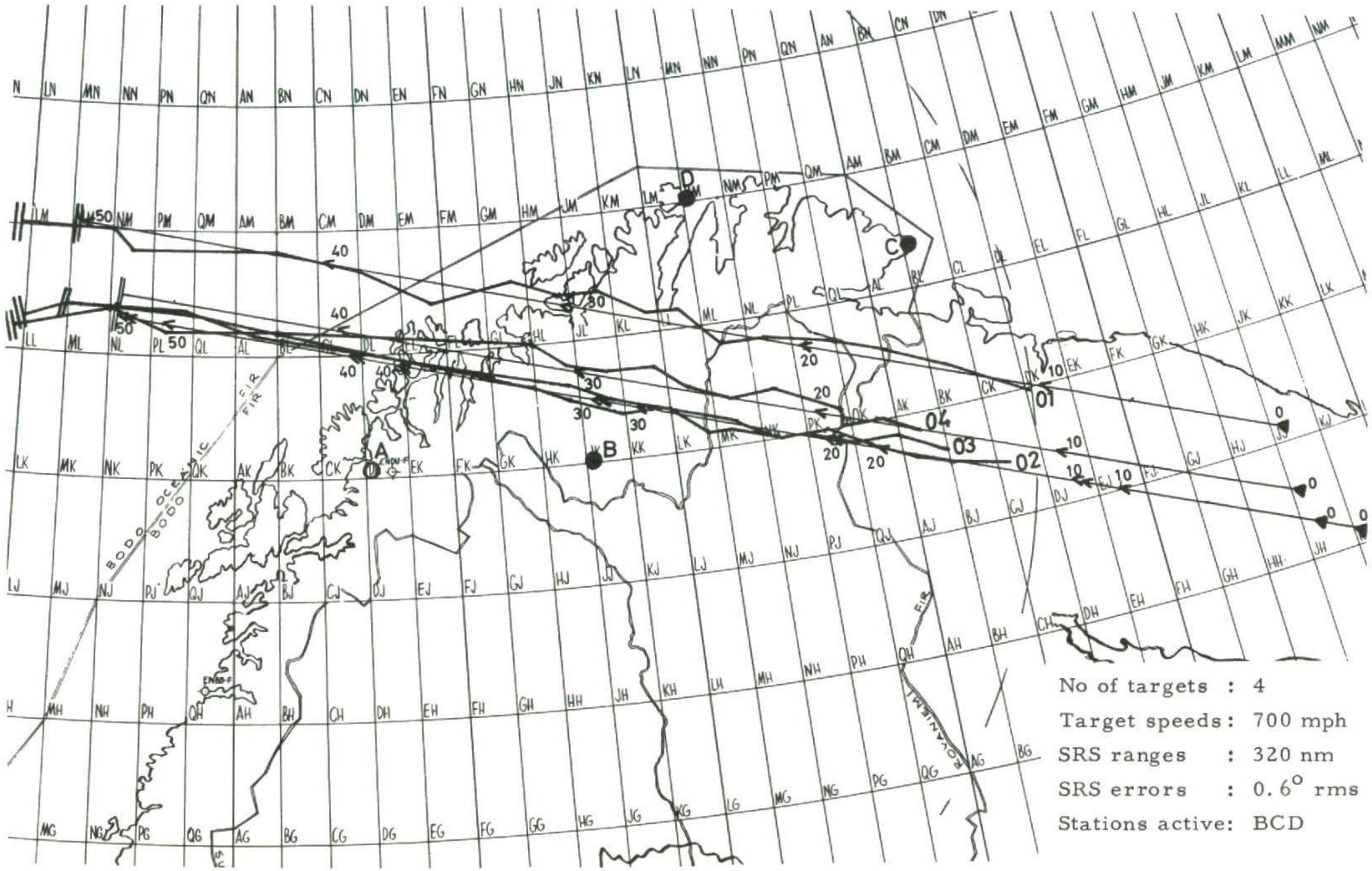

Figure 3.31 Tape simulated exercise

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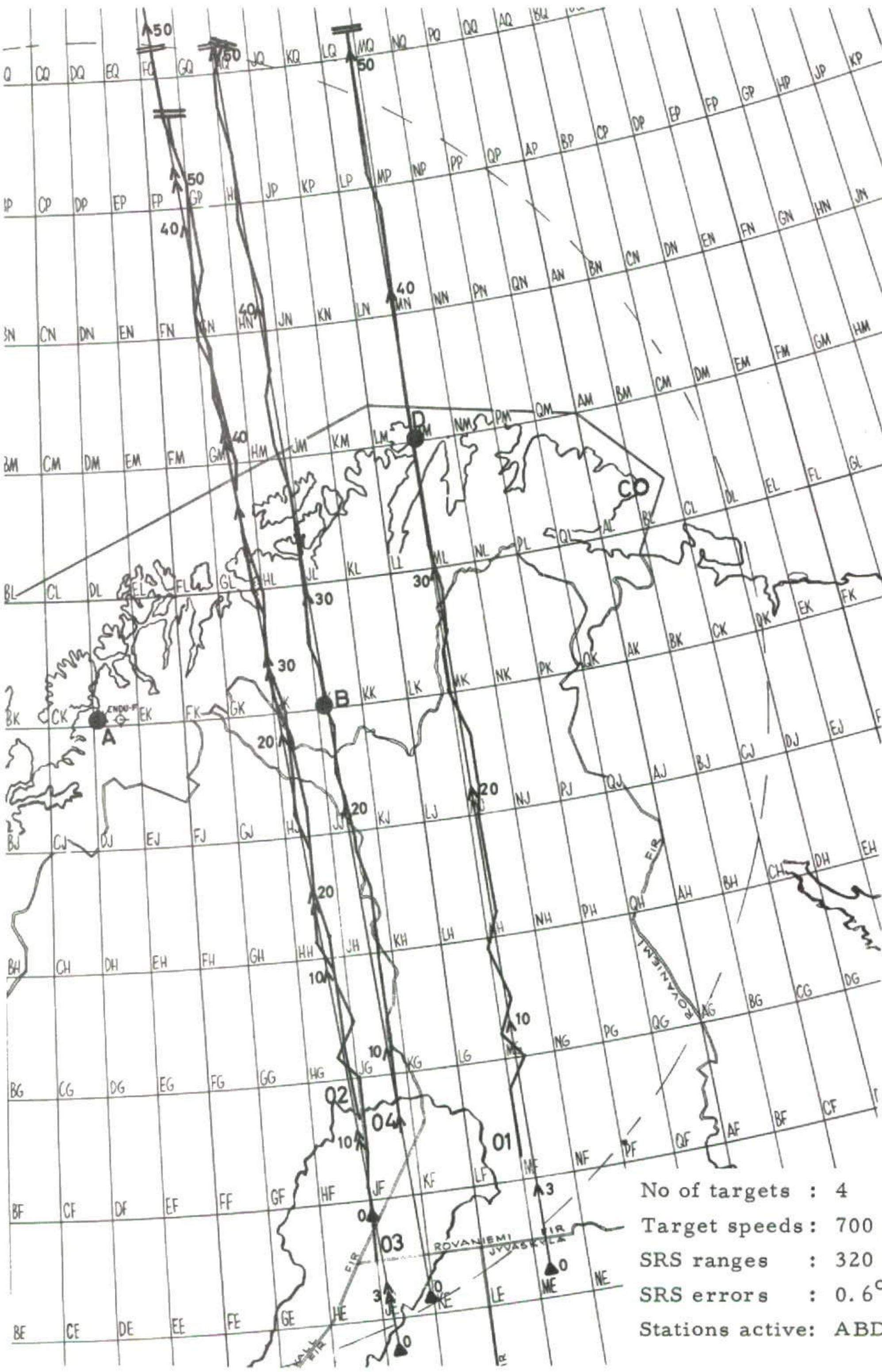
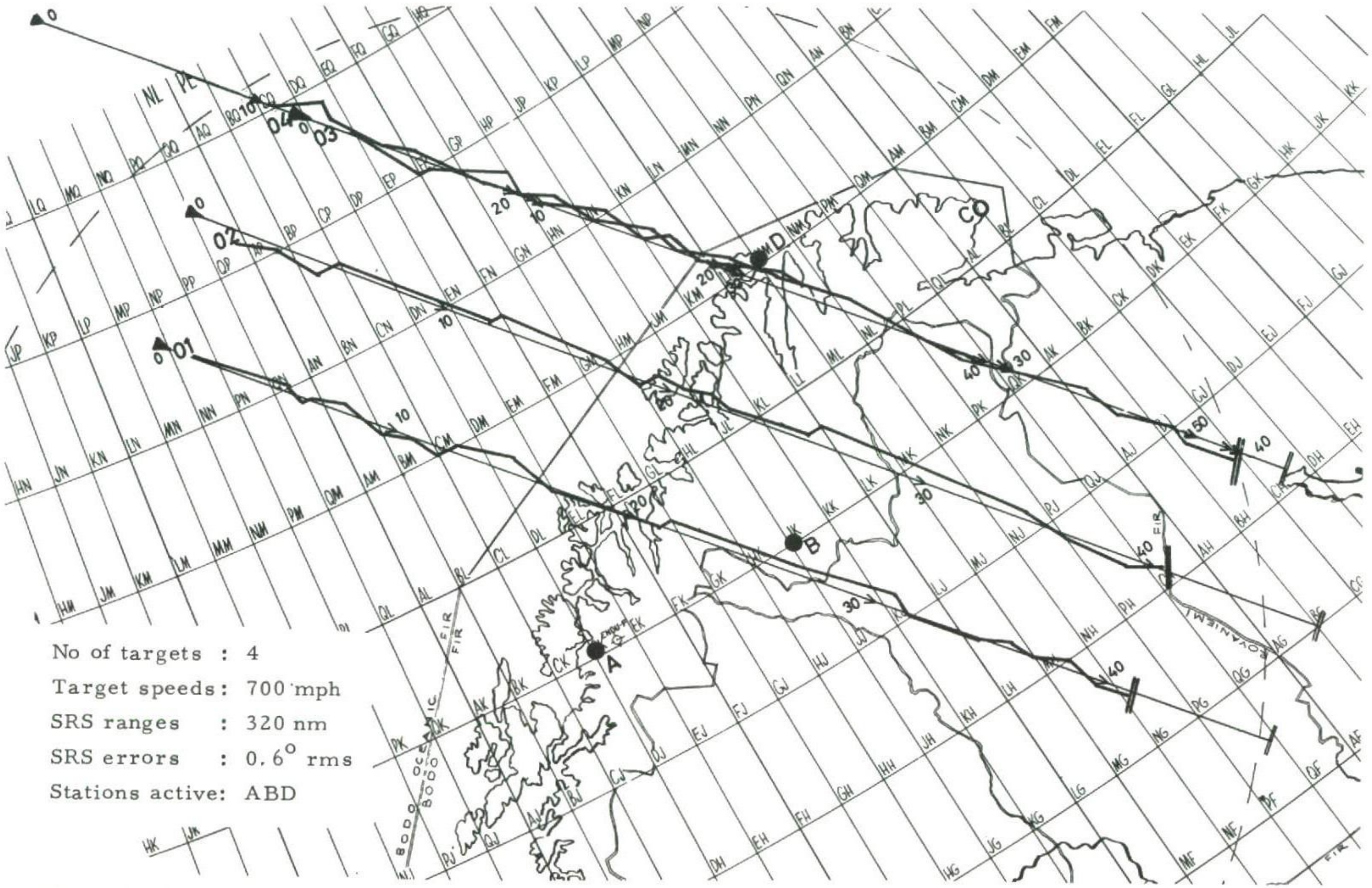


No of targets : 4
Target speeds : 700 mph
SRS ranges : 320 nm
SRS errors : 0.6° rms
Stations active: ABD

Figure 3.32 Tape simulated exercise



No of targets : 4
Target speeds : 700 mph
SRS ranges : 320 nm
SRS errors : 0.6° rms
Stations active : ABD

Figure 3.33 Tape simulated exercise

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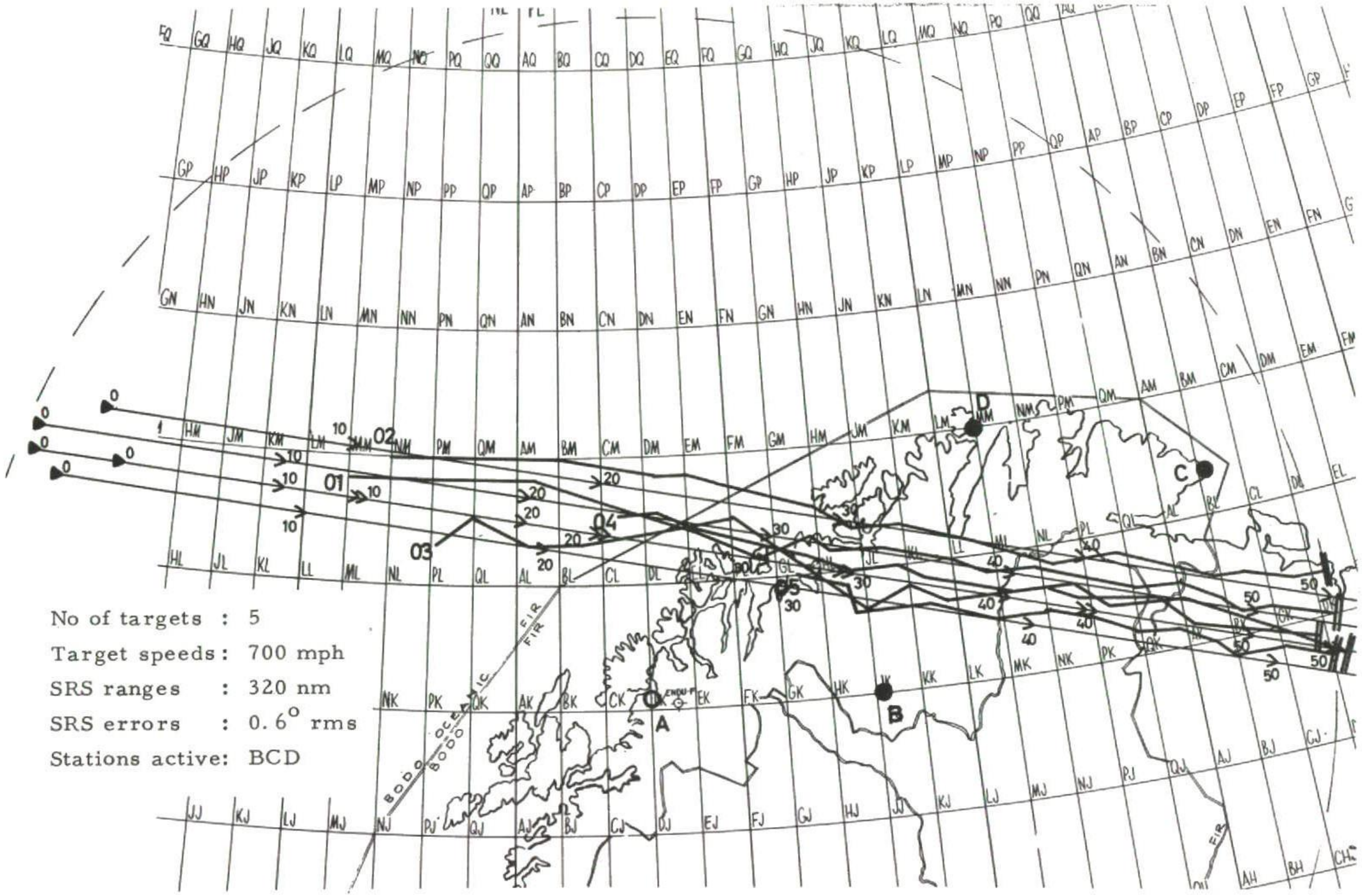

Figure 3. 34 Tape simulated exercise

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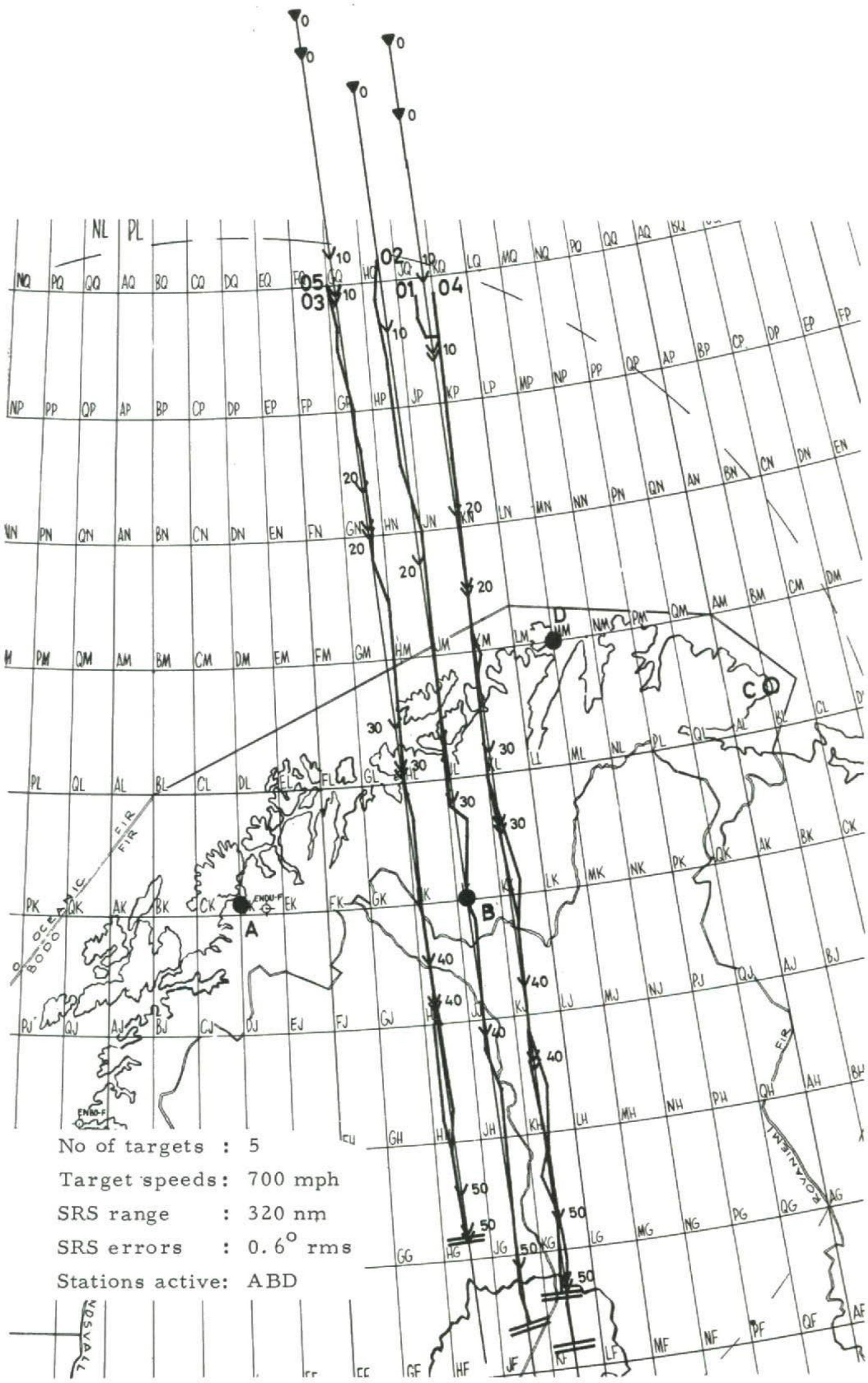

Figure 3.35 Tape simulated exercise

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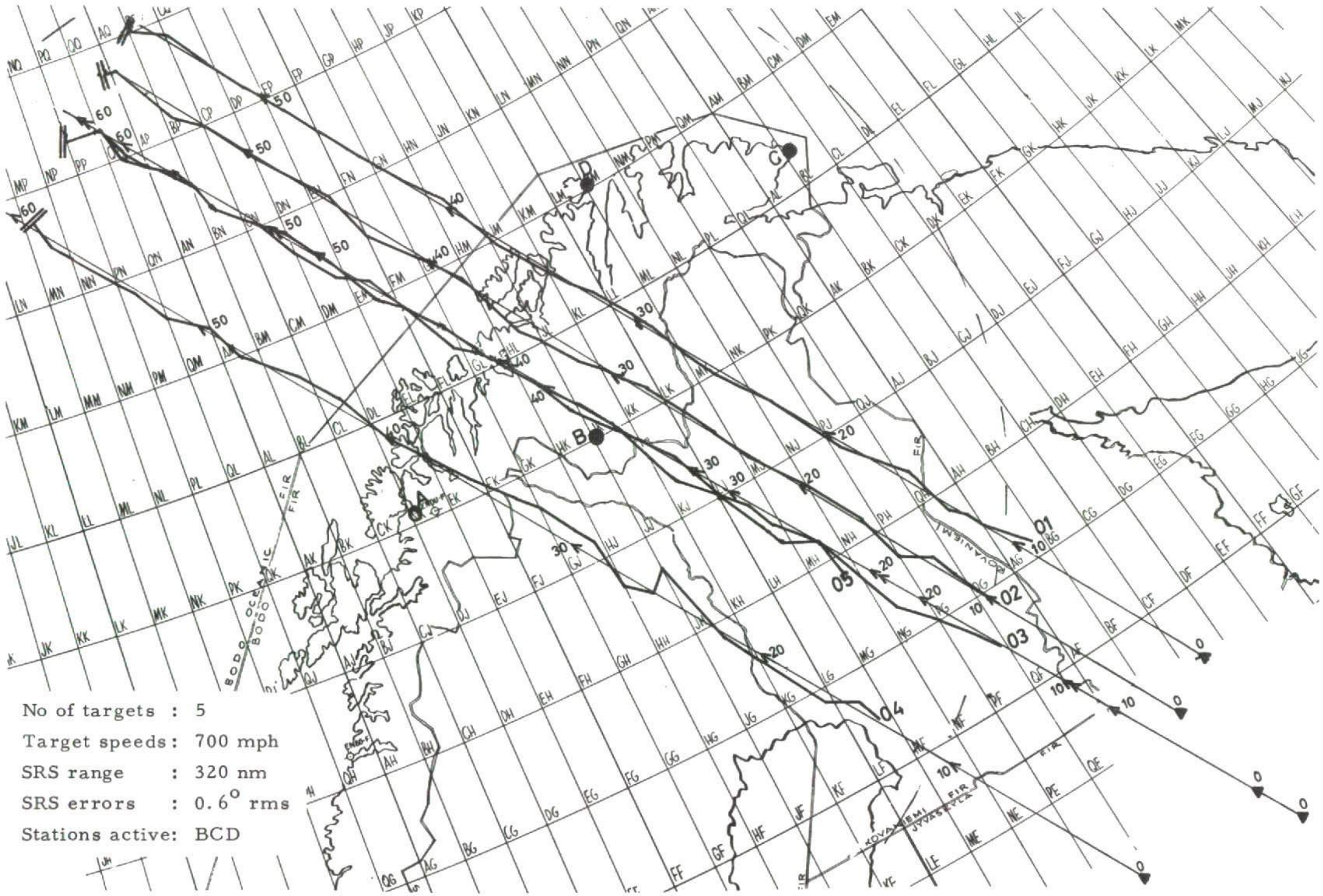
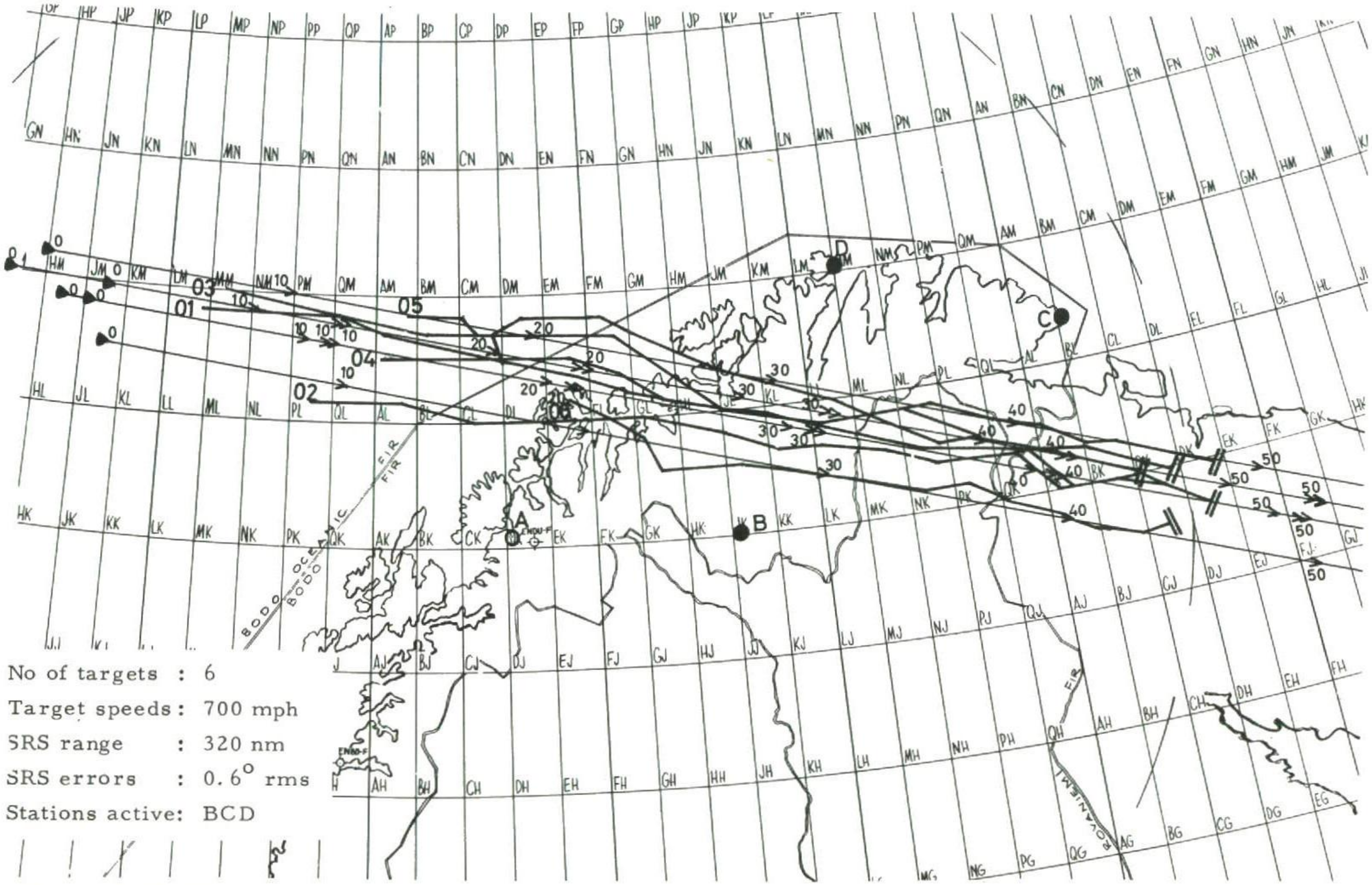


No of targets : 5
Target speeds : 700 mph
SRS range : 320 nm
SRS errors : 0.6° rms
Stations active: BCD

Figure 3.36 Tape simulated exercise

SECRET



No of targets : 6

Target speeds : 700 mph

SRS range : 320 nm

SRS errors : 0.6^{o} rms

Stations active: BCD

Figure 3.37 Tape simulated exercise

SECRET

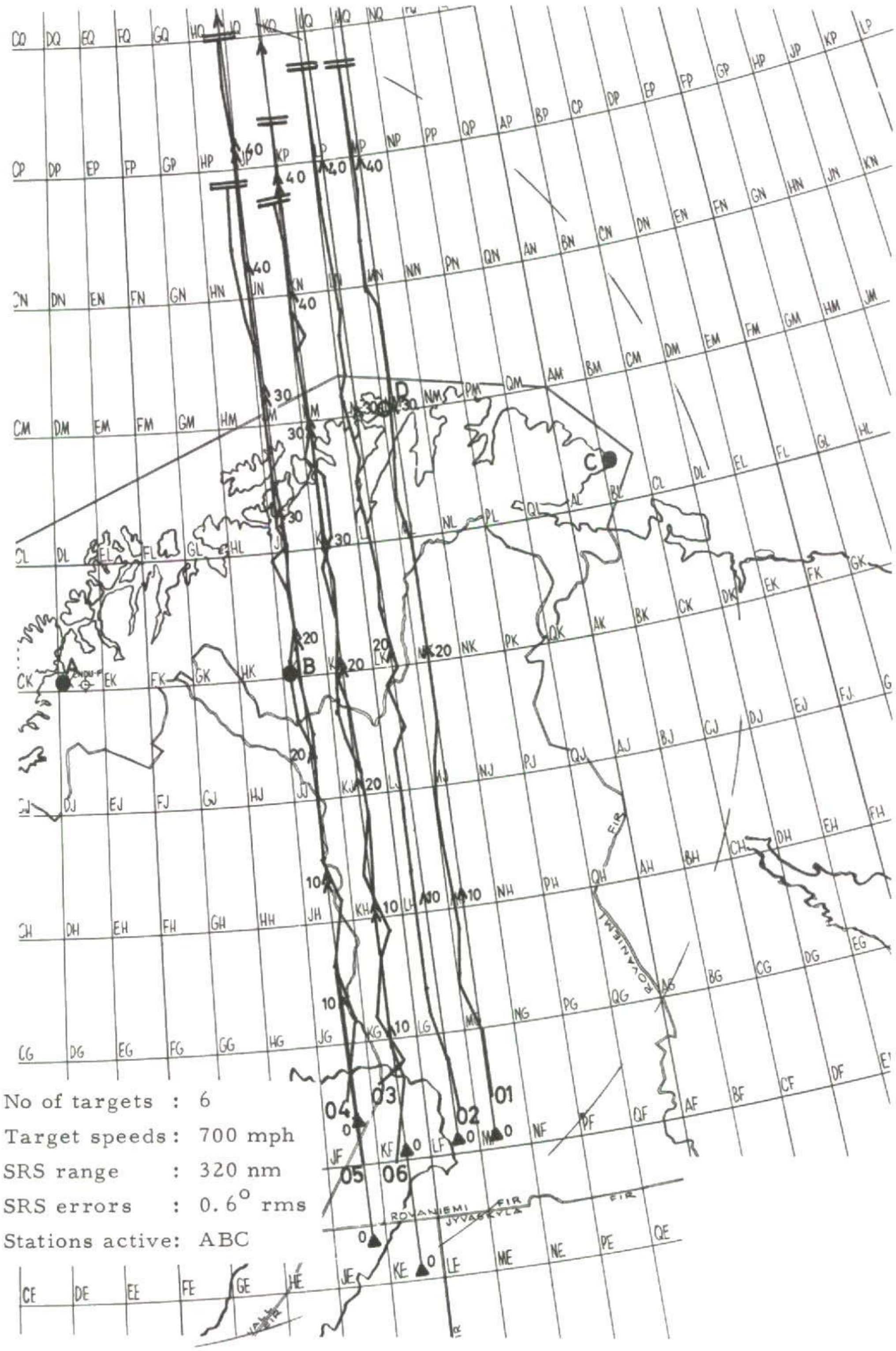


Figure 3.38 Tape simulated exercise

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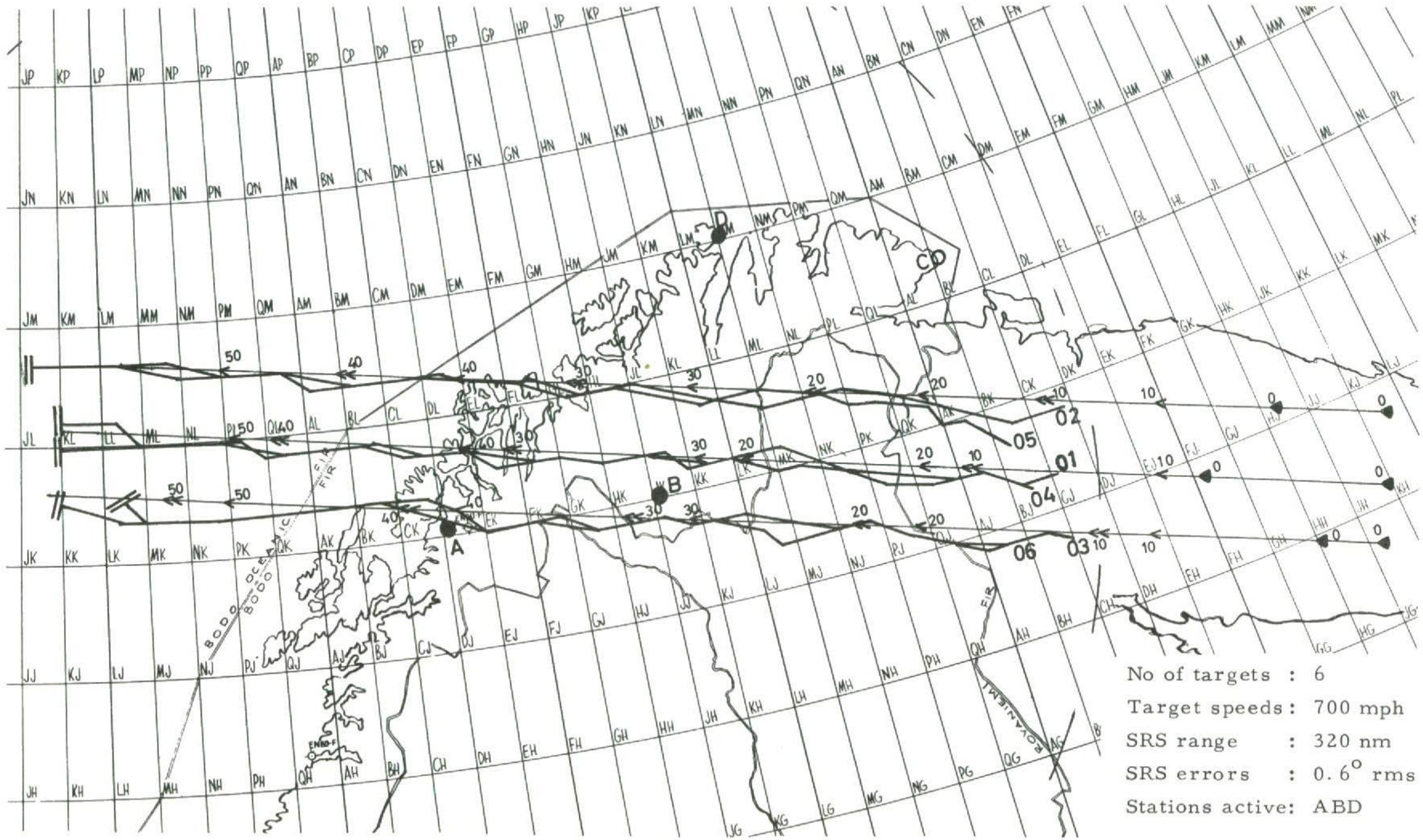

No of targets : 6

Target speeds : 700 mph

SRS range : 320 nm

SRS errors : 0.6° rms

Stations active: ABD

Figure 3.39 Tape simulated exercise

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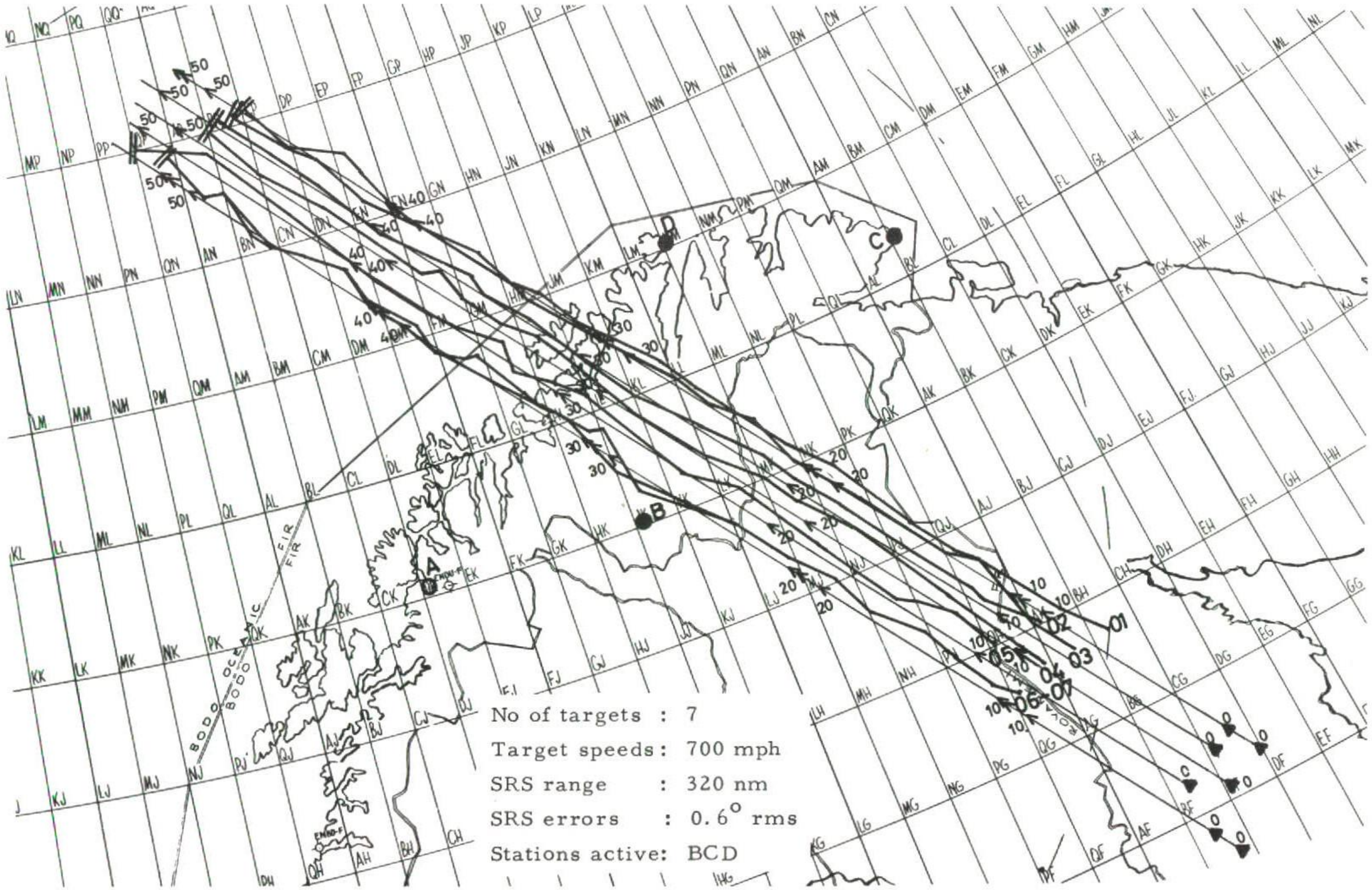

Figure 3.40 Tape simulated exercise

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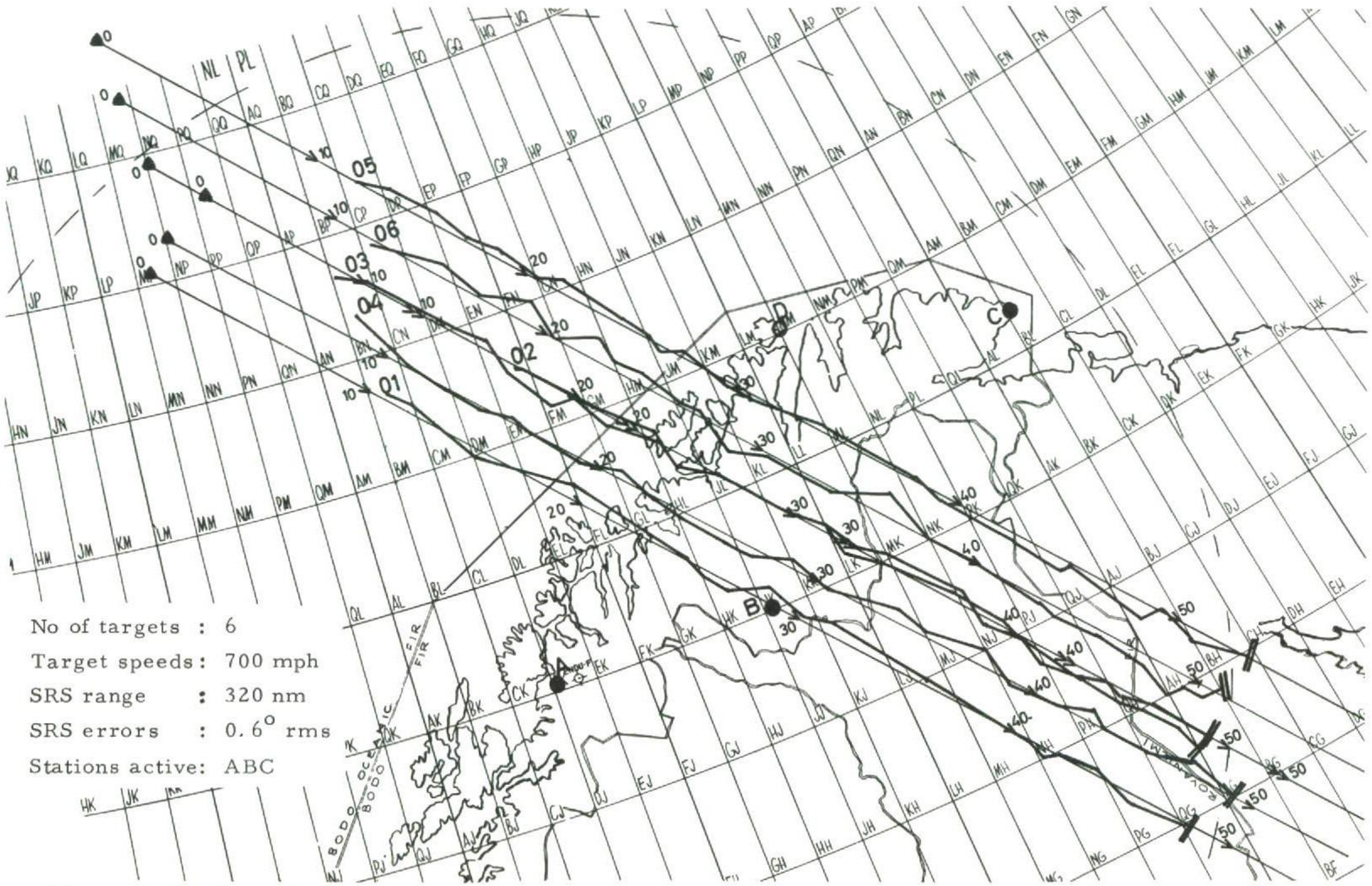

No of targets : 6
Target speeds : 700 mph
SRS range : 320 nm
SRS errors : 0.6° rms
Stations active: ABC

Figure 3.41 Tape simulated exercise

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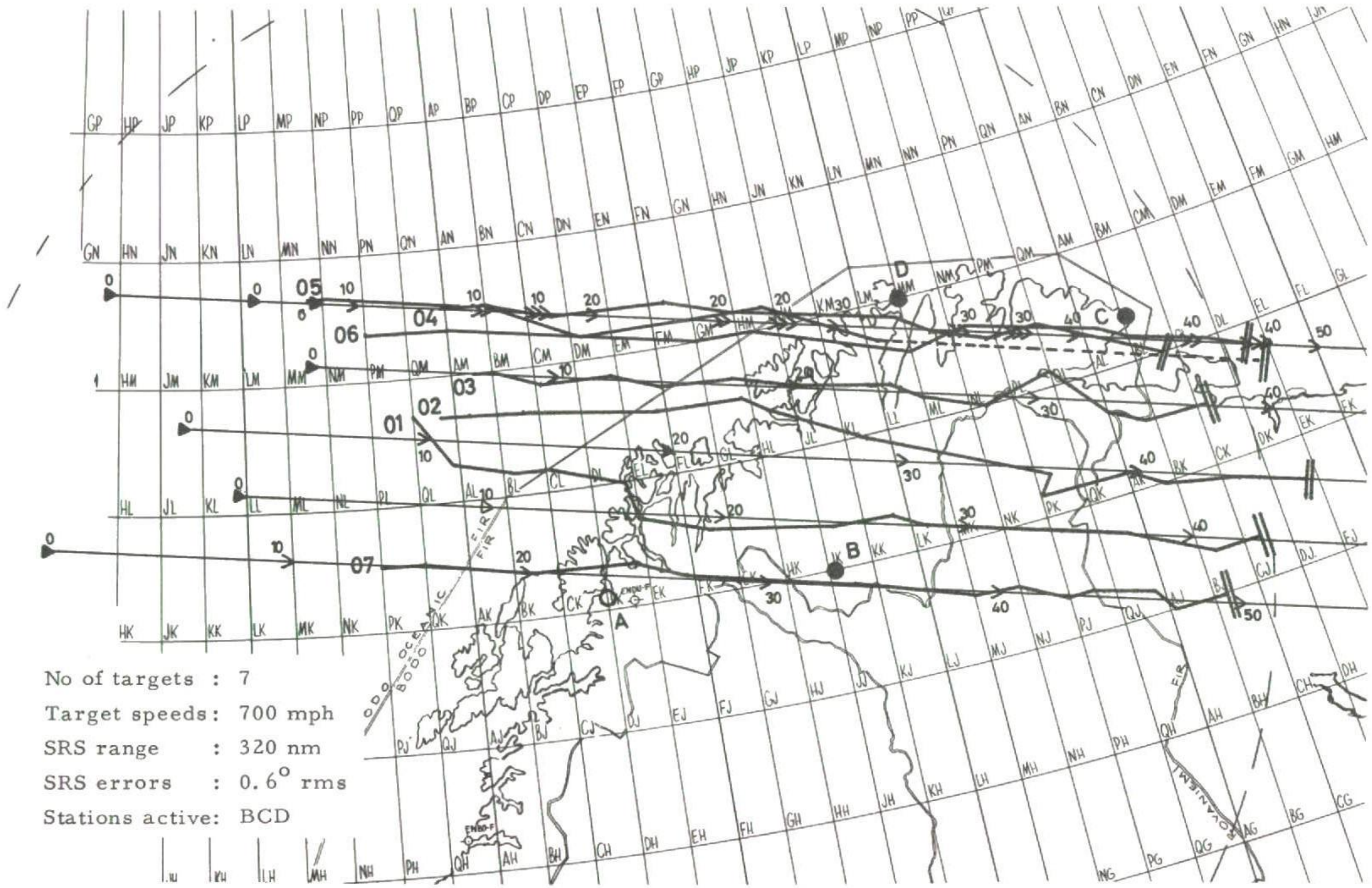

No of targets : 7
Target speeds: 700 mph
SRS range : 320 nm
SRS errors : 0.6° rms
Stations active: BCD

Figure 3.42 Tape simulated exercise

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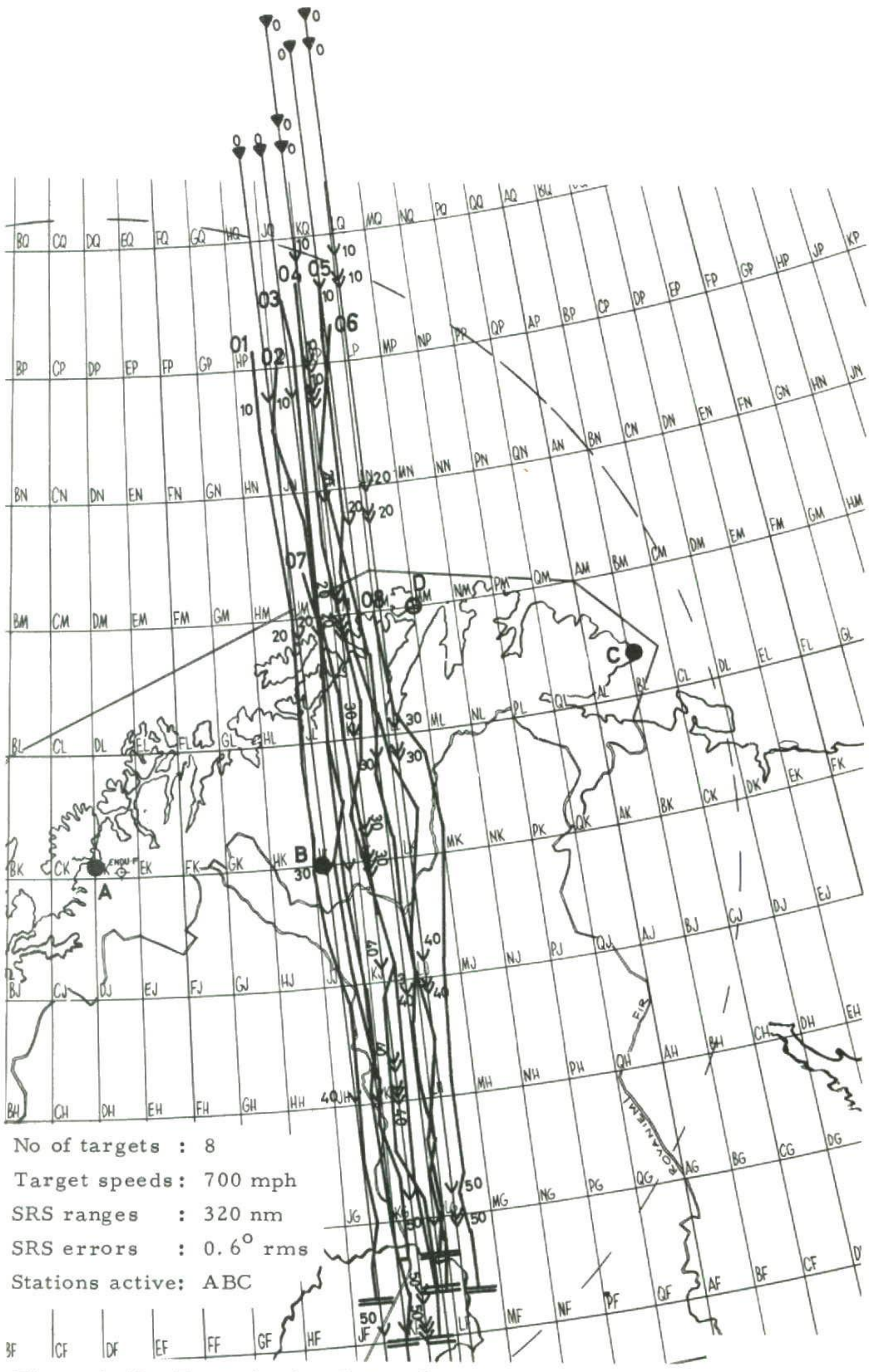
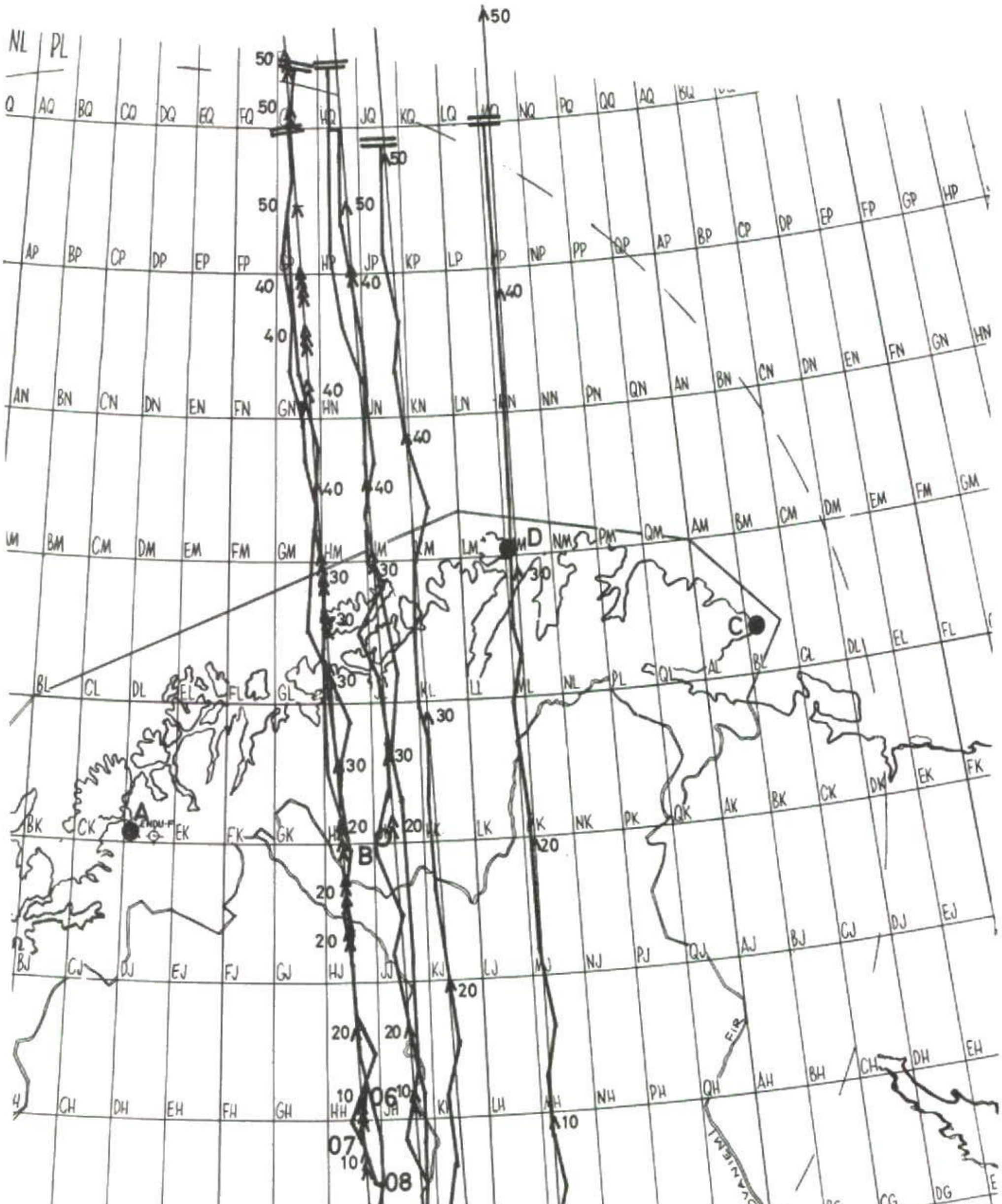


No of targets : 8
Target speeds : 700 mph
SRS ranges : 320 nm
SRS errors : 0.6° rms
Stations active: ABC

Figure 3.43 Tape simulated exercise



No of targets : 8
Target speeds : 700 mph
SRS ranges : 320 nm
SRS errors : 0.6° rms
Stations active: ACD

Figure 3.44 Tape simulated exercise

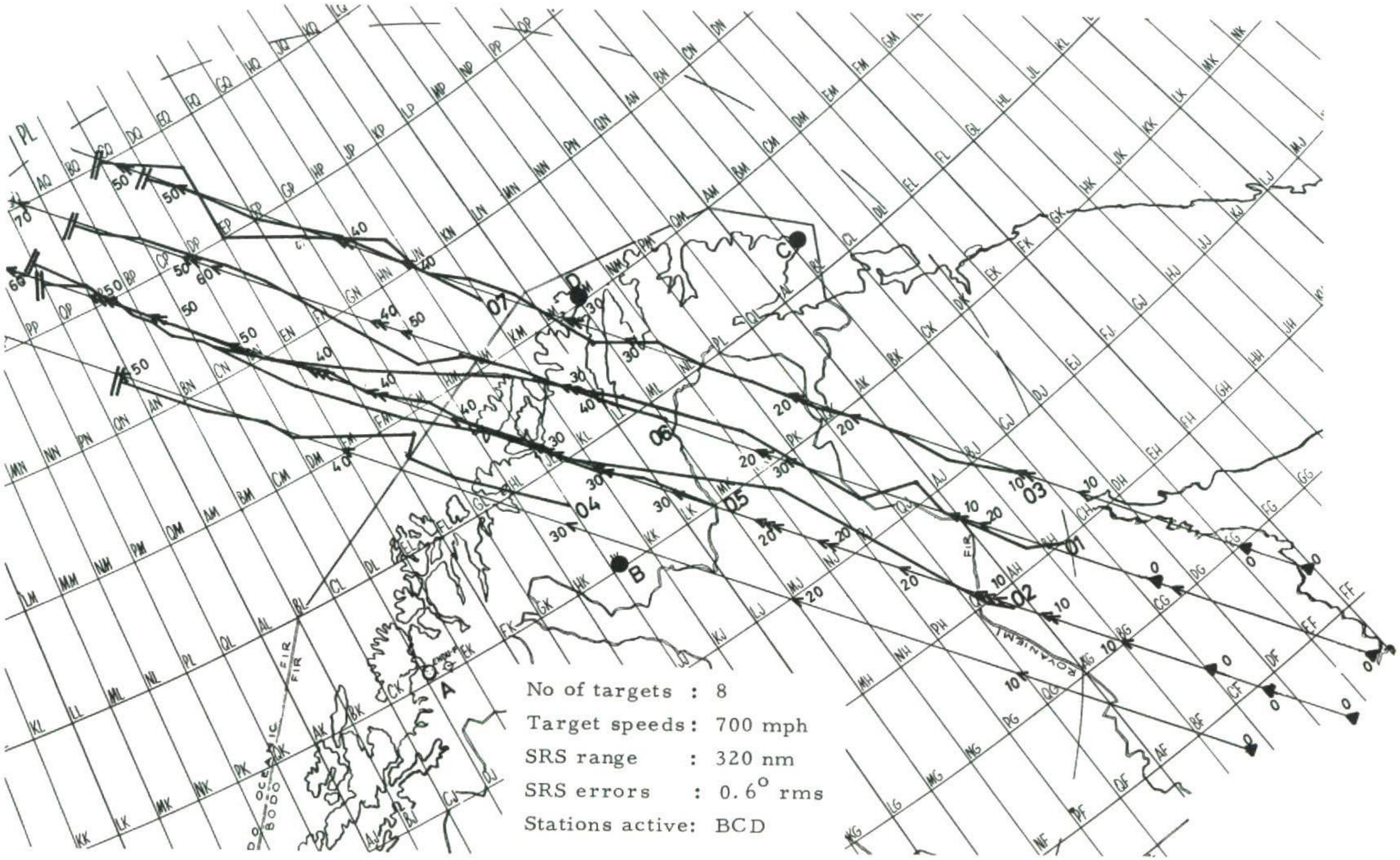


Figure 3.45 Tape simulated exercise

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In general it may be concluded that with three strobe reporting stations taking part most targets will be individually located within a few minutes for raids including up to at least 8 targets. For dense raids ghost tracking may occur even if the raid is smaller, but the ghost tracks will follow paths close to the true paths.

The raid strengths and areas have in all cases been correctly reported within a couple of minutes. (These observations are derived from the tape recorded log, but are not shown in the reproduced plots).

3.12 Equipment and installation

3.12.1 Installation

At the remote sites, the SRS equipment is installed in the operations room adjacent to an Early Warning plan position indicator. An operator can therefore by turning his chair quickly change over from active radar plotting to strobe reporting when jamming blinds his PPI, and extra SRS personnel are therefore not required. The installations have the additional advantage that as the jamming directions are determined in the operations room, the other operators can easily be directed for active radar search in the selected directions, and possible active returns in jammed sectors, whether acquired by the surveillance radar or the height finder, can be reported through the active radar data channels.

At the triangulation centre the triangulation table is conveniently located in the operations room, so that the triangulation operators may directly take advantage of supplementary data reported via the active radar data channel or other channels. They can also easily be assisted by the raid recognition officer in associating data. Due to the interconsole markings, directed search by other operators for possible active radar returns is easy. As the triangulation table is convertible from Early Warning PPI to triangulation, and triangulation will be used when the surveillance radar is partly or fully blinded, no extra personnel are required.

The SRS at the triangulation centre was for administrative reasons put in a separate cabin. This leads, however, to the requirement for extra SRS operators, and the location should therefore be reconsidered.

3.12.2 Servo system

At two sites, servo data converters have been inserted to match the SRS and the radar servo systems. For future installations it is advisable to avoid converters as they may introduce direction-finding errors, and instead use special servo data transmitters directly connected to the antenna platform.

3.12.3 Azimuth versus time recorder

An AVT recorder was incorporated in the experimental system in order that its usefulness should be considered. From the experience so far gained, the AVT recorder is of little or no importance, and may in future be omitted.

3.12.4 Recording of live exercises

In some cases, a permanent recording for later playback of live exercises is of advantage. This can be accomplished by magnetic tape recording of the audio tone signals in the teletype terminal equipment at the central station, and if the various teletype channels are properly stacked within a telephone channel bandwidth, all SRS channels can in fact be recorded on a single track tape recorder.

As the additional expenses incurred can be made small whatever solution is chosen, means for recording of live exercises should form part of future installations.

3.12.5 Cursor control by pedals

In order to permit the SRS operator to rest his right arm, pedals were installed as an additional cursor control. In practice the pedal controls are never used, as the hand-controlled wheel runs with very little friction, and no operator fatigue effects have been observed. The pedals may therefore be omitted without any operational sacrifice.

3.12.6 Miscellaneous

When the circuit development started, only germanium transistors were available in high power ratings, and their quality varied, making in certain cases a selection of individual transistors necessary. Even if all circuits have met the environmental and other tests prescribed, it is, in view of the now clear trend towards silicon power transistors advised that future systems are redesigned accordingly. This comment concerns only circuits DAF 1/12 and DAF 1/15.

For maintenance, an oscilloscope is used to check whether a given strobe message is approved or not by the central receiving equipment. As a visual indicator can easily be introduced, it is advised that such indicators form part of later equipment.

In the selection circuit DAF 4/7 it is advised that the trimming range of the origin coordinate setting potentiometers be reduced to make final adjustment less critical.

The commercial regulated power supplies used are in some cases too well protected against transients on the mains supply, and sometimes automatically cut out unnecessarily. As they are more sophisticated than required by the DAF equipment, simpler power supplies may be used to advantage for future systems.

The mechanical design of the SRS consoles and the CSR rack should be strengthened. Accessibility for replacement of blown lamps and servo components may be made easier.

3.12.7 Equipment failures

Experience as to the system reliability and maintainability is for obvious reasons still very limited. During the testing and evaluation periods a technical log has, however, been kept, and the principal failures recorded so far are:

a) A blown lamp on an SRS console had to be replaced.

b) A blown lamp in the teleprinter synchronizer had to be replaced.

c) On one occasion a servo motor stuck due to eccentric bearings, causing destruction of the power transistors in a servo amplifier.

d) An analog-to-digital disc encoder required cleaning due to periodic internal short circuits between segments.

Of the recorded failures, c and d were unexpected as the components in question did not stand up to their military specifications.

3.12.8 Conclusions

The equipment has been satisfactorily installed at all sites. At Sørreisa it is advised that the strobe reporting equipment be moved to the operations room. If this is done the entire DAF prototype installation will not require additional operators.

The circuits have met the design goals. Minor modifications are suggested to further ease maintainability and improve access for replacement of lamps and servo components of limited life expectancy.

Facilities such as azimuth versus time recorder and cursor pedal controls may be omitted without operational loss.

3.13 Summary

The DAF experimental system was installed at four sites in North Norway and connected to radar equipments of diverse nature without difficulty. On-line exercises have been carried out satisfactorily in spite of poor data channels available.

The areas of coverage as shown in Figures 3.2 - 3.3 are satisfactory for the altitudes at which airborne jamming against the active radar system is most likely.

As direct measurements have not been possible for reasons of defence security, the position accuracy as presented in Figure 3.20 has been indirectly assessed by way of studies of the basic system errors. The accuracy is satisfactory for Early Warning and limited close weapon control.

A few live exercises have been carried out employing IFF responses of non-jamming aircraft to simulate jamming strobes. By employment of triangulated data for the target positions, successful interceptions have been performed.

Numerous map exercises have been programmed on teleprinter tape and displayed at the triangulation centre with real time updating. From plots as shown in Figures 3.24 - 3.29 and Figures 3.31 - 3.45 it appears that in general the operators correctly detect and track most of the individual targets in raids including up to at least 8 targets. For dense raids some targets may be ghost tracked on paths close to the true paths. The positional inaccuracies appearing in the said plots mainly stem from the aural telling procedure so far used, and will be reduced when joystick telling facilities are available in late Summer 1964.

During all exercises adequate Early Warning reports have been given within a few minutes.

For DAF equipments installed in the main operations room no additional operators are needed, as the triangulation functions are taken over by regular radar operators when their active radar displays are fully or partly blinded by jamming.

Operator training has posed fewer problems than anticipated. The operators quickly grasp the basic principles, and are after a few exercises employing simulation by tape programs and IFF flights capable of resolving quite complex triangulation situations.

The equipment has proved to be reliable and easy to maintain. Certain modifications are suggested for further improvement. Facilities included for azimuth versus time recording of main jamming strobes and for pedal control of the strobe reporting cursor may be omitted. Means for magnetic tape recording of live exercises should be included.

It may be concluded that the design goals have been reached. The system adequately satisfies the requirements for Early Warning and gives a limited weapon control capability for areas subject to a medium airborne jamming threat.

References

(1) Endresen, K; K Lauritzen - Radius of uncertainty for a (φ,θ) navigation system, Teknisk notat T-85, Norwegian Defence Research Establishment (1962)

(2) Eggestad, M; K Endresen - Errors in triangulation of moving targets, Teknisk notat, Norwegian Defence Research Establishment (To be published)

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THE DEVELOPMENT OF PASSIVE TRACKING SYSTEM DAF

Final Project Report Mutual Weapons Development Program

Agreement No N-14-MWP-AF-62

NDRE REPORT No S8

Part II

FORSVARETS FORSKNINGSINSTITUTT
Norwegian Defence Research Establishment
PO Box 25 - Kjeller - Norway
May 1964

CONTENTS

List of Illustrations

1 SYMBOLS AND ABBREVIATIONS

1.1 Introduction

The circuitry is mainly composed of modular circuits. One or more modular circuits are assembled on one printed circuit card. Several printed circuit cards are assembled in one panel. The panels are interconnected by plug cards. Ancillary components are connected to the main cabling either directly, or by plugs or plug cards. External wires are connected by plugs or plints. The various terms and the symbols used are discussed below.

Some of the circuit modules are used only a few times in the main circuits and are described in their proper context.

Frequently used modules are described in Chapter 2.

Detailed printed circuit card diagrams are given in Chapter 5.

1.2 Circuit module designation

Circuit modules are designated by one to three letters followed by a number. The letters indicate the circuit function while the number refers to the particular circuit type. Example: EF3 identifies an emitter follower of type 3.

The symbols used are listed in Table 1.1.

AA	analog amplifier	MD	modulator
CD	core driver	MO	master oscillator
CG	clock generator	MV	multivibrator
CO	counter stage	PA	pulse amplifier
DA	digital-to-analog converter	PG	pulse generator
DL	diode logic	PH	phase shifter
DS	desensitizer	RA	read amplifier
EF	emitter follower	REL	relay circuit
FI	filter	SA	servo amplifier
FM	ferrite matrix	SH	shift register
G	gate	SI	simulator
I	indicator	SR	set/reset circuit
IN	integrator	ST	Schmitt trigger
IV	inverter	SY	synchronizer
LI	limiter		

Table 1.1 Circuit module designations

1.3 Printed circuit cards

One or more modules are assembled on printed circuit cards. Each card has a plug, the pins being numbered from 2 to 35 (making 34 pins). A card pin is in the text denoted by "j" followed by the number, e g "j21". For lack of space the "j" is omitted in the block diagrams. Each card contains several test points, designated "TP" followed by a number indicating the test point number counting downwards from the top of the card, e g "TP3". A card may also contain trimming potentiometers accessible from the end. These are designated by "p" followed by a number indicating its position starting from the card top. The test points are coloured in accordance with Table 1.2.

-12 volts	- Blue	Emitter	- Orange
+ 6 volts	- Red	Collectors	- Yellow
0 volts	- Black	Signals	- Other colours
Other voltages	- Violet		

Table 1.2 Test point colour scheme

1.4 Card panels and plug card

Several cards are assembled in 19" panels. Each panel is connected to the main cabling by means of one or more printed plug cards.

The plugs are denoted by a single letter, e g "I", and each pin is designated by the plug letter followed by the pin number, e g "I. 21".

Each panel is designated by the letters of its card plugs, e g "panel IJ".

A card position within a panel is identified by a number, indicating its position counting from left to right.

1.5 External plugs and ancillary components

Table 1.3 lists the abbreviations commonly used for designating external components. The designating letter is usually followed by a serial number, which may be further followed by a contact designation. Example: "P3.a" identifies contact "a" of ancillary potentiometer No 3.

A	- amperemeter	PS	- power supply
F	- fuze	R	- resistor
I	- indicator lamp	RS	- resolver
M	- motor	SW	- switch
P	- potentiometer	T	- transformer
P+letter	- plug		

Table 1.3 Ancillary components

1.6 Block diagrams

A typical detail of a block diagram is shown in Figure 1.1, and will as an example be described in some detail.

PH1, LI1 and MD1 are respectively phase shifter, limiter and modulator modules, and are all contained in panel IJ. The number above the module designation identifies the card on which the module is located (PH1 on card No 3 from the left, LI1 and MO1 both on card No 5 from the left).

Module PH1 is fitted with a trimming potentiometer p5, i e the fifth potentiometer from the top of card No 3.

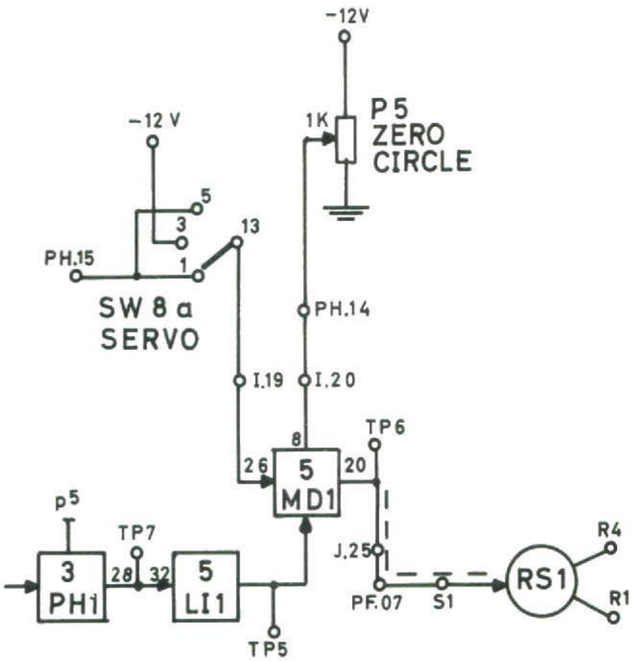


Figure 1.1 Example of block diagram

Card pin j3.28 is connected to card pin j5.32. The signal is available on test point TP3.07 (the seventh test point from the top of card No 3). The output of LI1 is fed to an input of MD1, and as both modules are on the same card, the connection is made internally. The signal may be tested on TP5.05.

MD1 receives on input j5.26 a signal from switch segment SW8a terminal 13. The signal is fed to panel IJ via card plug contact I.19. The switch bears the designation SERVO.

Another signal is taken from external potentiometer P5 (designated ZERO CIRCLE). The connection is taken via plug contact PH.14 and panel card plug contact I.20 to input j5.08.

The MD1 output j5.20 (test point TP5.06) is fed by a screened wire via panel card plug contact J.25 and plug contact PF.07 to input terminal S1 of a resolver RS1.

1.7 Component designation

In the circuit diagrams, the unit designations Ω, F and H are omitted as they will be evident from the context.

The power rating of a resistor is 1/4 W unless otherwise stated.

2 FREQUENTLY USED MODULAR CIRCUITS

2.1 Emitter followers EF

An emitter follower provides a high input resistance. The voltage gain is near unity, and the output is in phase with the input.

Figure 2.1 shows the various modules used. For EF1 and EF2 - EF5 the preceding module contains the necessary input leak resistance. EF1A replaces EF1 where the preceding stage does not include the base leak.

EF2 is used where the following stage provides the required emitter load.

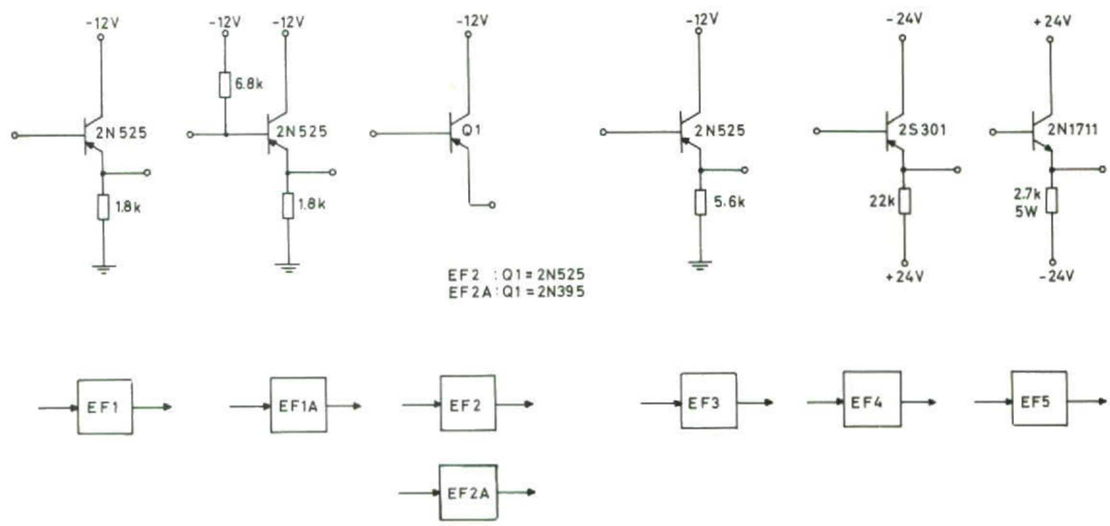


Figure 2.1 Emitter follower EF

2.2 Inverters IV

An inverter provides a medium high input resistance. The voltage gain is above unity, and the output polarity is reversed with respect to the input signal. Figure 2.2 shows the circuit used.

All circuits are designed to deliver a negative output (equal to the collector supply voltage through the collector resistance) when the input is near 0 volts, and zero output (earth through the saturated transistor) when the input is sufficiently negative.

The input circuits of IV1, IV1B, IV3, IV3A, IV3B and IV8 contain speed-up capacitors, whereas IV6 has a slow-down capacitor.

IV1C, IV4 and IV5 receive their collector supply voltages from the following stages.

2.3 Integrators IN

As integrating elements are used simple RC networks as shown in Figure 2.3. IN3 also includes a voltage divider.

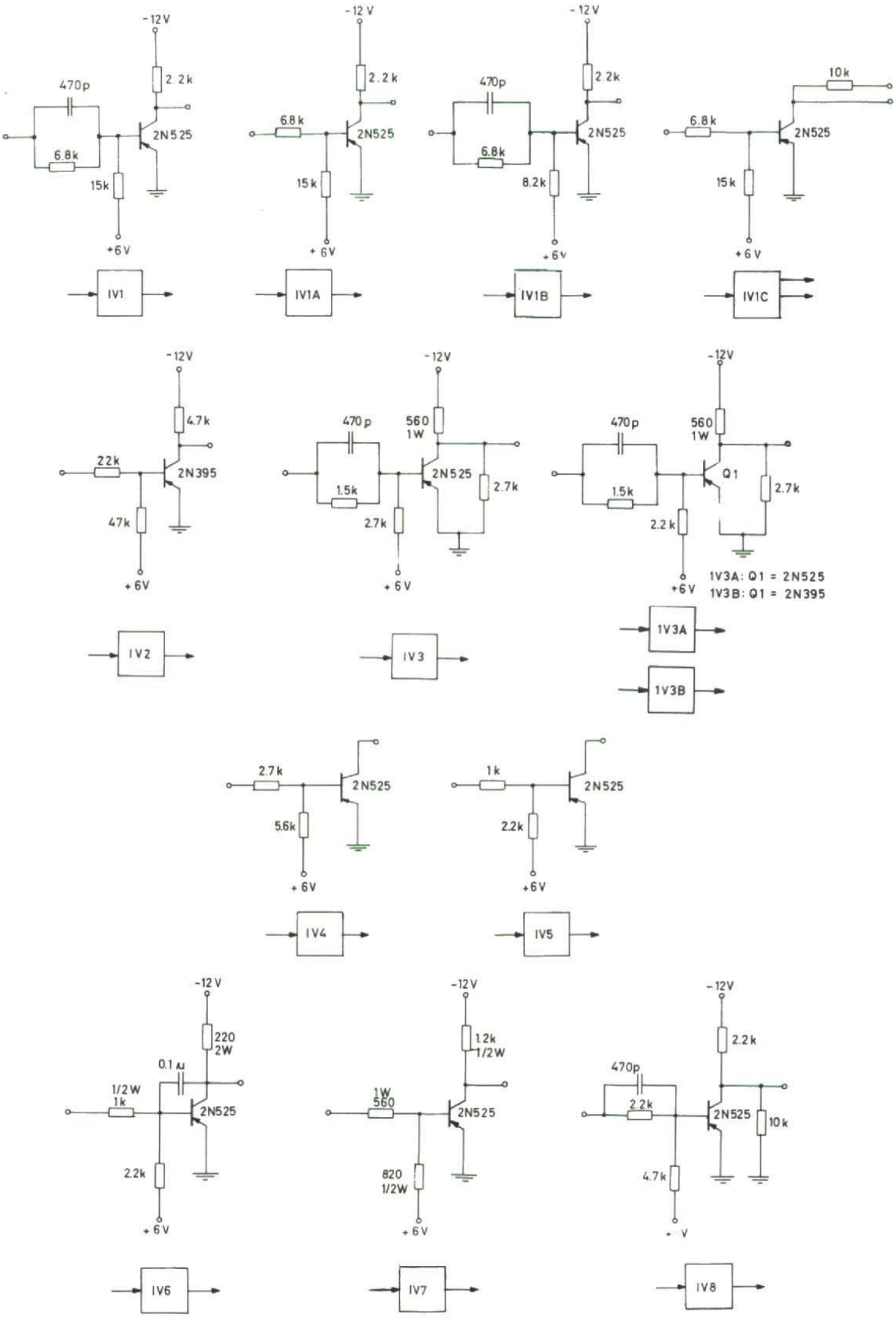


Figure 2.2 Inverters IV

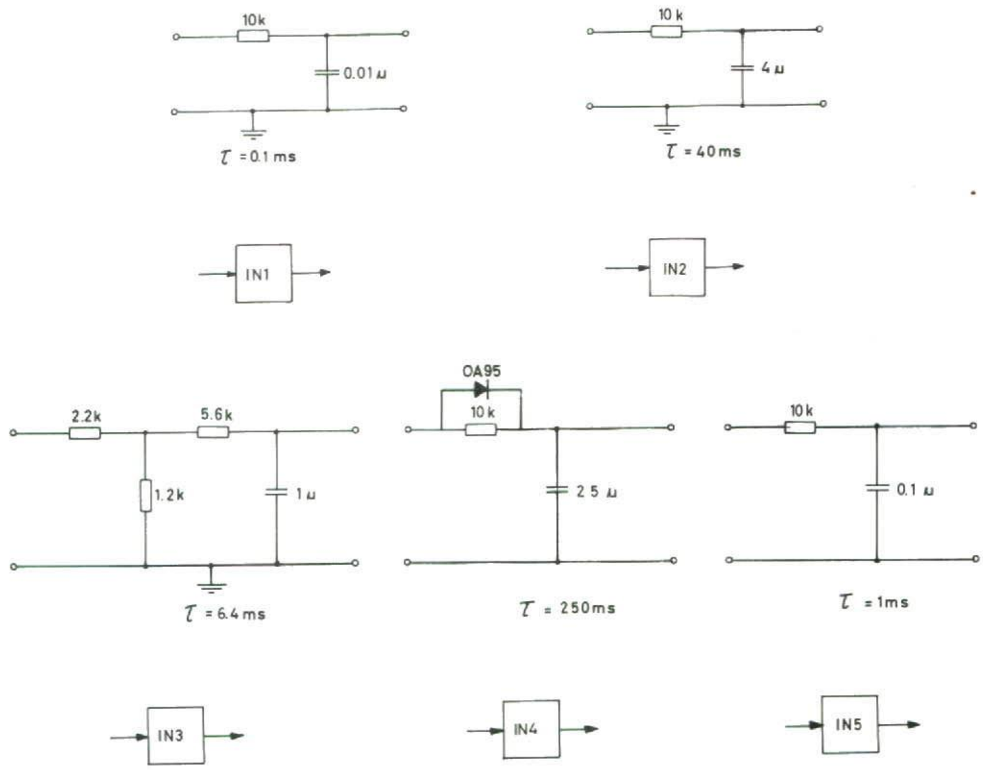


Figure 2.3 Integrators IN

2.4 Diode logics DL

The logic circuits used are all simple resistor-diode logics as shown in Figure 2.4.

DL1, DL1A and DL2 will give a zero output if one or more of the input voltages is zero, and a negative output if all inputs are negative. They are therefore OR-gates for positive inputs, or AND-gates for negative inputs.

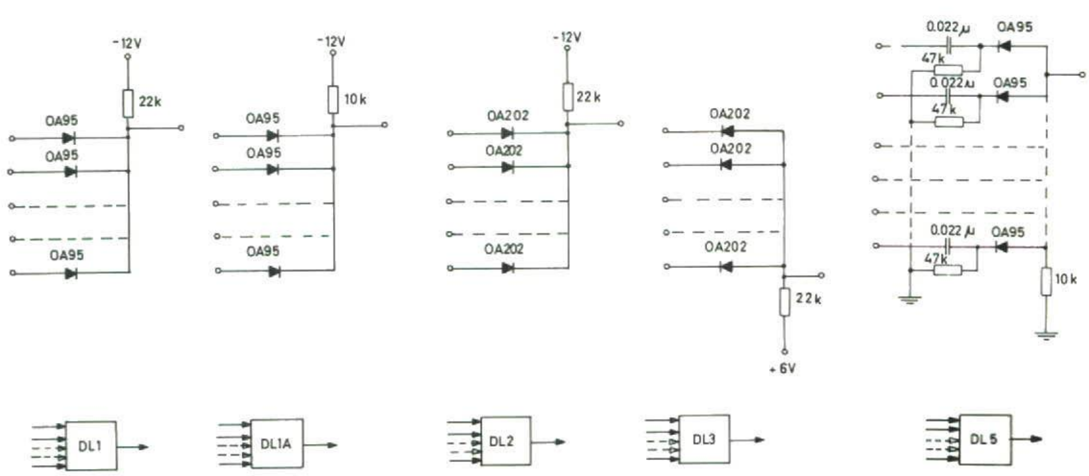


Figure 2.4 Diode logics DL

DL3 has a positive output if all inputs are positive, and a negative output if at least one input is negative. It is therefore an AND-gate for positive inputs, or an OR-gate for negative inputs.

DL5 is an OR-gate for negative pulses. DL4 (not shown in Figure 2.4) is a special purpose logic which is described in Section 4.3.5.

2.5 Gates G

Figure 2.5 shows the gates used. Gates G1, G3, G4 and G6 are basically inverter stages. In G3 and G6 the collector voltage supply is taken from the following stage. In each gate, b' may be the signal input terminal and e the control terminal, or vice versa. If e is used as the control terminal, the gate is open when e is zero, and the output at c is inverted with respect to the input at b'. The gate is closed when e is negative, the output becoming negative. If b' is the control terminal, the gate is open when b' is negative, and the output at c is uninverted with respect to the signal input at e. The gate is closed when b' is zero, and the output becomes negative.

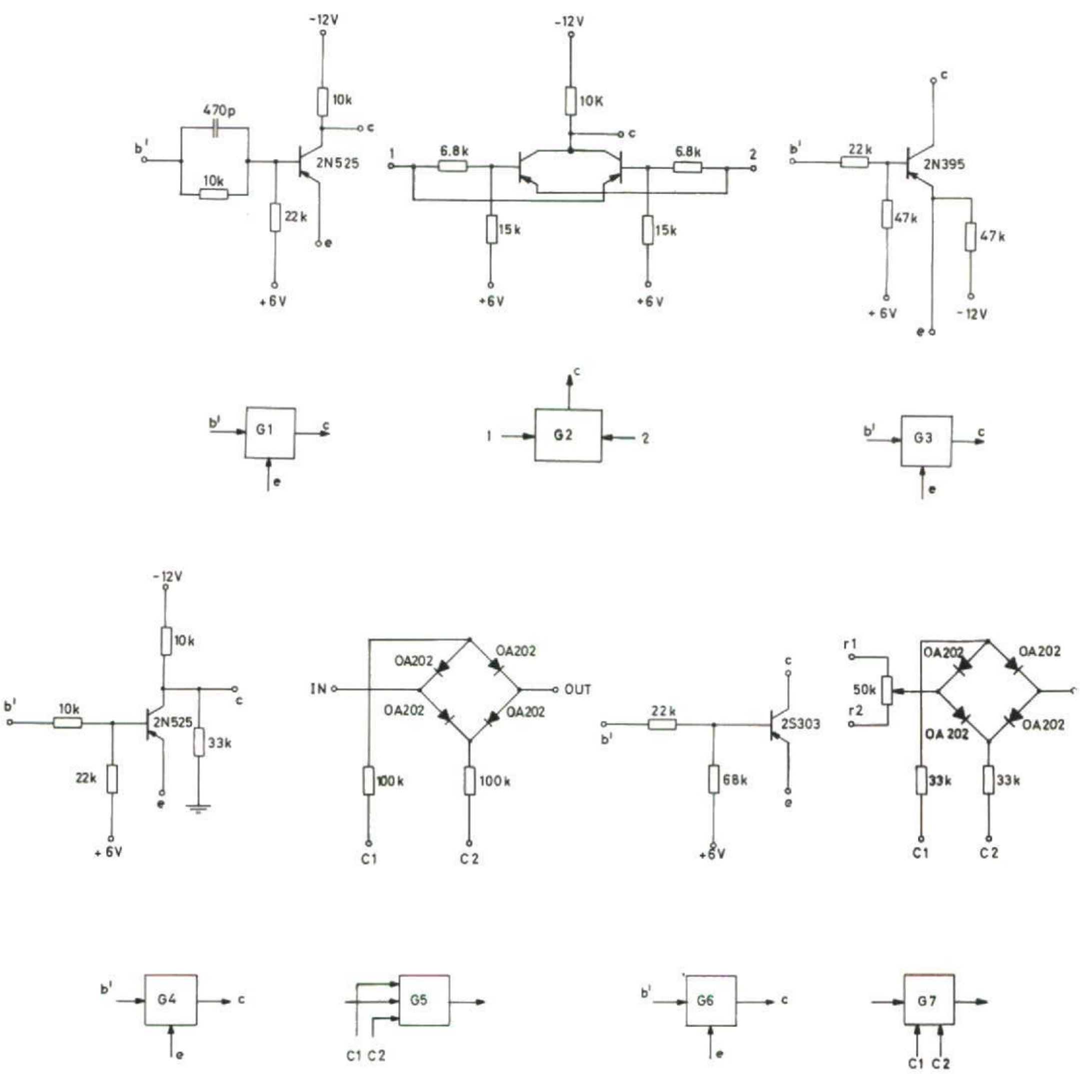


Figure 2.5 Gates G

Gate G2 is a coincidence gate. The output c is negative if inputs are either both zero or both negative. The output is zero if one input is zero and one is negative.

Gate G5 is used for analog signals having a DC bias of about -6 V. The gate is open for C1 = 0 V, C2 = -12 V, the output being equal to the input. When the C1 and C2 voltages are reversed the gate is closed. Gate G7 is used for gating the DC voltage from the sliding contact of a potentiometer connected between two reference voltages.

2.6 Set/reset circuits SR

A set/reset circuit has two controllable stable states. Figure 2.6 shows the circuits used.

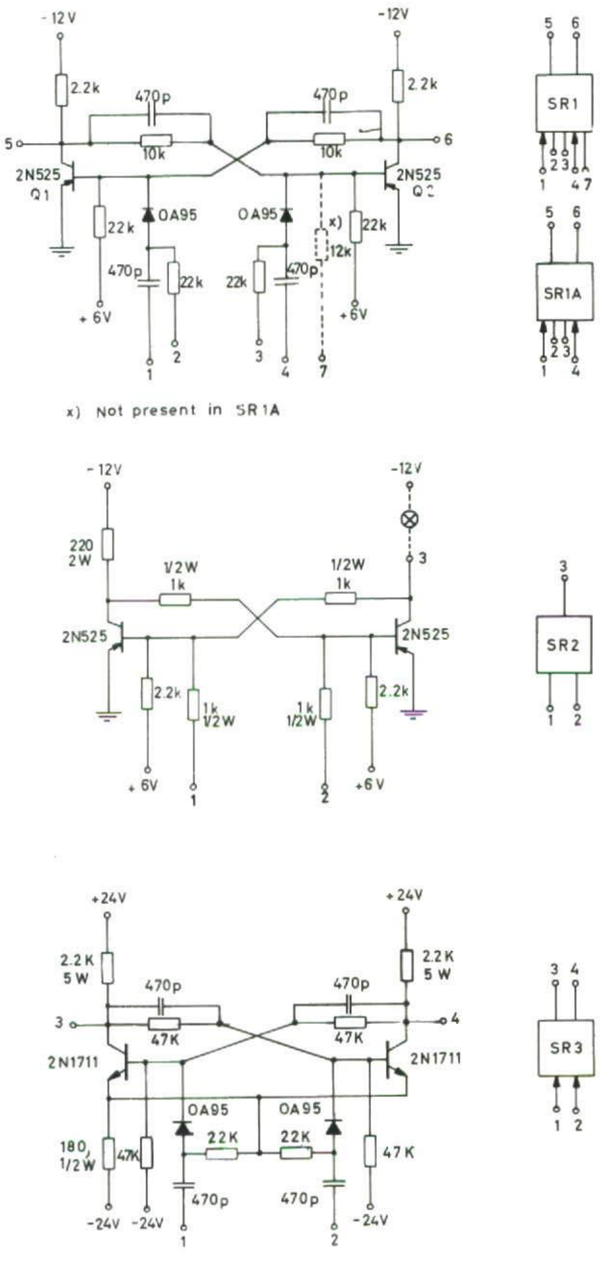


Figure 2.6 Set/reset circuits SR

In SR1, if inputs 2, 3 and 7 are earthed V5 becomes negative, and V6 becomes zero if a positive pulse is applied to input 1. A positive pulse to input 4 renders V5 zero and V6 negative. If input 2 is connected to a negative supply input 1 is inhibited. Likewise, connection of input 3 to a negative supply renders input 4 inoperative. If input 7 is connected to a negative supply, V5 is negative and V6 zero irrespective of control pulses on inputs 1 and 4.

SR1A lacks input 7, but is otherwise identical to SR1.

In the block diagrams, inputs which are permanently earthed are not indicated.

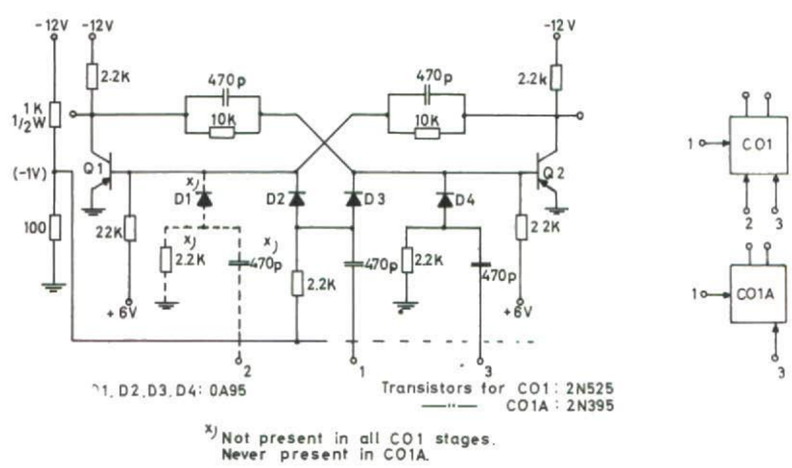
SR2 is used for the control of an external indicator lamp. Under quiescent conditions inputs 1 and 2 are floating. The lamp is lit if a negative pulse is applied to input 2, and is turned off if a negative pulse is applied to input 1.

SR3 operates in a similar manner to SR1. It operates between +24 V and -24 V, and has an output which is symmetric about zero.

2.7 Counter stages CO

The counting circuits used are shown in Figure 2.7.

In CO1, transistor Q1 becomes cut-off giving a negative output and Q2 becomes saturated giving zero output when a positive set pulse is applied to input 2. A positive set pulse to input 3 saturates Q1 and cuts off Q2. With respect to inputs 2 and 3, the circuit is therefore a set/reset circuit. When positive pulses are applied to input 1, the circuit acts as a scale-of-two counter, alternating between states.



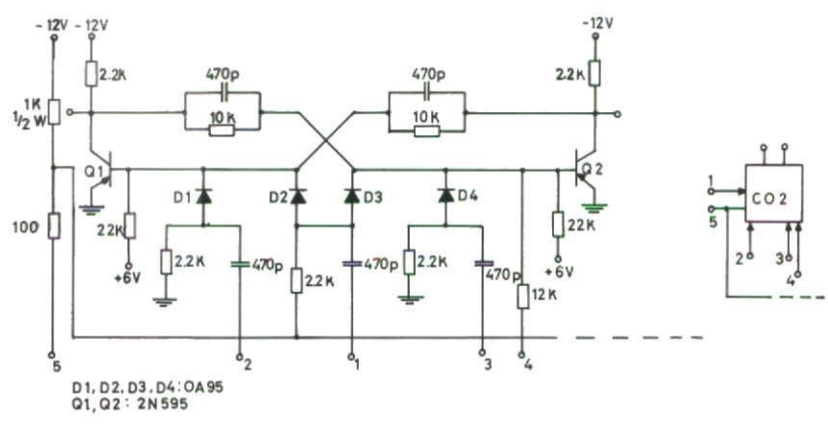


Figure 2.7 Counter stages CO

CO1A is similar to CO1, but has a faster response due to the transistor types used.

In CO2 the counting pulses may be inhibited by a negative voltage on input 5. The state of the circuit may be controlled by a DC signal applied to input 4. In all other respects the circuit is identical to CO1.

2.8 Shift register SH

A shift register consists in principle of a series connection of set/reset circuits in such a manner that a trigger pulse applied to all stages transfers the state of any stage to the following stage.

Figure 2.8 shows two stages SH1 of a shift register. The state of each stage is initially set by control voltages (inputs 3 and 11) and positive trigger pulses (inputs 2 and 10). If the control voltage for a stage is zero, the trigger pulse makes the right hand transistor cut-off and the left hand transistor saturated. If the control voltage is negative, the state depends on the past history.

Assume both stages to be in identical states, e g V6 = V8 = 0 V, V7 = V9 = -12 V. Diode D3 is therefore biased off. A subsequent positive shift pulse on common terminal 1 is allowed through D4, but causes no effect since Q4 is already cut-off. Similarly, no change would take place in the second stage if V6 = V8 = -12 V and V7 = V9 = 0 V.

If the stages are in opposite states, e g V6 = V9 = 0 V, V7 = V8 = -12 V, a shift trigger is blocked by D3 but passed by D4, changing the state of stage 2. Similarly, if V6 = V9 = -12V and V7 = V8 = 0V, diode D4 is biased off and the shift pulse through D3 causes a change of state of stage 2.

It is thus seen that each stage will assume the state of the previous stage when a shift pulse is received.

The terminals 4 and 5 of the first stage of a shift register chain will usually be connected to earth and -12 V respectively. After the first trigger pulse, Q1 will therefore become cut off and Q2 saturated. This state will be assumed by all stages when the number of applied shift pulses becomes equal to or greater than the number of stages.

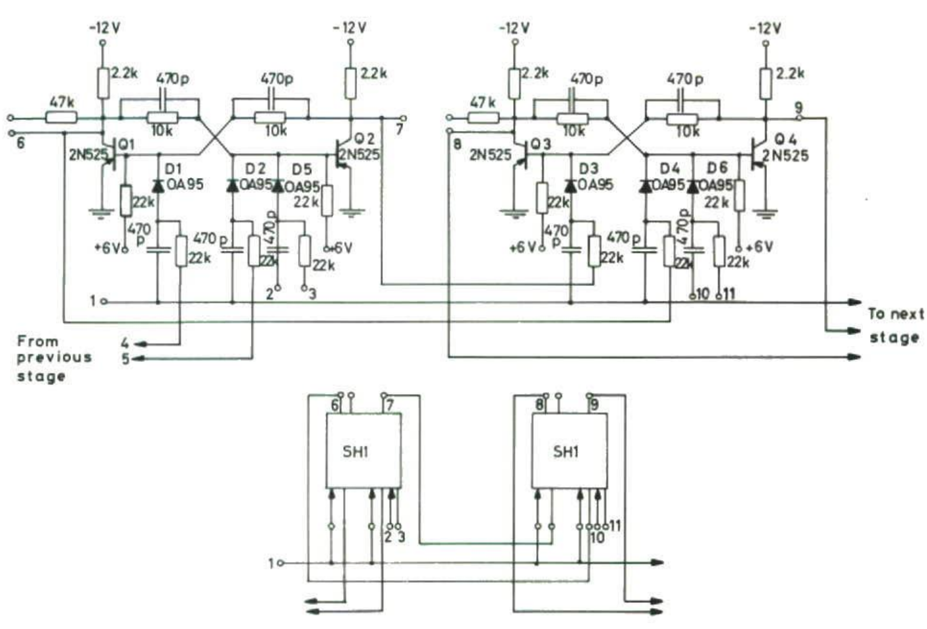


Figure 2.8 Shift register stages SH

2.9 Schmitt trigger ST

A Schmitt trigger circuit has two stable states. The state assumed depends upon an input voltage level. The change between states is cumulative.

Figure 2.9 shows the circuit ST1 used. Q2 is either cut off or saturated, dependent upon whether the input voltage is negative or positive with respect to the change-over voltage which is approximately -2 V.

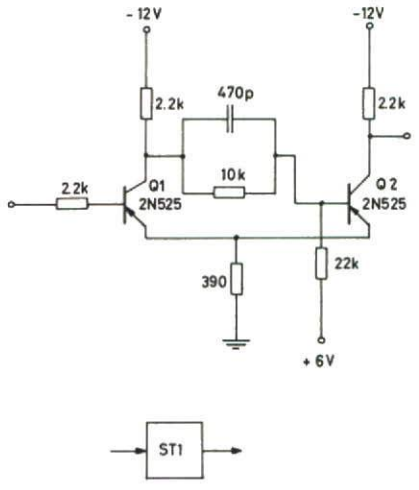


Figure 2.9 Schmitt trigger circuit ST

2.10 Relay circuits REL

Figure 2.10 shows the relay circuits which connect the DAF system to the external data channels.

REL1 is for data transmission. Transistors Q1-Q2 operate in push-pull. For a zero volt input signal (MARK), relay contacts A and T are connected. For a negative input (SPACE), A makes contact with Z.

REL2 is for data reception. For an input current direction as shown by the arrows (MARK), relay contacts A and T are connected, giving zero output. For the opposite current direction, the output is negative.

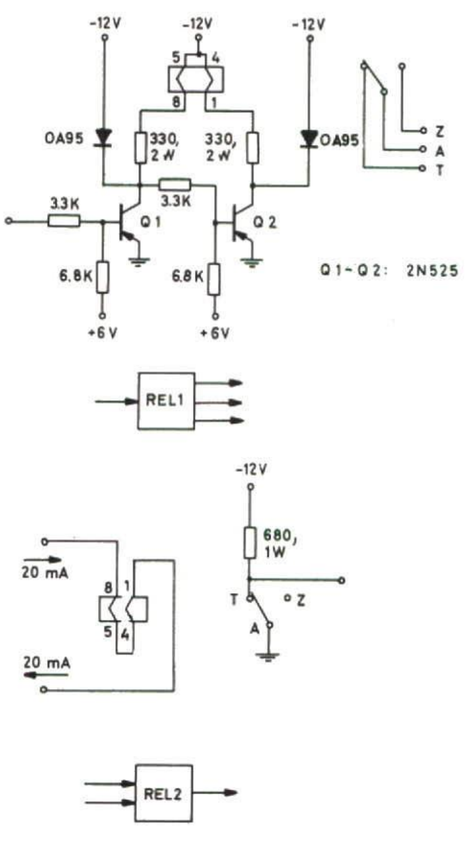


Figure 2.10 Relay circuits REL

2.11 Indicator circuit I

In Figure 2.11 the column of indicator tube DM160 will be lit if the grid voltage is zero. The column is extinguished for a grid voltage more negative than -3 V.

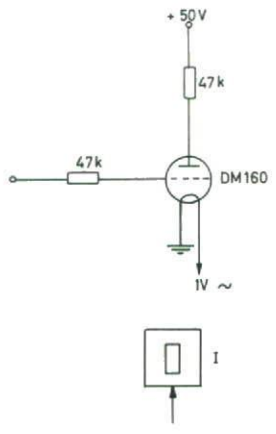


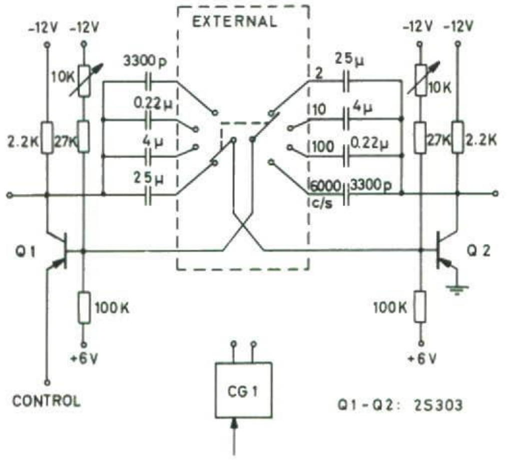
Figure 2.11 Indicator circuit I

2.12 Clock generators CG

The clock generators shown in Figure 2.12 are controlled astable multivibrators.

CG1 delivers square waves of duty cycle 0.5 when the control terminal is grounded. With the control terminal negative, the Q1-Q2 collector voltages are negative and zero respectively. The frequency may be selected as 2, 10, 100 or 6000 c/s by external connections.

CG2 may be gated in a similar manner. The duty cycle is approximately 0.45, due to the unsymmetric base resistors used. The frequency is approximately 80 kc/s.



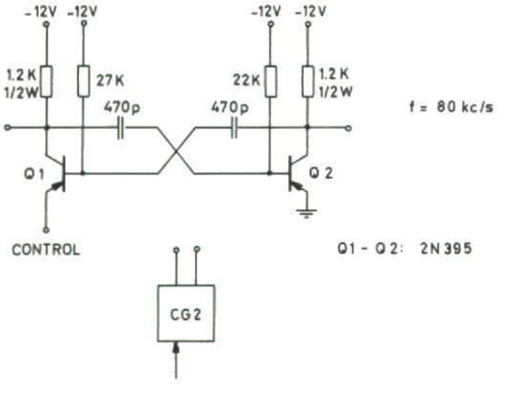


Figure 2.12 Clock generators CG

3 STROBE REPORTING STATION SRS-1, DETAILED DESCRIPTION

The main principles of the strobe reporting station have been outlined in Part I Section 2.2 and will not be repeated here.

It will also be assumed that the reader is fully familiar with Part II, Chapters 1-2.

For the location of the various circuits and controls, reference is made to Figures 3.101 - 3.105 at the end of this chapter.

3.1 Direction finding receiver

In the direction finding receiver chain shown in Figure 3.1, the pulse generator is mounted on card No 6 of panel IJ. The other blocks are contained in the display drawer.

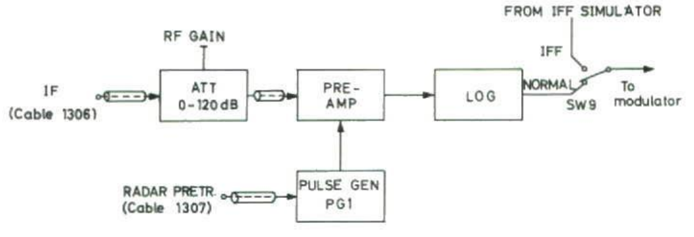


Figure 3.1 Direction finding receiver, block diagram

The attenuator is of commercial type (Hewlett Packard type 355B). It has a range 0 - 120 dB in 10 dB steps and its control shaft is available on the front of the display drawer. The input is fed on external cable 1306 from the output of the first IF amplifier of the main radar receiver.

3.1.1 Preamplifier

Photographs of a preamplifier are given in Figure 3.2

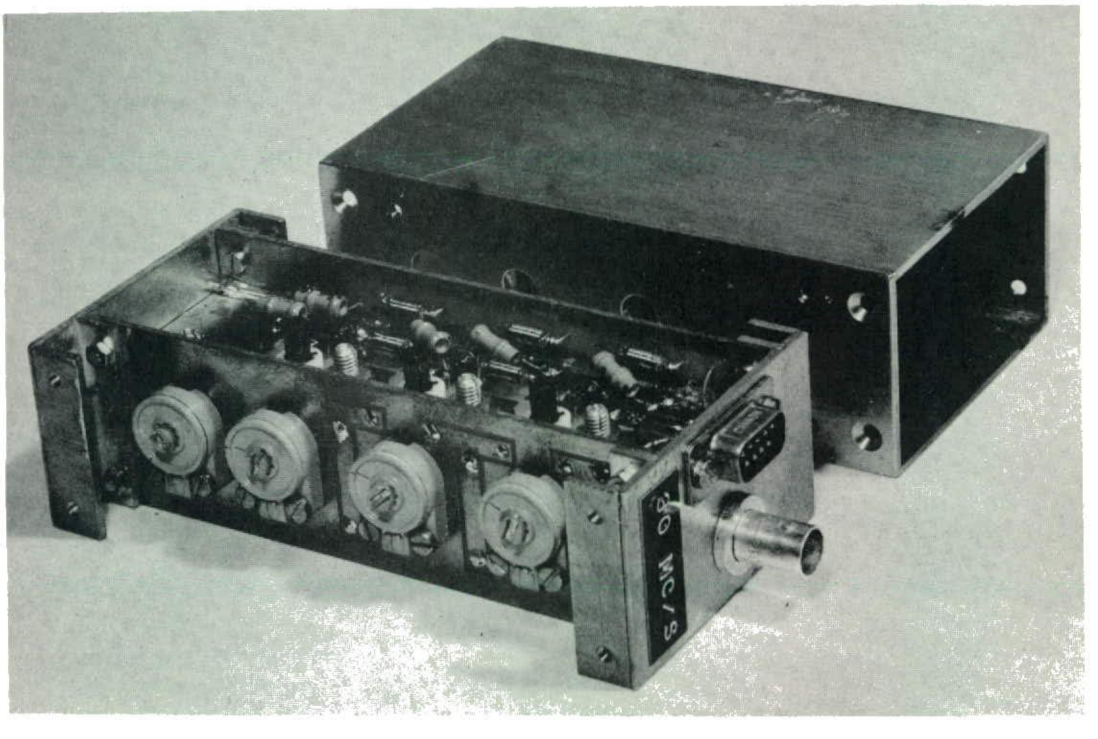
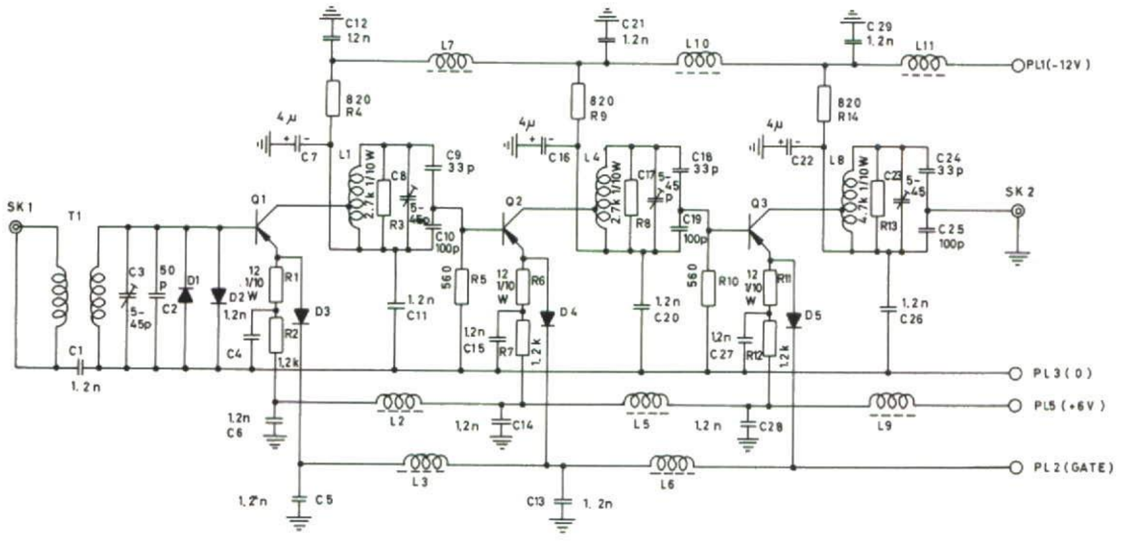


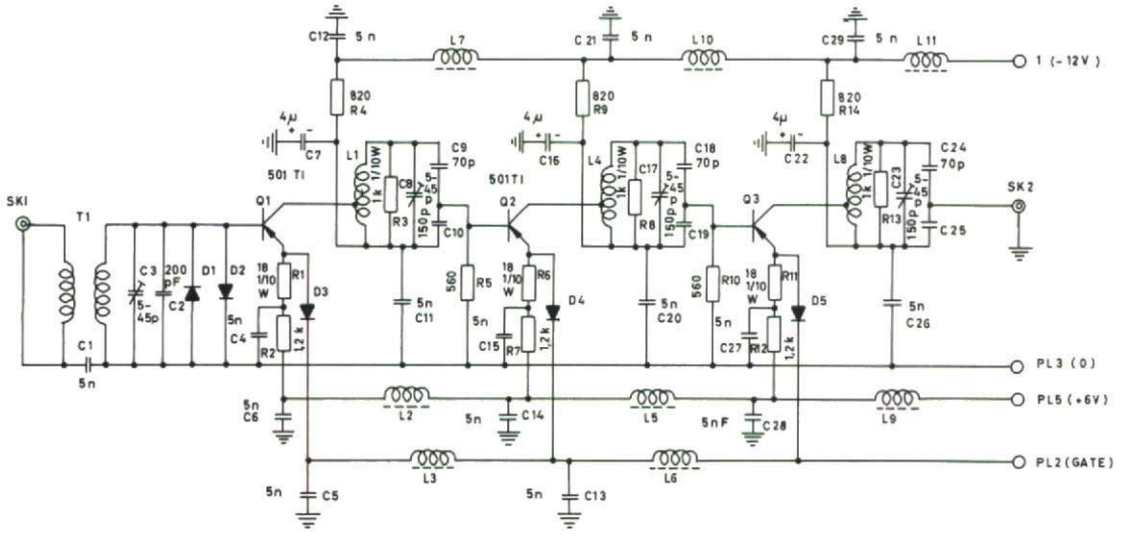
Figure 3.2 Preamplifier type DAF 1

Some radar stations employ an IF frequency of 30 Mc/s while others use 13.5 Mc/s. Figures 3.3 and 3.4 show the corresponding circuit diagrams.



D1 - D2 : 1N252
D3 - D5 : 0A202
Q1 - Q3 : 501T1
All resistors 1/4 W unless otherwise stated

Figure 3.3 Preamplifier DAF 1A (30 Mc/s), circuit diagram



D1 - D2 : 1N252
D3 - D5 : 0A202
Q1 - Q3 : 501T1
All resistors 1/4 W unless otherwise stated

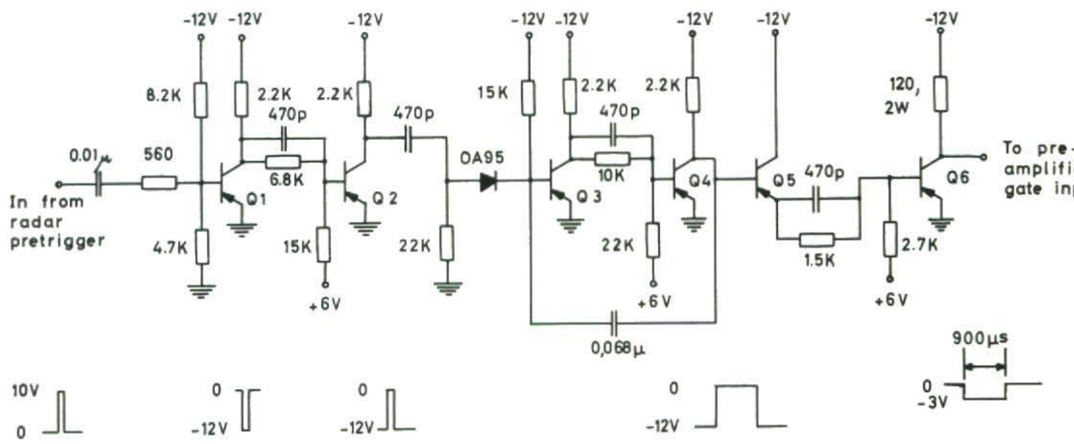
Figure 3.4 Preamplifier DAF 1B (13.5 Mc/s), circuit diagram

The input terminal SK1 is DC isolated from system ground. Diodes D1-D2 are present to protect the input circuit in case of excessive input drive from the preceding valve amplifier.

3.1.2 Pulse generator

The preamplifiers are gated off during the initial part of each radar sweep. The pulse generator PG1 is shown in Figure 3.5.

The saturated transistor Q1 is cut off by the radar trigger pulse. The negative pulse is inverted in the following stage, and thereafter triggers the monostable multivibrator Q3-Q4. A positive pulse of approximately 900 μs duration is generated.



Q1 - Q6 : 2N525

Figure 3.5 Pulse generator PG1

After amplification and inversion, the output pulse is fed to the preamplifier gate input (Figure 3.3 or 3.4) where the transistors Q1-Q3 are cut off for the duration of the negative gate pulse. The preamplifier is thus rendered insensitive to radar ground clutter from areas closer than some 75 nm.

3.1.3 Logarithmic amplifier

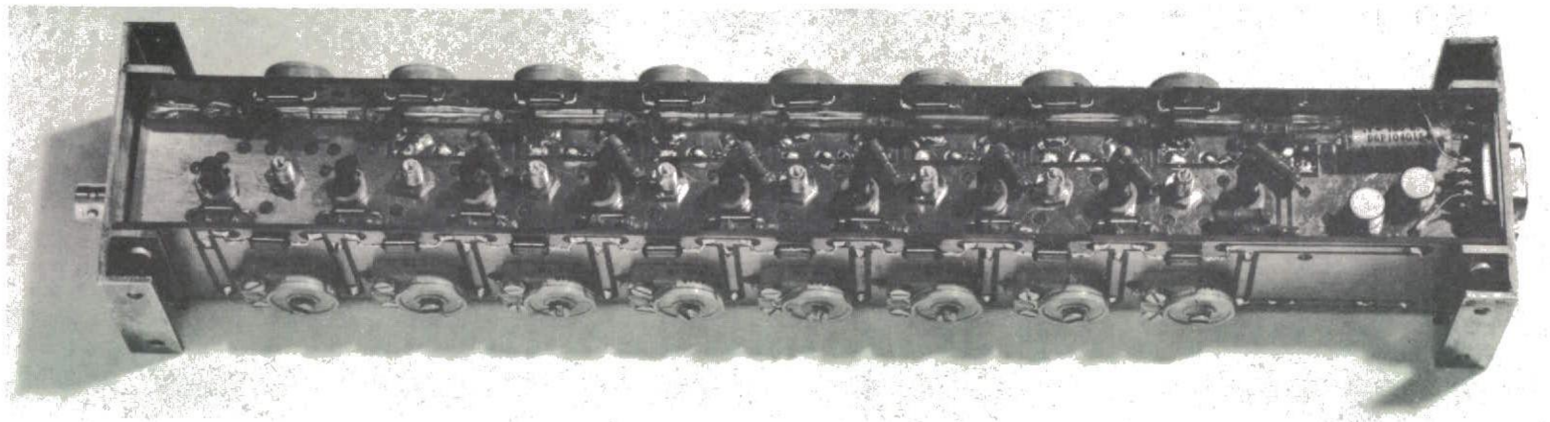
The output of the preamplifier is fed to the input of the logarithmic detector shown in Figure 3.6. As two different IF frequencies are used, two versions of the logarithmic detector are employed.

The circuit diagram is given in Figure 3.7, and component values are listed in Table 3.1.

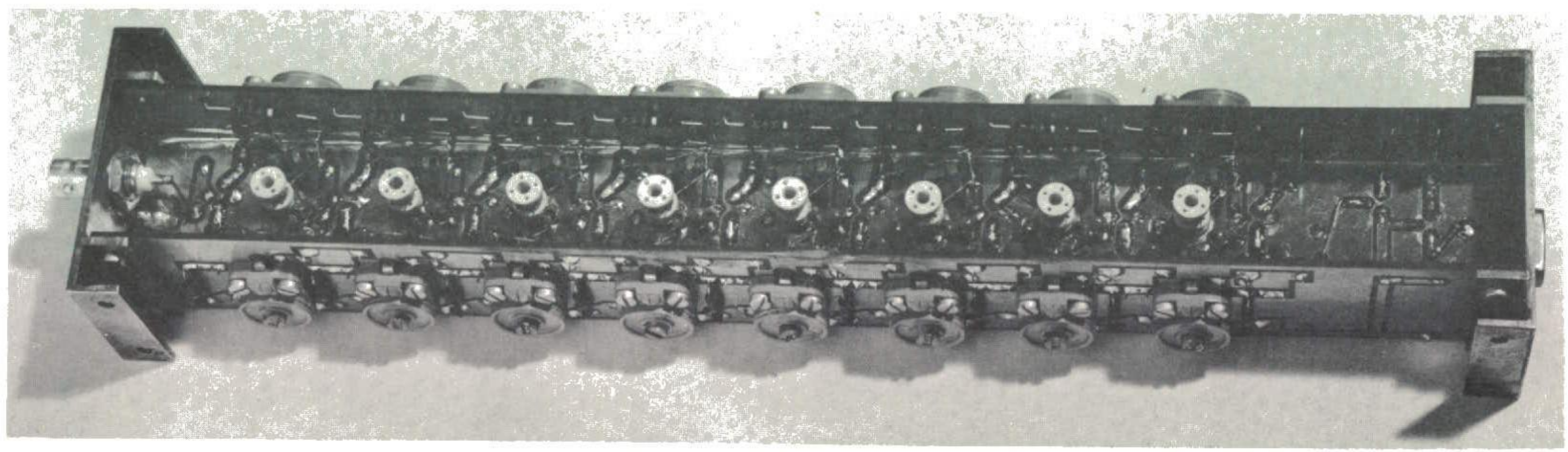
The amplifier consists of an input IF stage Q1 followed by eight identical IF amplifying stages Q2-Q9. The base signals of transistors Q2-Q9 are rectified by diodes D1-D8 and the rectified outputs are added in an RLC series connected chain (R30-R37, L18-L24, C37-C44). This results in an output DC signal which is closely proportional to the logarithm of the incoming IF signal voltage.

The output is integrated by the R29, C85 combination, giving a time constant of about 10 ms. The signal is then amplified by the DC amplifying stages Q10-Q11.

The output voltage is approximately zero for a zero IF input voltage, and -10 V for a fully saturating IF input.



Top view



Bottom view

Figure 3.6 Logarithmic detector type DAF 2 A/B

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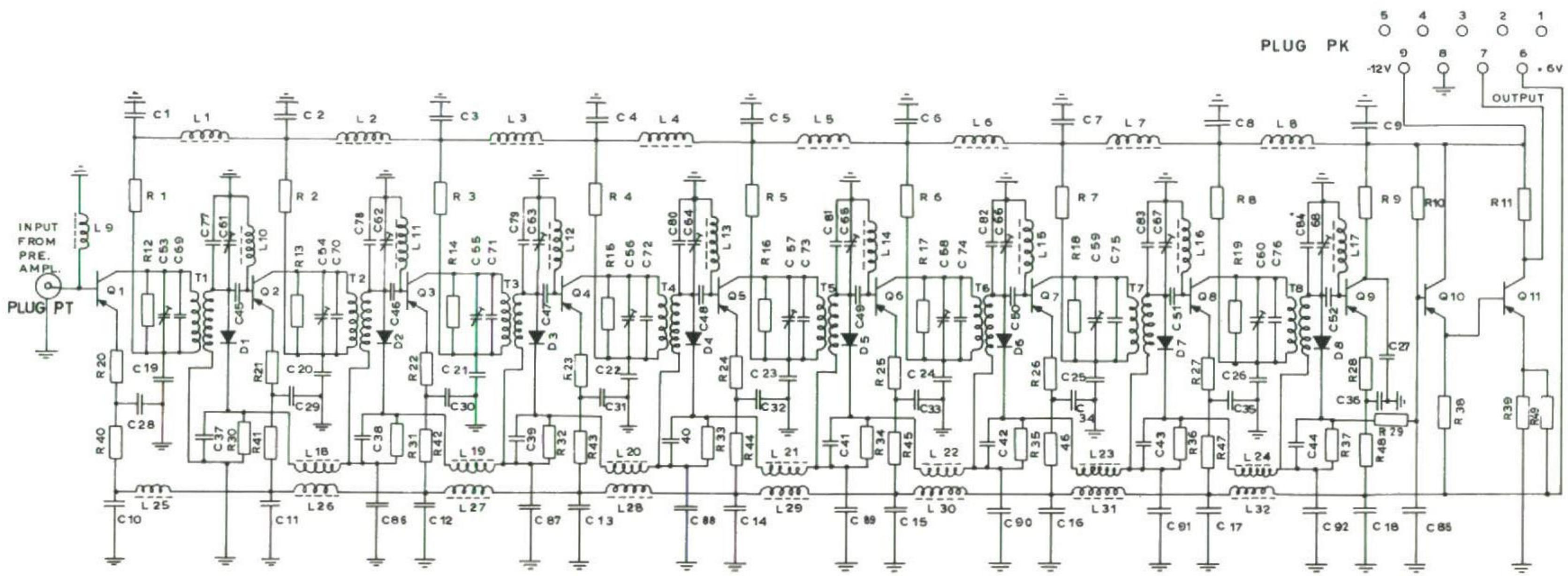

Figure 3.7 Logarithmic detector DAF 2 A/B, circuit diagram

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Component designation	Component value	
	DAF 2A (30 Mc/s)	DAF 2B (13.5 Mc/s)
Q_1 -Q_9	501T1	501T1
Q_{10}-Q_{11}	2S303	2S303
R_1 -R_9	1.5 kohm	1.5 kohm
R_{10}	150 "	120 "
R_{11}	5.6 "	5.6 "
R_{12}-R_{19}	220 ohm	220 ohm
R_{20}-R_{28}	47 "	68 "
R_{29}	47 kohm	47 kohm
R_{30}-R_{37}	2.7 "	2.7 "
R_{38}	18 "	18 kohm
R_{39}	820 ohm	1.5 "
R_{40}-R_{48}	1.2 kohm	1.2 "
R_{49}	∞	18 "
C_1 -C_{27}	5 nF	5 nF
C_{28}-C_{52}	1.2 "	1.2 "
C_{53}-C_{68}	5-45 pF	5-45 pF
C_{69}-C_{84}	100 "	100 "
C_{85}	0.15 μF	0.15 uF
C_{87}-C_{92}	5 nF	5 nF
L_1 -L_{32}	7.6 μH	7.6 μH
T_1 -T_8	IF-transf	IF-transf
D_1 -D_8	IN270	IN270
Plug PT	BNC 50	BNC 50
Plug PK	Cannon DE-9P	Cannon DE-9P

Table 3.1 Logarithmic detector type DAF 2A/B, components

3.2 Display system

A block diagram of the main display system is given in Figure 3.107.

3.2.1 Oscillator assembly (TF1, MO1, PH1 and PH2)

The master oscillator MO1 together with tuning fork TF1 are shown in Figure 3.8. The oscillator generates highly stable 1600 c/s square waves, the harmonics of which are removed in a tuned LC filter.

The 1600 c/s sine wave is fed to four parallel phase shifting networks of types as shown in Figure 3.9. By means of a potentiometer each signal can be phase adjusted within the range 0 - 170° with a nearly constant amplitude.

One of the four phase shifted outputs is fed to the multiplexing equipment contained in panel GH (ref Figure 3.107). Two outputs feed the cursor and readback resolvers RS2 and RS3, and one is fed to limiter LI1 for use in modulator MD1.

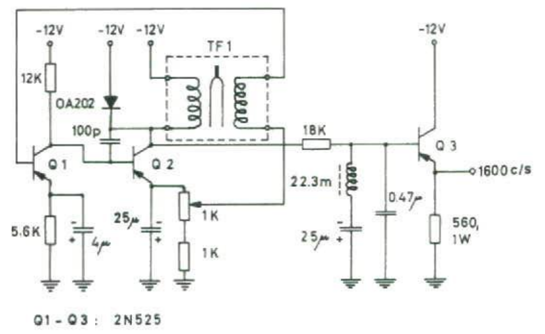


Figure 3.8 Master oscillator MO1

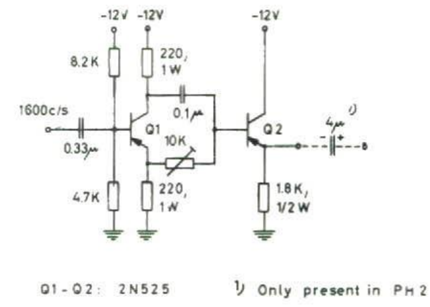
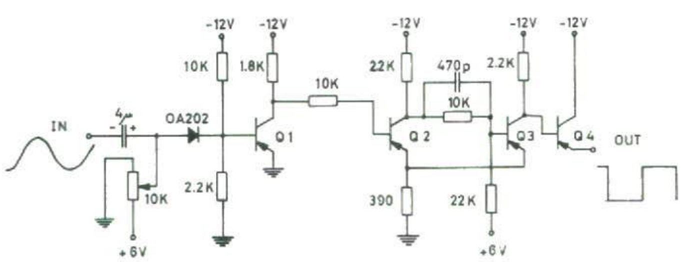


Figure 3.9 Phase shifter PH

3.2.2 Limiter LI1 and modulator MD1



Q1 - Q4 : 2N525

Figure 3.10 Limiter LI1

The limiter LI1 in Figure 3.10 is fed from a sine wave of approx 3 V amplitude peak-to-peak. The signal is clipped by diode and transistor actions in transistor circuit Q1, and is then squared by Schmitt trigger circuit Q2-Q3. The emitter follower Q4 output is a 1600 c/s square wave alternating between -12 V and 0 V.

This square wave is fed to the base circuit of transistor Q2 in the modulator MD1, Figure 3.11, thus switching transistor Q2 between saturation and cut off.

The base voltage of Q3 is therefore alternated between ground potential and the input signal level. The emitter of Q3 is biased by a negative voltage, variable by means of the ZERO CIRCLE control available on the front panel. Transistor Q3 will therefore only pass that part of the chopped waveform which exceeds the bias level. The Q3 output signal is filtered by an LC-circuit, and amplified by Q4-Q5. The output signal thus obtained is a sine wave of amplitude proportional to the difference between input signal and bias voltage if this difference is negative, and is zero otherwise.

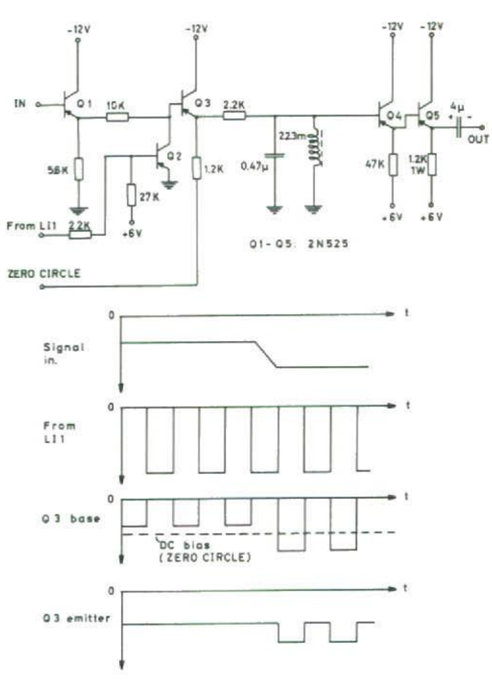


Figure 3.11 Modulator MD1

3.2.3 Recorder amplifier AA3

One modulator output feeds recorder amplifier AA3, ref Figure 3.12. The output of emitter follower Q1 is voltage divided in a 5 kohm external potentiometer (AVT GAIN) located on the front panel.

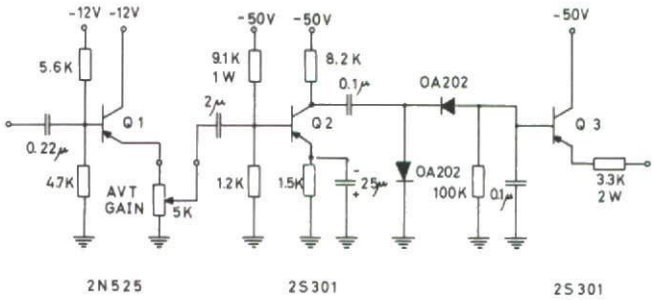


Figure 3.12 Recorder amplifier AA3

The signal is amplified by Q2 and then rectified in a voltage doubling rectifier, the output of which is amplified in emitter follower Q3. The DC output is fed through a series resistor to the recording helix of the AVT recorder, where the circuit is closed through the recording paper to ground.

3.2.4 Signal amplifiers AA1 and AA2 and gates G5

The resolvers RS2 and RS3 are fed with constant voltage 1600 c/s sine waves, and RS1 is fed with a sine wave of amplitude dependent upon the signal level. Each resolver has two outputs, being proportional to the sine and cosine of the rotor angle respectively.

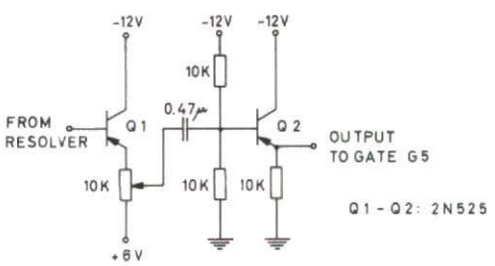


Figure 3.13 Analog amplifier AA1

Each resolver output is fed to an analog amplifier AA1 (ref Figure 3.13) where the appropriate gain is adjusted in the emitter circuit of transistor Q2. The signal is then fed through emitter follower Q2 with a DC bias of -6 V to the input of a gate G5 (ref Figure 2.5).

The gates are combined in two groups each of four gates. In each group there are two pairs each containing two gates gated in phase opposition, their outputs being strapped together. Each pair delivers one of the two input signals. One pair of the first group selects the sine output of RS1 or RS2, the other group selects the corresponding cosine output.

The second group selects in a similar manner either the outputs from the first group or the outputs from resolver RS3.

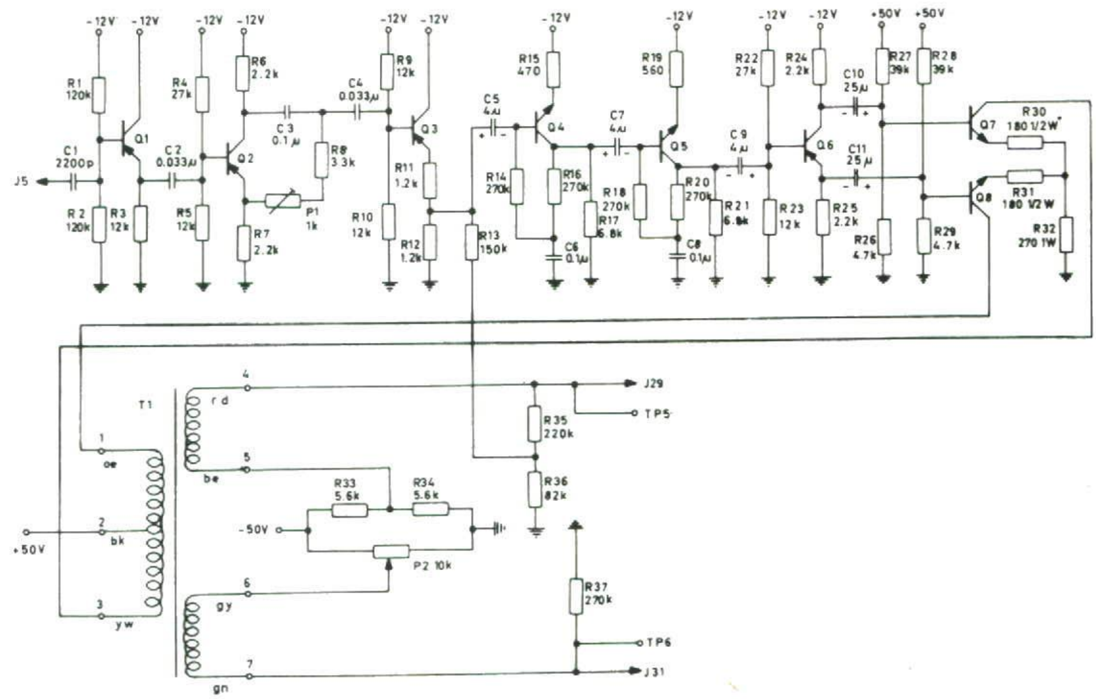
In normal operation the selection is performed by the multiplexing circuit. For maintenance and control purposes selection can take place by means of switch SW7 located on the control panel. SW7 has the following positions:

1) NORMAL	Gating is performed by the multiplexing equipment.
2) SIGNAL	The first gate group is blocked for the RS2 signals, and the second group is blocked for RS3 signals. Only the RS1 signals are permitted through the gates.

3) CURSOR — The first group is blocked for RS1 signals, and the second group is blocked for RS3 signals. Only the RS2 signals are passed by the gates.

4) READBACK — The first group is blocked for RS1 signals. The second group is controlled by the multiplexing equipment. The RS2 and RS3 signals are thus passed in time division multiplex.

Each of the two outputs of the second gate group is fed to an amplifier type AA2, which drives the X- and Y-deflection plates of the cathode ray tube. The amplifier (ref Figure 3.14) delivers an output signal of amplitude 600 V or higher. By means of a potentiometer the amplifier's phase shift can be adjusted, to provide equal phasing in the X and Y channels. (Equal overall gain is adjusted by means of the appropriate potentiometer in AA1, ref Figure 3.13). A potentiometer in the output stage is provided for centering of the display.

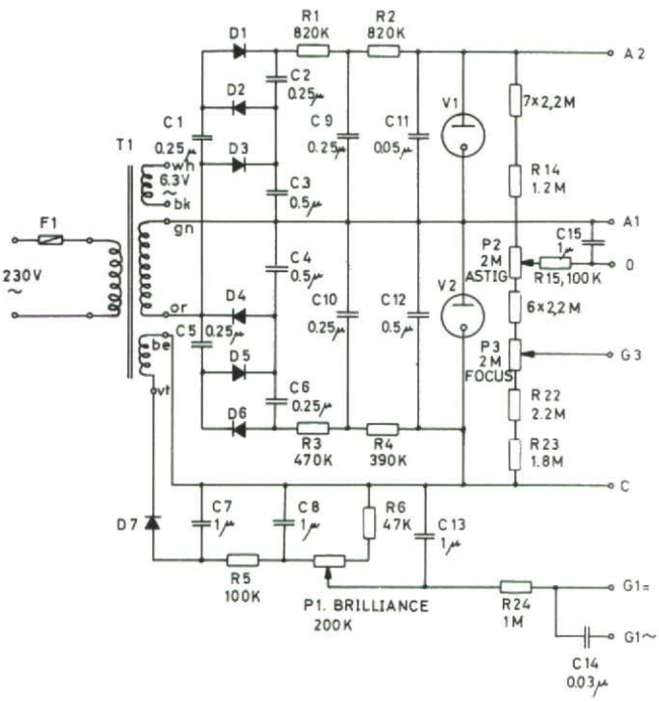


Q1, Q2, Q3, Q6 : 2S303
Q4, Q5 : 2N1711
Q7, Q8 : 2N699

Figure 3.14 Output amplifier AA2

3.2.5 High voltage supply PS5

The high voltage supply PS5 (ref Figure 3.15) for the cathode ray tube is located in the oscilloscope drawer. The following operator controlled potentiometers are available on the front: BRILLIANCE, FOCUS and ASTIGMATISM.



D1 - D6 : Sentercel K3/40
D7 : Sentercel K3/8
V1 - V2 : SC2/2500
F1 : 100 mA fuse

All resistors 1W

Figure 3.15 High voltage supply PS5

3.2.6 Multiplexing equipment

The main parts of the multiplexing equipment are located on cards 14 - 20 in panel GH.

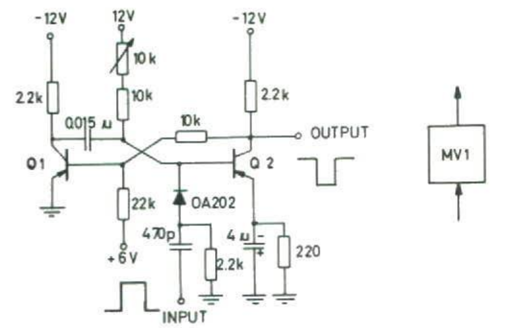
The purpose of the multiplexing equipment is on the one hand to control gates G5 to allow the three sets of input from RS1-RS3 through amplifiers AA2 in the right sequence, and on the other hand to generate brightening pulses to the cathode ray tube grid such that undesired parts of the various signal waveforms are suppressed on the CRT display.

The main waveforms are shown in Figure 3.106 which should be studied together with Figure 3.107. 1600 c/s square wave pulses (A) derived from master oscillator MO1 feed a four stage binary counter type CO1. The output $\overline{C}$ of the last stage is inverted to produce waveform C, and again inverted to reproduce $\overline{C}$. The two latter outputs control through switch SW7 the passage of the signal (from RS1) and the cursor (from RS2) through the first set of gates G5. During a negative half cycle of C eight full cycles of the RS1 waveform are passed, and during a positive half cycle of C eight full cycles of the RS2 waveform are passed.

The second gate G5 group is normally kept open for the signals arriving from the first group. The second group must, however, change over to the RS3 signals when readback strobes are to be presented.

When readback display is requested, a SET pulse is fed to an eight stage shift register type SH1 and is shifted in synchronism with the inverted clock signal $\overline{A}$. Waveform E (normally negative) becomes zero and reverts the state of the second gate group G5. E will stay zero until the initial SET pulse has passed out of the fifth SH1 stage, thus permitting the passage through the gates of 4.5 cycles of the RS3 waveform.

Each uninterrupted RS1 and RS2 waveform train consists of eight full sine wave cycles. The first four cycles are blanked on the display to suppress transients occurring in amplifiers AA2 due to the gate switching. This is achieved by a logic combination in a DL1 circuit on card 16 of clock pulses A with the output B of the third counter stage. Similarly, after a readback interruption, the first three cycles are blanked. For the latter purpose, waveform D is generated (DL2, EF2 on card 16). The logic AND combination ABD (where ONE ≡ -12 V, ZERO ≡ 0 V) yields the basic waveform I (TP16.06).



Q1, Q2 : 2N525

Figure 3.16 Monostable multivibrator MV1

Readback is requested 3.5 cycles before the readback signal (from RS3) is to be displayed, to allow transients to die out. A control pulse F is therefore taken from the fifth SH1 stage (TP18.04). F is logically combined with A to give a display order pulse G (TP 6.07). By combination of I and G, waveform K = IG results (TP16.09).

Waveform K is fed to the monostable multivibrator MV1, Figure 3.16, which through EF2 (TP16.11) delivers brilliance pulses L of the required duration T/4 (where T equals one 1600 c/s cycle).

It is required that the brightness level of the displayed RS2 signals can be made lower than that for RS1 and RS3. A brightness level waveform H is therefore generated according to the logic equation $H = \overline{C}\,\overline{G}$ (TP16.08).

H and L feed a desensitizing circuit DS1 shown in Figure 3.17. When H = 0 V, transistor Q1 is cut off and Q2 saturated, supplying Q3 with full collector voltage supply. Q3 and Q4 therefore act as a normal emitter follower and an inverter respectively, the output yielding pulses of 50 V amplitude.

When H is negative, Q1 is saturated and the base supply of Q2 is variable between 0 and -2.5 V by means of external potentiometer P1 (CURSOR BRIGHTNESS). For L = 0 V, Q3 and Q4 are both cut off. For L = -12 V, the working point of Q4 is variable between saturation and cut-off by means of P1.

The output diodes serve as overvoltage protection for Q4 when the high voltage power supply PS5 (ref Figure 3.15) is switched on or off.

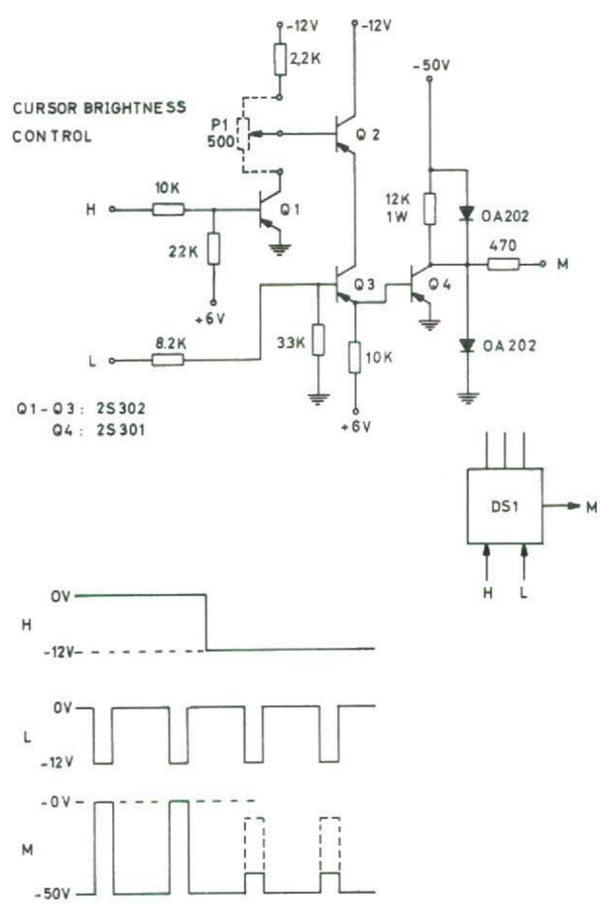


Figure 3.17 Desensitizer DS1

3.2.7 Servo system

In Figure 3.107 resolver RS1 and the recorder helix shall both be slaved to the antenna rotation. This is achieved by means of a closed loop servo system as shown in Figure 3.108. It receives a double set of inputs, one from a 1 : 1 synchro transmitter ("Coarse") and one from a 36 : 1 synchro transmitter ("Fine"), plus an AC reference.

In servo amplifier SA1 the inputs are first combined in a data switch comprising diodes D1-D4, Zener diodes Z1-Z2, resistors R1-R3 and capacitor C1. The Zener voltage of Z1-Z2 is about 4 V. If the coarse error voltage exceeds the Zener voltage, Z1 and D1 (or Z2 and D2) have a negligible resistance, and the coarse synchro voltage takes control of transistor Q1 input. For small coarse synchro errors, transistor Q1 input is controlled by the fine synchro voltage. The critical coarse synchro error is approximately $\pm 3^{o}$.

The 115 V AC reference voltage is divided by R2 and the coarse synchro rotor impedance to provide a 2.5 V AC stick-off voltage in order to remove the possible false stable nulls near 180^{o} coarse synchro error. The coarse synchro is offset 2.5^{o} to preserve the true stable null position. Diodes D3-D4 serve to protect the input transistor in case of excessive error voltages.

The input error signal is amplified by Q1-Q2 in a normal manner, and phase split in Q3 (assuming SW8 to be in position NORMAL, making Q3 active and Q4 cut-off). The two phase split signals are next amplified by transistor circuits Q5-Q8 and Q9-Q12 respectively, Q7-Q8 and Q11-Q12 operating on a reduced collector voltage supply (-6 V derived from R29, Z3).

Servo amplifier SA2 contains its own power supply of approximately -33 V. Through class B output stages Q3-Q4 the two halves of one stator phase of servo motor M2 are fed in push pull, the second phase being driven by the reference voltage. Motor M2 in turn drives the input synchros, resolver RS1 and the AVT helix through appropriate gear assemblies.

When switch SW8 is in either of the two FREE positions, transistor Q3 of SA1 is cut off, and Q4 is active. The input error signal is thereby blocked, and replaced by a constant AC voltage supplied to the base of Q4. The servo system is thereby made free running.

3.2.7.1 Connection at AN/FPS-8 stations

At the AN/FPS-8 stations the DAF servo system is directly connectable to the antenna data take-off system, shown in Figure 3.109.

3.2.7.2 Connection at S-266 stations

Stations equipped with Marconi type S-266 radar employ an open loop selsyn system, having a selsyn transmitter geared in a ratio of 30 : 1. A servo gearbox is therefore used for convertion to a double speed 1 : 1 and 36 : 1 servo system for application requiring the latter data. The converter (developed and produced by the Royal Norwegian Air Force, Air Materials Command and Air Depot) is shown in Figure 3.110 together with the DAF termination.

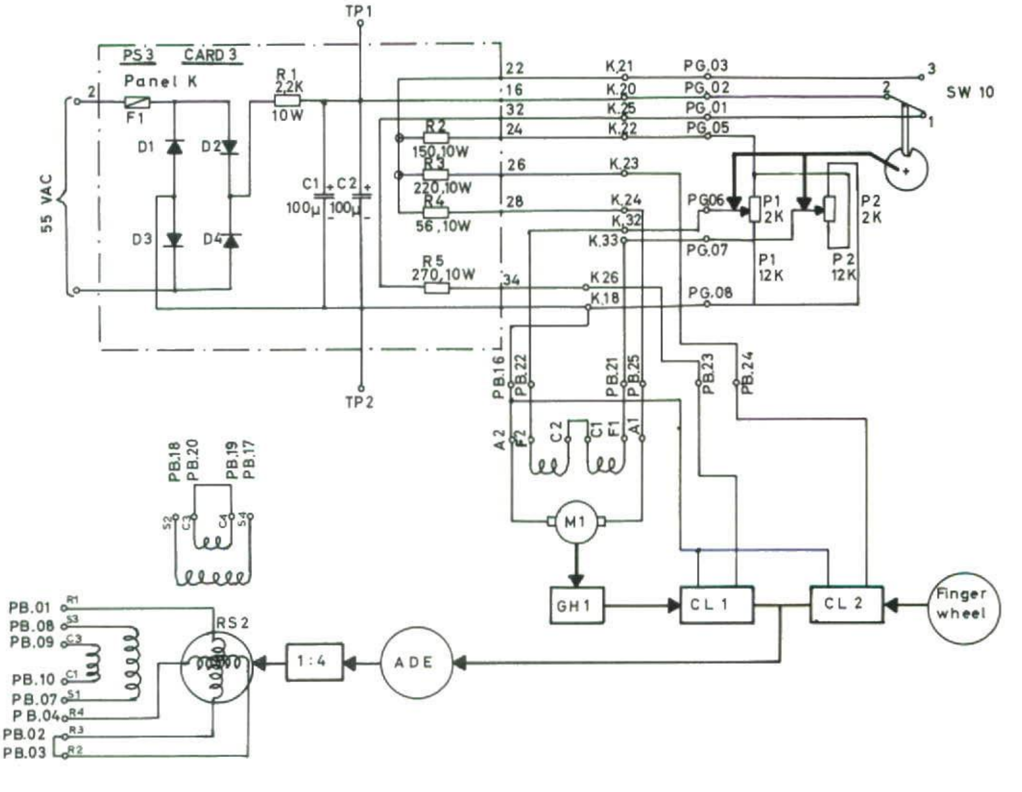
By means of a 6 : 5 gear, the desired 36 : 1 fine synchro speed is obtained. To avoid the 30-fold ambiguity, two cam operated switches are connected to the coarse synchro drive, closing a relay circuit during an arc of $\pm 2^{o}$ about North. The relay voltage supply is controlled by a switch connected to the antenna drive, the latter switch being opened $\pm 4^{o}$ about North. Thus, if an erroneous phase has been obtained, the relay will operate when the receiving system is at the apparent North position, and the receiver selsyn is stopped. The relay circuit is broken when the antenna is in the true North position, and from then on the receiver system is slaved to the antenna.

3.2.8 Cursor control

The rotor position of resolver RS2 can be controlled by a wheel located on the control desk, or by means of motor M2 which is governed by two pedals (for clockwise or counterclockwise rotation). Geared to the resolver RS2 is the analog-to-digital encoder ADE. The gearing ratio (4 : 1) is determined by the fact that the ADE requires four rotations for one full cycle of its most significant digit.

The circuit diagram is given in Figure 3.18. The pedals control the sliding contacts of potentiometers P1-P2, and also switch SW10 which changes over when the pedals move from the neutral position. In the neutral pedal position clutch CL1 is disengaged and CL2 engaged, such that RS2 and ADE control is by means of the wheel only.

When the pedals leave their neutral positions, cam switch SW10 changes over and motor M1 receives armature and field voltages. Simultaneously, clutch CL1 becomes engaged and CL2 disengaged. The motor therefore takes over the control, and the wheel is disabled. The sign and amplitude of the field voltage are dependent upon the pedal excursions. With a motor speed of 8000 rpm, a full rotation of the resolver takes about 0.5 seconds.

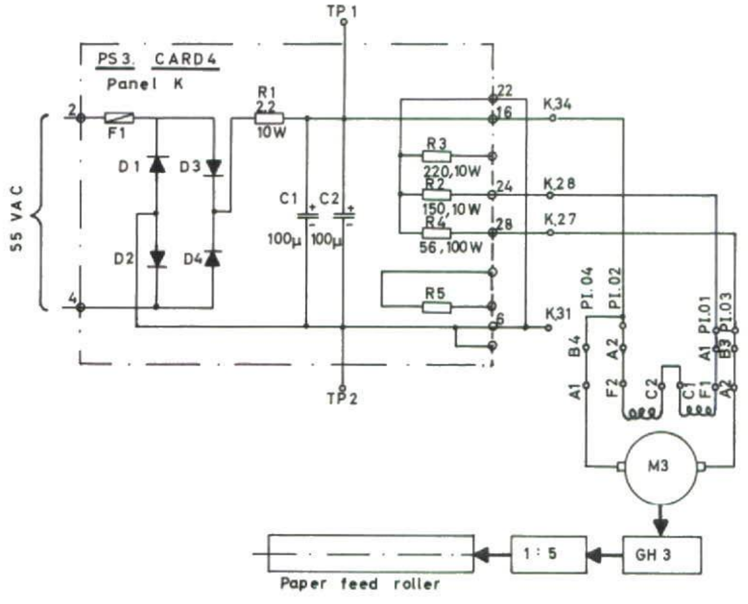


M1 : Evershed FAR 101/B6/BD
ADE : Librascope 713D
RS2 : Kearfott R980-41A
CL1-CL2 : Kearfott R5750-002
GH1 : Kearfott-CVO-5708-008 (65 : 1)
D1-D4 : 1N1117
F1 : 2.5 A fuse

Figure 3.18 Cursor control system

3.2.9 Paper feed drive

The AVT paper drive circuit is shown in Figure 3.19. The motor rotates at approximately 8000 rpm with the gear ratios chosen, the paper is fed approximately 8 mm per minute.



D1 - D4 : 1N1117
M3 : Evershed FAR 101/B6/BD
GH3 : Kearfott CVO 5708-031 (12300:1)
F1 : 2.5 A fuse

Figure 3.19 AVT paper feed drive

3.2.10 IFF simulator SI1

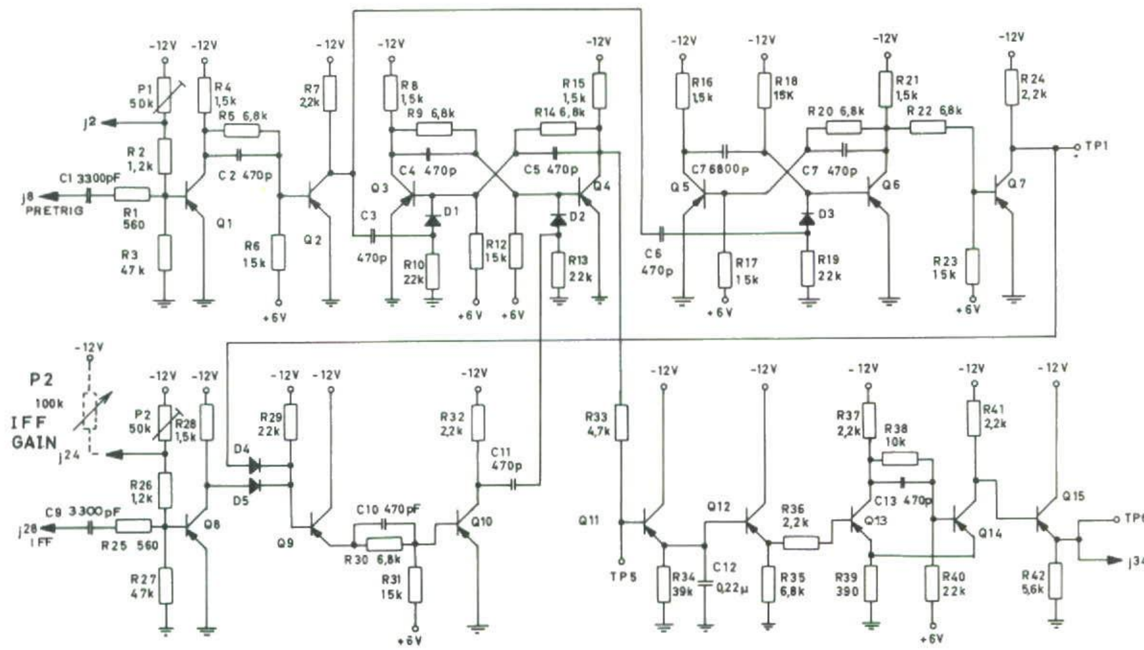
When switch SW9 in Figure 3.107 is in the IFF SIMULATOR position, a continuous IFF request is sent to the IFF equipment via cable 1313. The IFF equipment is prewired to challenge mode 1 on the selected channel and the IFF returns are received via cable 1308. The modulator MD1 input is now connected to the simulator SI1 output, and the AVA display will paint a constant amplitude sector for every train of IFF returns.

Figure 3.20 shows the circuit diagram of the simulator, and the main waveforms are given in Figure 3.21. (A train of two IFF returns only is shown). The radar pretrigger (some 5 - 10 μs ahead of the main radar trigger) is amplified and inverted by transistor Q1. After further inversion in Q2, the monostable circuit Q5-Q6 is triggered to produce an inhibition pulse of approximately 80 μs duration. Simultaneously, the set/reset circuit Q5-Q6 is reset (if not reset beforehand).

An incoming IFF return is amplified and inverted in transistor Q8. If the IFF pulse arrives within 80 μs of the radar pretrigger, the diode logic D4-D5, R29 is closed. This arrangement is introduced to prevent triggering by undesired leakage of the radar transmitter pulses on to the IFF receiver.

If the IFF return arrives outside the inhibition interval, it is amplified and inverted by Q9-Q10, and then used to set circuit Q3-Q4. The output of Q4 is first peak rectified in the Q11 circuit, and then passed to emitter follower Q12. The Q12 output feeds the Schmitt trigger circuit Q13-Q14, the output of which is amplified in emitter follower Q14.

The trailing time constant τ of the R34-C12 network of the rectifying circuit has been selected such that the Schmitt trigger output pulse has an excessive length



Q1 - Q6, Q8 - Q10 : 2N395
Q7, Q13-Q15 : 2N525
Q11-Q12 : 2S302
D1 - D5 : OA95

Figure 3.20 IFF simulator SI1, circuit diagram

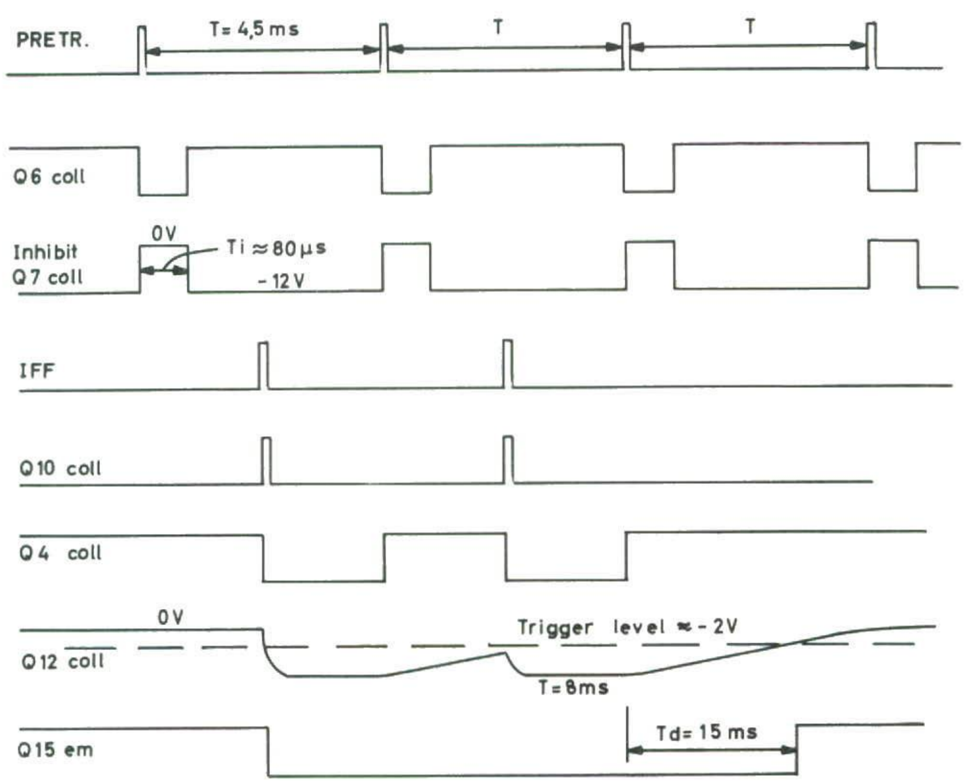


Figure 3.21 IFF simulator SI1, waveforms

$T_d > 2T$ where T is the radar repetition period. The reason is that if other operators request modes 2 and 3, a mode 1 return will be received only during each third radar sweep.

In the simulator potentiometer p1 is preset to ensure stable operation of transistor Q1 for the existing signal to noise ratio in the radar pretrigger circuitry.

Internal potentiometer p2 is set at maximum, and is parallelled with external potentiometer P2, located on the front panel. This potentiometer (IFF GAIN) is adjusted by the operator to give a reasonable rate of false alarm, i e triggering due to noise in the IFF channel.

3.3 Data transmitter

For a description of the main principles of the data transmitter, reference is made to Part I, Section 2.2.3.

The data transmitter is contained in panel AB with controls located on the operator's desk.

A complete block diagram is given in Figure 3.112 which should be used for general reference throughout this section.

The transmitter includes the following main units:

a) Keyboard switches and associated circuits

b) Address read out unit

c) Information read out unit

d) Electronic data converter

3.3.1 Keyboard switch controls

The keyboard switches shown in Figure 3.22 are connected to the transmitter panel AB by card plugs N and O. Each push-button on the keyboard is provided with a built-in lamp (terminals d - e). When a button is pressed, a double set of contacts a, b, c and f, g, h is operated.

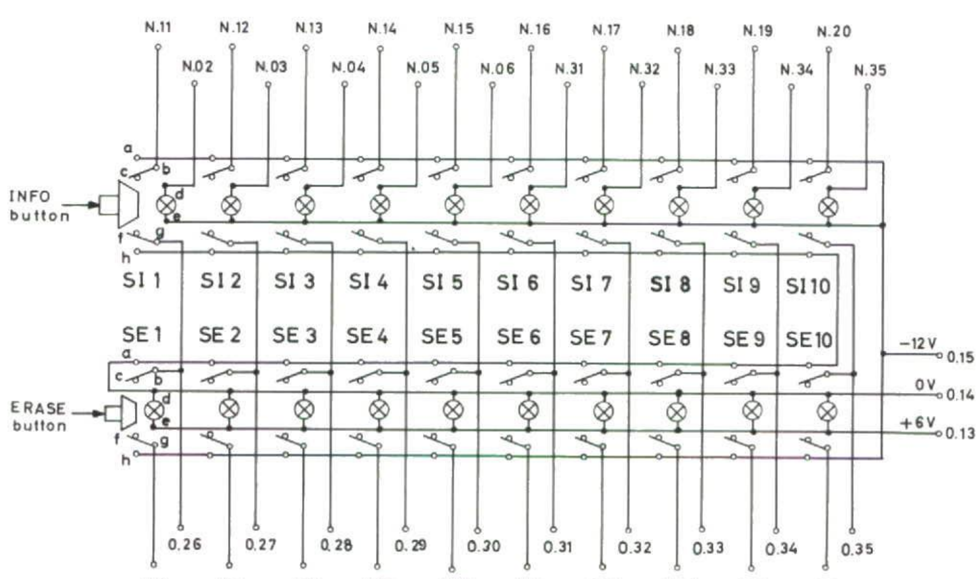


Figure 3.22 Keyboard switch controls

The three main functions of the keyboard switches are:

a) To supply control potentials (-12 V) to the set and reset terminals of the circuits controlling the illumination of the information buttons.

b) To provide one of the ten input terminals of either the information or the erase trigger channel with a negative potential (-12 V) enabling a start pulse to be generated for the electronic data converter.

c) To provide a control potential (0 V) to one of the input terminals of the address read out unit.

The functions are described below.

3.3.1.1 Lamp control circuits

The lamps in the ERASE buttons of the keyboard are supplied from a steady 6 V source which is half the nominal lamp voltage. The ERASE buttons are therefore always weakly illuminated. The illumination of each INFO button is controlled by a set/reset circuit type SR2. Since the circuits for all button sets are identical, only one of them will be treated in more detail.

The control circuit for button set No 1 is shown in Figure 3.23. When the INFO button is pressed, a negative potential of -12 V is fed to the set terminal of SR2 via contacts a, b of SI1 and plug card contact N.11. The transistor Q2 becomes saturated and the lamp in the INFO button is lit. (The series resistor in the lamp circuit, not shown in Figure 3.112, is located on plug card N on the keyboard.) When the ERASE button is pressed, -12 V is fed to the reset terminal and the light in the INFO button is extinguished.

As shown in Figure 3.112, the lamp control circuits SR2 are located on cards 1-2 in panel AB.

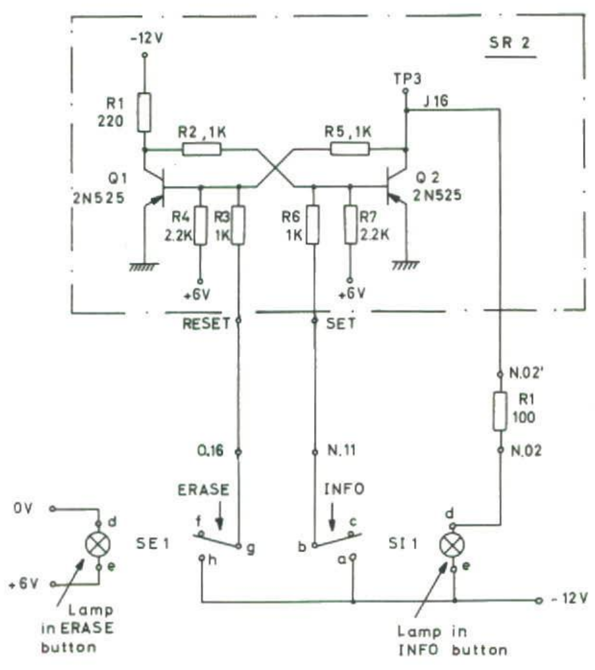


Figure 3.23 Lamp control circuit for ERASE and INFO buttons No 1

3.3.1.2 Start pulse generation

The reset signals to the SR2 circuits, provided by the ERASE switches SE1 - SE10 are also fed to diode logic DL5 of the erase trigger channel located on card 6, DL5 being an OR gate for negative pulses. When any ERASE button is operated, a differentiated negative pulse will therefore occur at the DL5 output (TP6.01). As the pulse may be distorted due to contact jitter as illustrated in Figure 3.24, certain precautions have to be taken. The output pulse from the gate is regenerated in a Schmitt trigger circuit ST1 and amplified in an emitter follower and inverter EF2-IV1B. The output of IV1B (TP6.06) may consist of more than one positive pulse and in order to discriminate against extraneous pulses, this waveform is connected to the set terminal of the set/reset circuit SR1. As SR1 responds only to the first pulse received, a negative step function is generated (TP15.03). This step function is integrated and amplified in the circuits IN2-EF3 and the integrated signal reaches the triggering level of a Schmitt trigger ST1 after a time delay of

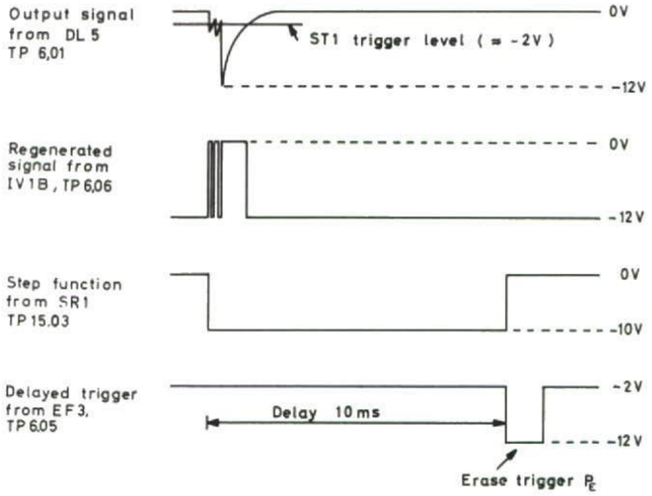


Figure 3.24 Start pulse generation

approximately 10 ms. The ST1 output waveform, a negative step function, is amplified in EF3 and fed back to a DC-coupled reset terminal on SR1. The Schmitt trigger ST1 is therefore triggered back to its quiescent state, giving out a delayed pulse P_E (TP6.05).

The INFO trigger channel is in all details equal to the ERASE trigger channel. The set signals to the lamp circuits SR2 obtained from the INFO switches SI1 - SI10 are fed to DL5 of the INFO trigger channel. When any INFO button is pressed, a delayed trigger pulse P_I is generated (TP7.05).

As shown in Figure 3.112 the delayed triggers P_E and P_I are further treated by logic circuits type DL3. These operations are described in Section 3.3.4.

3.3.2 Address read-out unit

The address read-out unit receives inputs from the keyboard switches via plug card contacts O.26-O.35. These terminals may be connected to earth potential (0 V) either through the a, b contacts of the ERASE switches SE1-SE10 or the g, h contacts of the INFO switches SI1-SI10, ref Figure 3.22.

The address read-out unit is shown in Figure 3.25. When the keyboard switches are all unoperated, the input terminals j3-j12 are floating and the diodes D1-D30 may be regarded as disconnected from the transistor circuits. In the quiescent state the base terminals of the transistors Q1-Q5 are connected to -12 V through

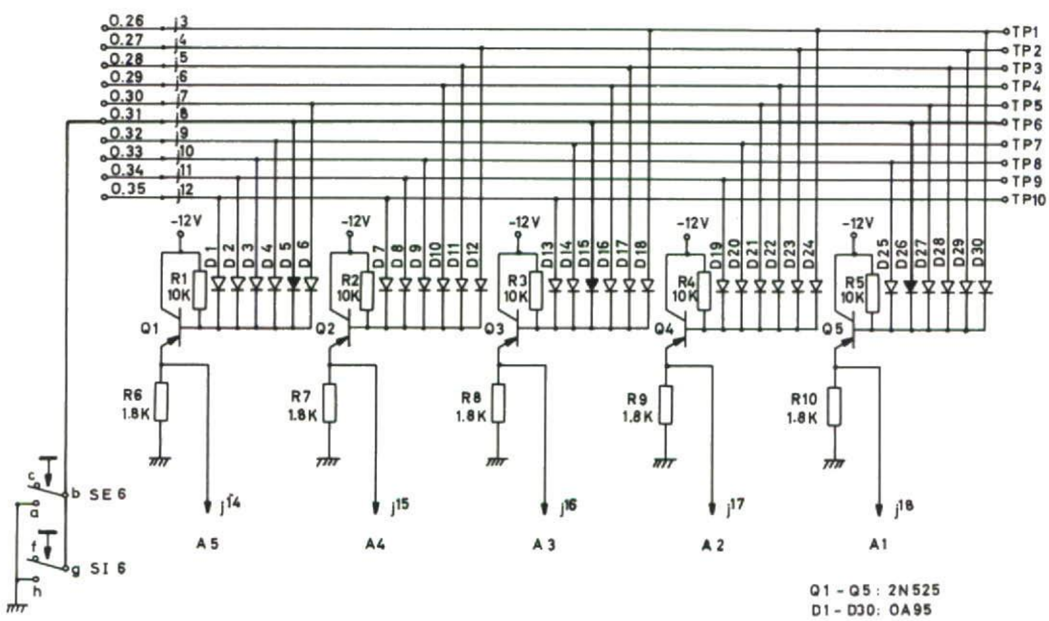


Figure 3.25 Address read-out unit

a resistance of 10 kohm and the output on-load voltages of the emitter followers are approximately -10 V. Since all the address digits A1 to A5 are negative, the read-out address combination is 00000, a ONE being here represented by the ground potential.

If a push button is pressed, an address which always contains three ONE's and two ZERO's is read out. When for example ERASE or INFO button No 6 is pressed, the input terminal j8 is connected to ground potential via plug card contact O.31. This potential is transferred to the bases of the transistors Q1, Q2 and Q5 through the diodes D5, D15 and D26 respectively. The outputs from these transistors are therefore 0 V, while the outputs from transistors Q2 and Q4 are negative. The address combination fur button No 6 is consequently 10101. Similar principles apply for the other inputs. Whenever an input line is earthed the outputs are zero from the three transistors which are connected to the line, while the outputs from the remaining two transistors are negative.

The address read out unit is located on card 3. The proper earthing of the input terminals via the keyboard switches may be measured at test points TP3.01 - TP3.10. The read-out address combination is also made visible on the transmitter indicator card L.

3.3.3 Information read-out unit

The angle to be transmitted is represented by the output of an analog-to-digital shaft encoder (ADE). The ADE contains two commutator discs mechanically geared in the ratio 64:1. The first disc (fast) is connected to the input shaft and carries seven binary digits, while the second disc (slow) carries six additional digits. The capacity of the encoder is thus 13 bits. In the data transmitter an accuracy of nine bits is required. This is obtained by omitting the four most significant bits of the second commutator disc and gearing the input shaft of the ADE to the cursor resolver RS2 in the ratio 4:1.

3.3.3.1 ADE brush selection logics

The least significant digit track on the first commutator disc is provided with only one pick-off brush B0 and the information from this brush may be read out directly. All other tracks are provided with two brushes in order to eliminate ambiguity. An information read-out unit, which selects one of the two possible brushes on each track, is therefore required. The choice of brushes is made according to the following rule:

> If the information read out from the index brush B0 is a ZERO, the second digit shall be read from the leading brush B1b of the next track. If the information from B0 is a ONE, the lagging brush B1a shall be selected.

The rule is general. If, for instance, the information read out from brush Bna (or Bnb) is a ZERO, the leading brush B(n+1)b on the next track is to be selected for the next digit.

A diagram of the three first stages of the information read-out unit is shown in Figure 3.26. As all metal parts of the commutator discs are grounded, the brushes have been drawn as switches which are either open circuited or grounded. In the description below, the following convention is used:

ZERO ≡ negative

ONE ≡ 0 V

B0 is read out directly by means of an emitter follower EF1A located on card 3. If B0 is open the least significant digit $\varphi 1$ is read out as a ZERO (negative). If B0 is closed, as shown in the figure, $\varphi 1$ is read out as a ONE (0 V). According to the rules the lagging brush B1a is to be selected in this case.

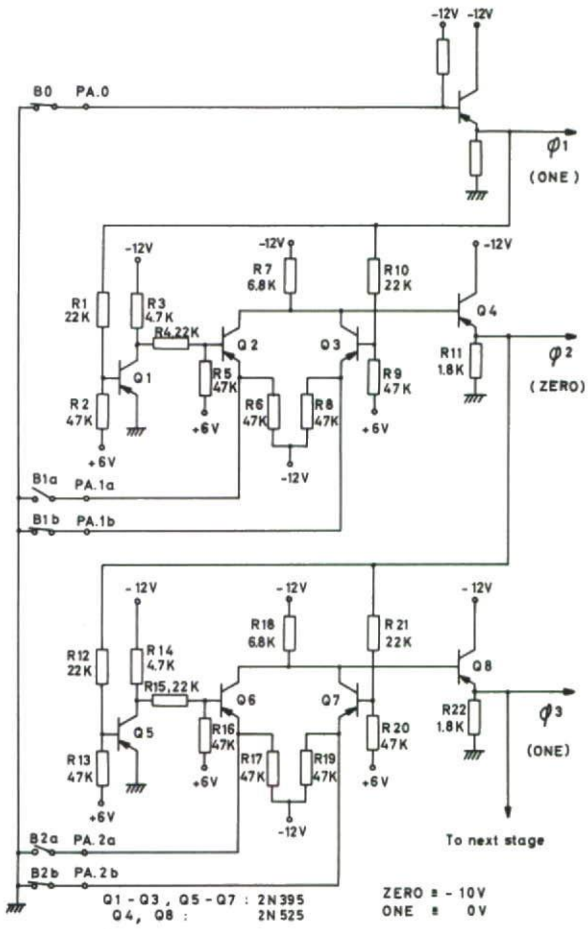


Figure 3.26 ADE brush selection logic

When φ1 is a ONE, the base of Q3 receives a positive bias. This transistor is therefore cut off and may be regarded as disconnected from the common collector load R7. No information can thus be transferred from the leading brush B1b to the output circuit. The inverter transistor Q1 is also cut off and -12 V is fed to the base terminal of the gate transistor Q2 through resistors R3-R4. This gate is therefore open and the information from the lagging brush B1a is transferred to the output. If the B1a brush is closed, Q2 is saturated and the collector load R7 is grounded through the transistor. The φ2 information is read out as a ONE (0 V). When the brush B1a is open as shown in Figure 3.26, the emitter of Q2 is biased negatively through R6. The transistor is therefore cut off and a ZERO is read out from Q4.

When φ2 is ZERO, transistor Q6 is cut off and Q7 is active. The information from brush B2b is transferred to the φ3 output, as shown in the figure. This output is further connected to the input of the next stage of the information read-out unit, and so forth.

3.3.3.2 ALL ZERO converter

The nine angle digits φ1 - φ9 from the information read out unit are fed to diode logic DL2 (located on card 3) which acts as an OR-gate. If one or more of the angle digits is ONE the output is at ground potential. The output from this gate is amplified in EF2 and inverted in an IV1A circuit. The output from IV1A is further connected to a second OR gate DL2 together with the least significant angle digit φ1. If one or more of the angle digits is ONE the output from IV1A is negative and the output from the second OR gate will be determined by the φ1 digit, i e x = φ1. When all angle digits φ1 to φ9 are ZERO, the output from IV1A is at ground potential and the x output from the second OR gate is a ONE.

The above logic chain therefore acts as an ALL ZERO converter as described in Part I, Section 2.2.3.

The outputs φ1 - φ9 of the information read-out unit and the x output from the logic circuits are made visible on the transmitter indicator card L.

3.3.4 Electronic data converter

The task of the electronic data converter is to convert the parallel information read out from the address and information. The conversion is done in a shift register having fifteen SH1 stages located on cards 8-11. Each SH1 stage contains an inherent input gate. The control terminals of the gates are connected to the output terminals of the address and information read out unit as shown in Figure 3.112.

The input gate of the first stage is controlled by the x digit, which equals $\varphi 1$ unless all angle digits are ZERO. Stages 2-9 are controlled by $\varphi 2$-$\varphi 9$, while the stages 10-14 are controlled by the address digits A1-A5.

Stage 14 is also used for parity setting as will be made clear later. The A5 signal is for this purpose connected to the input of a diode logic DL1 together with a parity control signal. DL1 acts as an OR gate for positive signals. The parity control signal, which is obtained from an SR1 circuit is always negative when the address set pulse arrives. The initial setting of stage 14 is therefore controlled by A5. Later on, when the address has been transferred to the shift register, the input terminal j3.32 of DL1 is grounded by the parity control signal. The input gate of stage 14 is then open without regard to the A5 control signal.

As shown in the block diagram, the address and angle information are transferred to the shift register by two set pulses derived from the ERASE and INFO trigger pulses P_E and P_I. The P_E and P_I pulses and a test pulse from the pulse sequence generator are connected to the input terminals of three diode logics DL3, acting as OR gates for negative pulses.

3.3.4.1 Start gate

The upper DL3 in the diagram, which receives both P_E and P_I, is a start pulse gate. When any of the keyboard switches are pressed, a negative pulse is obtained from the output of this gate (TP16.05). The pulse is amplified and inverted in circuits EF2-IV1B, and the positive start pulse from the output of IV1B (TP16.08) is connected to the input j15.30 of an SR1 circuit.

3.3.4.2 Address gate

The second DL3 circuit from the top is an address gate, which under normal operation of the data transmitter acts in exactly the same way as the start pulse gate. If an ERASE or an INFO button is pressed, a positive address set pulse is obtained from the output inverter IV3 (TP13.09). By this pulse the address digits A1-A5 are transferred to the shift register. The setting of A5 is done indirectly through the circuits SR1, DL3, EF2, IV1. This will be described in more detail below.

3.3.4.3 Information gate

The third DL3 circuit from the top is an information gate. During normal operation this gate receives only the P_I pulse from the information trigger channel. The negative pulse from the gate is amplified in EF2-IV3 and the positive INFO set pulse from the output of IV3 (TP14.09) is connected to the set terminals of stages 1 - 9 of the shift register. It is thus seen that the information angle can only be transferred to the shift register if an INFO button is pressed. As shown in the diagram, both the address and the information gate may receive a test pulse P5 from the pulse sequence generator if the MODE SELECTOR SW3 is in the TEST (2) position. This test operation will be described later.

3.3.4.4 Pulse sequence generator

The conversion of the address and angle information into teleprinter characters is controlled by a pulse sequence generator. The signals generated within this part of the data transmitter are shown in Figure 3.111, which should be consulted together with Figure 3.112. With the MODE SELECTOR switch SW3 in the NORMAL position, a 100 c/s clock signal obtained from the display system is fed to the input gate EF2-G1 on card 12. G1 is controlled by a set/reset circuit SR1. When a start pulse (from TP16.08) is received by the set terminal of SR1 the control terminal j12.32 of G1 is grounded. The gate is then open and the clock signal is transferred to the input terminal of the element counter on card 17 through EF2-IV1. The relationship between start pulse (TP16.08), clock control signal (j15.32) and the clock signal received by the counter (TP12.05) is shown in Figure 3.111.

The element counter counts the positive going edges of the clock signal. As shown in the main block diagram some of the output signals from the counters are connected to five DL1 circuits. To avoid excessive loading on the element counter, four of the CO1 signals are amplified and inverted in EF2-IV1 (card 19). The output signals from the right hand sides of the CO1 stages are labelled A, B, C, D, E and F in Figures 3.111 - 3.112. The corresponding left hand outputs are $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$ $\overline{E}$ and $\overline{F}$. As inputs to DL1 circuits are fed various combinations of the S, A, B, $\overline{B}$ C, $\overline{C}$, D, $\overline{D}$, E and F waveforms, the DL1 circuits acting as AND gates for negative signals. The upper DL1 in the diagram receives the waveforms B, $\overline{C}$ and $\overline{D}$. If the inputs are all negative, a negative pulse is obtained (TP19.03) which is further amplified and inverted in EF2-IV1. The output pulse P1 (TP14.04) is thus defined by the logic equation

$$P1 = \overline{B\overline{C}\overline{D}}$$

The other control pulses P2-P5, where

$$P2 = \overline{AB\overline{C}D}$$

$$P3 = \overline{CD}$$

$$P4 = \overline{SA\overline{B}\overline{C}DF}$$

$$P5 = \overline{ABCDEF}$$

are generated in a similar manner.

3.3.4.5 Teleprinter character frame

The P3 waveform is identical to an ALL SPACE teleprinter character. The negative cycle of the signal consists of a start pulse of duration 20 ms and five SPACE elements each of the same duration. The positive period has a duration of 30 ms corresponding to a teleprinter stop pulse. A total period of 150 ms, which equals the length of one teleprinter character, has been obtained by letting the positive edge of the P3 signal give an extra count to the element counter. This is done via the set terminal j17.14 on the first stage of the element counter.

The positive edges of the P3 waveform are counted also by the character counter as shown. Since the output signal from the data transmitter always consists of three teleprinter characters the character counter must count modulo 3.

An extra count is therefore given by the positive edge of the inverted P5 signal, which is taken from the EF2-IV1 circuits on card 12 (TP12.03) and fed to the reset terminal j18.17 of the character counter. The modified counter waveforms from the element and character counters will thus be as shown in Figure 3.111.

3.3.4.6 Shift signal generation

The required shift signal to the shift register is obtained by the proper gating of the $\overline{A}$ waveform from the first stage of the element counter. The control terminal j12.33 of shift gate G1 is connected to a set/reset circuit SR1 (located on card 20) which is set by the P1 pulse and reset by the P2 pulse. The obtained shift control signal (TP20.03) is shown in Figure 3.111 together with the amplified shift signal from IV3 (TP12.09). The shift signal is fed to the shift terminal of the shift register (TP11.01).

The setting of the address digit A5, which has been mentioned earlier, may now be explained in more detail. The A5 set pulse is obtained from an SR1 circuit (j20.27). SR1 is set by the normal address trigger (TP13.09) and is reset by the P1 pulse. The negative A5 set pulse is fed to the input terminal (j16.24) of a diode logic DL3, acting as an OR gate for negative signals. From Figure 3.111 it may be seen that the inverted P4 signal is positive when the A5 set pulse arrives. The A5 pulse is therefore transferred to the output of DL3 and the inverted A5 pulse (TP16.10) sets stage 14 of the shift register in accordance with the A5 control signal.

3.3.4.7 Combiner circuit

The final mixing of the ALL SPACE teleprinter character P3 with the output signal from the shift register is performed in a DL1 circuit on card 19 and the output is amplified in an emitter follower EF3 (TP19.02). The output signal from the shift register (TP11.07) has been transferred to the input of DL1 via an information gate G1. This gate is controlled by an SR1 circuit which is set by the P1 pulse and reset by the positive edge of the P3 signal. During the first 20 ms of the P3 signal the information gate is closed. Both the output signal from G1 and the P3 signal are then negative and a negative teleprinter start pulse is obtained from the output of DL1. After 20 ms the information gate is opened and the first shift pulse is received by the shift register. The address digit A5 is thereby shifted to the output stage of the shift register. If A5 is a ONE the output from the shift register (TP11.07) is negative. This negative pulse is inverted in G1 and a positive MARK element is transferred to the output of DL1. When the next shift pulse arrives 20ms later, the A4 digit is shifted to the output stage of the shift register. If this digit is a ZERO the output from G1 is negative and a negative SPACE element is transferred to the output of DL1. In this way the five address digits A1 - A5 are converted to MARK or SPACE elements in the first teleprinter character. When the address information has been inserted in the first teleprinter character, information gate G1 is closed and the positive stop pulse of the P3 waveform is transferred to the output.

During the two last character periods the procedure is repeated and the nine angle digits $\varphi 1$ - $\varphi 9$ are converted to MARK and SPACE elements within the two last teleprinter characters. The fifth element of the last character is used as a parity check as described below.

3.3.4.8 Parity pulse generation

During the conversion period the total number of ONE's in the address and angle information is counted by a parity counter CO1 on card 18. Whenever a ONE is shifted out of the shift register, the control terminal (j13.33) of a gate G1 becomes grounded. The negative edge of the shift signal is thereby inverted in G1 and a count pulse (TP13.08) is given to the parity counter. When a ZERO is shifted out the gate G1 becomes closed and no count pulse is received by the parity counter.

The output from the parity counter controls the parity pulse gate G1 on card 14. If the parity counter has received an even number of counts when the last angle digit $\varphi 1$ has been checked, the control terminal (j14.32) is grounded. The gate G1 is therefore opened and a positive parity pulse P4 is obtained from the output (TP14.07). P4 is amplified and inverted by the circuits EF2-IV1 on card 13 and the output is fed to the input terminal (j16.26) of a diode logic DL3. Since the A5 set signal is positive when the parity pulse arrives, the inverted P4 pulse will be transferred to the output of DL3. The pulse is further amplified and inverted by EF2-IV1 and the positive output pulse (TP16.10) sets stage 14 of the shift register.

When the shift pulse arrives 5 ms later the parity pulse is shifted to the output stage. The parity is thereby converted to a MARK element in the last teleprinter character.

If the parity counter receives an uneven number of counts, the P4 pulse is inhibited and a SPACE element is generated as a parity.

The above procedure ensures that the transmitted message always includes an odd number of ONE's. As the number of ONE's in the address character is always three, the number of ONE's in the angle characters is consequently always even.

When the conversion has been completed the positive edge of the P5 waveform resets the parity counter via the terminal j18.28. The same pulse is also fed to the reset terminal j15.34 of the SR1 circuit controlling the clock gate. The clock signal to the element counter is thereby inhibited and the data transmitter is returned to its quiescent state.

3.3.4.9 Arrest circuit

The P5 waveform also controls the WAIT and REPEAT indicators on the operator's desk and inhibits the address and information set pulses during the working period of the data transmitter as described below.

The P5 waveform, which is negative during the conversion period, is connected to the input terminal (j12.06) of an emitter follower EF2. The negative output (j12.04) from EF2 is fed to the input terminal (j16.13) of an inverter IV5. The output of the inverter is thereby grounded and the WAIT indicator lamp is lit for the duration of the data transmission period.

The negative P5 waveform (j12.04) is also integrated and amplified in the IN1-EF3 circuits on card 16 and after a short time delay the output terminals for the address and information set pulses will be grounded by the two inverter circuits IV4 (TP13.09 and TP14.09). It is therefore impossible to set the shift register during the normal working period of the data transmitter.

The inverted P5 waveform from the IV1 circuit (TP12.03) is fed to the set control terminal (j15.29) of an SR1 via an emitter follower EF1. The set gate of SR1 is thereby opened so that if a start pulse is received during the conversion period the SR1 circuit is set. The output from SR1 (j15.27) is inverted by EF2-IV5 and a REPEAT indicator lamp is lit. When the data transmitter has reached its quiescent state the reset control terminal (j15.26) is grounded by the EF2 circuit (j12.04) and on arrival of a subsequent normal start pulse the SR1 circuit is reset. The REPEAT indicator is thereby extinguished.

3.3.4.10 Test facilities

The data transmitter may be operated in the four modes shown in Figure 3.112. In the NORMAL and OPEN LOOP modes the clock signal to the pulse sequence generator is obtained from the display system via the plug contact G.17. The teleprinter signal from the emitter follower EF3 (TP19.02) is fed to a relay circuit REL1 which supplies approximately ± 20 mA to the line modulator. In the OPEN LOOP mode the teleprinter signal is also fed locally to the input terminal of the data receiver via the MODE SELECTOR segment SW3a, as will be described in Section 3.4.

In the two TEST modes the clock signal to the pulse sequence generator is taken from a clock generator CG1 (TP21.06). The frequency of the clock signal can be selected by the TEST GENERATOR switch SW2. The available frequencies are 2, 10, 100 and 6000 c/s. The three low frequencies are convenient when the operation of the shift register is checked visually by means of the transmitter indicator card L, while the highest frequency may be used when signals are measured with an oscilloscope.

In the TEST (1) mode the data transmitter is working in a normal manner apart from the different clock frequencies used. Also, the output teleprinter signal is disconnected from the line.

In the TEST (2) mode, which is a free running mode, the operation is somewhat different. The P5 pulse, which normally is fed to the reset terminal (j15.34) of the SR1 circuit controlling the clock gate, is disconnected by the MODE SELECTOR segment SW3b. When SR1 receives a start pulse (j15.30) the clock gate is opened and will remain open until the system is switched back to any of the other modes. The element and character counter will therefore run continuously and all control signals are steadily repeated. The P5 waveform is in this mode connected to the input terminals of the diode logics DL3 of the address and information set pulse channels via an emitter follower EF1 on card 16. When a complete message consisting of three teleprinter characters has been generated, the address and information are transferred to the shift register by the negative edge of the P5 signal and the whole message is repeated.

3.4 Data receiver and store

In the data receiver the information content of the received teleprinter signal is converted into parallel information in a shift register under the control of a sequence control unit. During the conversion period the received message is continuously checked by an address and parity checking unit. If the message is approved, an erase pulse and a delayed set pulse are delivered to the data store. According to the received address A1-A5 a word in the data store is selected and the angle information $\varphi 1$- $\varphi 9$ is transferred to this word location.

The receiver circuits are located in panel CD, and the store in panel EF. Some of the store control circuits are located in panel CD.

3.4.1 Sequence control and data conversion

The description below is given with reference to the main block diagram in Figure 3.115 and the control signal waveform in Figure 3.113.

The signals from the line demodulator are received by a relay circuit REL2. When the MODE SELECTOR switch SW3 is in the NORMAL position, regenerated signals (TP22.13) are fed to the input terminal (j6.06) of the data receiver. When the system is operated in the OPEN LOOP mode or in either of the TEST modes, the line circuit is disconnected and the signals from the local data transmitter are fed to the receiver input terminal via a resistor located on the MODE SELECTOR switch. In either case, MARK is represented by ground potential while SPACE is negative.

For the following description the teleprinter signal shown in Figure 3.113 will be used as an example. Address No 4 (combination 01110) has been chosen, while the angle combination is 010101010 corresponding to 170 angle increments or approximately 119.5°. The parity in this example is zero.

3.4.1.1 Pulse length discriminator

The negative start pulse is integrated by IN3 and amplified by EF3. The output signal (TP16.04) reaches the trigger level of a Schmitt trigger circuit ST1 after a delay of approximately 10 ms. The chain IN3, EF3, ST1 therefore acts as a pulse length discriminator, being insensitive to negative interference pulses shorter than 10 ms.

The regenerated negative pulse (TP16.05) is further amplified and inverted by EF2-IV1B and the positive output pulse (TP16.06) is applied to the set terminal (j9.17) of a set/reset circuit SR1. The setting of SR1 is controlled by the inverted teleprinter signal. When the teleprinter signal is negative, as will be the case when a start pulse is received, the control terminal (j9.16) of SR1 is grounded from the output of inverter IV1 (TP6.03) and SR1 is set. During the reception of a teleprinter character, more than one positive pulse may be obtained from the output of IV1B. Once set, however, SR1 will not react to further pulses on the input j9.17.

3.4.1.2 Clock generator

The negative output signal from SR1 (j9.15) is amplified and inverted by EF2-IV1 and the control terminal (j1.28) of clock generator CG1 becomes grounded. The generator thereby starts and the 100 c/s clock signal (TP1.03) is amplified and regenerated by EF3-ST1. The output (TP1.05) is further amplified and inverted by EF2-IV1B. The resulting waveform S (TP1.06) is shown in Figure 3.113. The clock signal S is started by every teleprinter start pulse after a delay of approximately 10 ms and is turned off at the end of each teleprinter character by a P5 pulse derived from the sequence control unit (TP7.08) applied to the reset terminal (j9.13) of the SR1 controlling the clock generator. Once reset, the SR1 is again free to be set by the next teleprinter start pulse.

3.4.1.3 Sequence control pulses

The clock signal S from IV1B (TP1.06) is fed to the input of an element counter of four CO1 stages. The output waveforms from the right hand side of the counter stages CO1, designated A - D, are accessible on test points, and are shown in Figure 3.113. The corresponding inverted waveforms, available from the left hand side of the CO1 stages are designated $\overline{A}$ - $\overline{D}$.

To avoid excessive loading some of the output waveforms ($\overline{A}$, $\overline{C}$ and $\overline{D}$) are amplified in emitter followers and inverters (EF2 - IV1). The various waveforms are combined in five diode logics DL1 acting as AND gates for negative signals. The output of each gate is amplified and inverted by EF2-IV1.

The following waveforms result (a ONE being represented by a negative potential):

$$P1 = \overline{A\,\overline{B}\,\overline{C}\,\overline{D}} \qquad (TP15.07)$$

$$P2 = \overline{S\,\overline{A}\,B\,\overline{C}\,D} \qquad (TP15.08)$$

$$P3 = \overline{A\,B\,\overline{C}\,D} \qquad (TP7.09)$$

$$P4 = \overline{S\,\overline{A}\,\overline{B}\,C\,D} \qquad (TP7.07)$$

$$P5 = \overline{S\,A\,C\,D} \qquad (TP7.08)$$

The P5 waveform is used as a stop pulse within the sequence control unit. It resets the SR1 controlling the clock CG1 as described above, and also resets the second stage of the second CO1 stage of the element counter.

3.4.1.4 Shift register operation

The set and shift signals to the shift register are obtained by suitable gating of the A waveform. The gating is controlled by P1 and P2 such that the gate controlling circuit SR1 is set by P1 and reset by P2. The output signal from SR1 (TP9.04) is fed to the control terminal (j8.32) of G1. When G1 is open, an $\overline{A}$ signal appears at the output (TP8.07), which is further amplified and inverted by EF2-IV1. The output of IV1 (TP8.03) is applied as a set signal to the first stage of the shift register. The inverted set waveform obtained from inverter IV3 (TP8.09) is employed as a shift signal. The positive going edges of the shift signal will be seen to coincide with the front edges of the teleprinter information elements. The positive going edges of the set signal occur in the middle of each teleprinter element. The set signal will set a ONE into the first shift register stage making the right hand output negative if the control input terminal (j11.15) is at ground potential. If j11.15 is negative, the first stage is not set. After the application of a shift pulse, the first stage is reset, putting the right hand output at ground potential.

Before the process starts, the state of each stage is determined by the contents of the previously received message.

As an example, the processing of the teleprinter character shown in Figure 3.113 will be discussed.

The first shift pulse shifts the old information one step to the right, and resets the first stage to a ZERO state. During the first set pulse, the teleprinter element A5 is negative. The first SH1 state therefore remains ZERO. The second shift pulse transfers this state to stage 2.

The second set pulse occurs in the middle of the positive element A4. The first SH1 state therefore becomes ONE. The third shift pulse transfers this state to stage 2, and the previous state of stage 2 is transferred to stage 3.

The process continues. At the end of character No 1, SH1 stages 1-5 contain the information A1-A5 respectively, while stages 6-15 are occupied by old information.

The second character is treated in a similar manner. At the end of this character SH1 stages 1-5 contain $\varphi5$ - $\varphi9$, and stages 6-10 contain A1-A5, while stages 11-15 contain old information.

At the end of the third character, all old information has been shifted out, and the address, angle and parity digits will be located in the shift register as indicated on indicator card M.

3.4.2 Address and parity checking circuits

For the description of the address and parity checking circuits constant reference is made to the control waveforms in Figure 3.114 and the main block diagram in Figure 3.115. This part of the receiving system receives the output signal from the first stage of the shift register and four pulses P1-P4 from the pulse sequence control unit.

The negative going edges of the output from SH1 stage 1 of the shift register is employed for address and parity checking. As shown in Figure 3.113 a negative pulse of duration 10 ms is generated for each MARK element received (TP11.04). In the diagram it has been assumed that the parity of the preceding message was a ONE. If the previous parity were a ZERO the dotted line in the diagram would apply. This, however, would not affect the number of negative going edges.

The output of SH1 stage 1 (TP11.04) is amplified and inverted by EF2-IV1, and the output signal from IV1 (TP8.04) is fed to the input terminal of a two stage address and parity counter. The input signal to the counter and the right hand output waveforms E and F are shown in Figure 3.114, where also the received teleprinter signal has been repeated for reference purposes.

3.4.2.1 Address checking

The P3 waveform (TP7.09) from the pulse sequence control unit is connected to the input terminal (j3.32) of a two-stage character counter. The counter counts the positive going edges of the P3 waveform, i e near the end of each teleprinter character. The relationship between the counter right hand output waveforms G and H and the P3 waveform is as shown in Figure 3.114.

In order to check that the first teleprinter character contains a possible address, the counter waveforms $\overline{E}$, F, G and H are connected to the input terminals of a diode logic DL1 located on card 5, the circuit acting as an AND gate for negative signals. When the address and parity counter has received three count pulses $\overline{E}$ and F are both negative. If this occurs during the reception of the first teleprinter character, i e before the character counter has received the first count from the P3 waveform, G and H are also negative and a negative output is obtained (TP5.03). This output is amplified and inverted by EF2-IV1 (TP15.04) and fed to the control terminal (j9.31) of an SR1 circuit. The SR1 control potential is therefore positive (0 V) when the P2 pulse arrives, and SR1 is set and the output voltage I becomes negative.

The SR1 would remain unset, with I positive (0 V) for counts different from 3, i e for any first teleprinter character not containing a possible address, and at the end of the first character SR1 and the counters would be reset by a P4 pulse as explained in Section 3.4.2.5.

When a possible address has been received, the SR1 circuit is, however, set as described above. The SR1 therefore acts as a correct address memory during the reception of the characters to follow.

3.4.2.2 Message checking

The P2 pulse is inverted by circuits EF2-IV1 (TP15.05) and fed with negative polarity to an input of a DL1 circuit, the other inputs being I (correct address memory output), G and $\overline{H}$ (character counter outputs) and $\overline{E}$ (from address and parity counter). As DL1 is an AND-gate for negative signals, $\overline{E}$, G and $\overline{H}$ must all be negative if $\overline{P}2$ is to be passed by the diode logic. The requirements are satisfied near the end of the third character, before the arrival of the third P3 pulse, and then only if the message is correct. A correct message is characterized by:

a) Correct address in first character (I negative)

b) Two full characters received before the end of the third character (G and $\overline{H}$ negative)

c) Total number of ONE's odd ($\overline{E}$ negative)

If all the above criteria are satisfied, $\overline{P2}$ is passed by DL1 (TP5.04), amplified by EF2-IV8 (TP10.09) and fed as an erase pulse to the data store (j18.02).

The pulse is also fed to an integrator IN5 having a time constant of 1 ms. The IN5 output is fed through EF3 (TP10.08) to a Schmitt trigger circuit ST1, where the triggering level is reached after 200 μs (TP10.10). After amplification and inversion in EF2-IV7 a positive set pulse is therefore obtained which lags the erase pulse by 200 μs (TP10.11). The set pulse is applied to the inputs of nine G4 gates.

3.4.2.3 Normal reset

The address and parity counter, the character counter and the address memory circuit are normally reset by a controlled P4 pulse. The P4 pulse from inverter IV1 (TP7.07) is amplified and inverted by EF2-IV1 and the output pulse $\overline{P}4$ (TP8.05) is fed to the input of two diode logics type DL1. The lower DL1 circuit in the diagram also receives the $\overline{G}$ and H signal from the character counter on its input terminals. When the character counter has received the third count from the P3 pulse, i e towards the end of the last teleprinter character, both $\overline{G}$ and H are negative and the negative $\overline{P4}$ pulse is transferred to the output of DL1 (TP5.07). The pulse is further amplified and inverted by EF2-IV1, the positive output pulse (TP15.09) being fed to the reset terminal (j9.34) of the address memory circuit SR1.

The I output from this circuit is thereby turned positive (0 V) and is amplified and inverted by the circuits EF2-G1 on card 8. (As shown the emitter terminal of the G1 gate is grounded and the gate is therefore operating as a simple inverter). The output $\overline{I}$ from G1 (TP8.08) which is now negative, is fed to the second input terminal of the upper DL1 circuit. The negative $\overline{P4}$ pulse will therefore appear on the output terminal of this circuit after a slight inherent delay of approximately 2 μs. The output pulse (TP4.07) is amplified by EF1 and fed to the input of diode logic DL3, which is an OR gate for negative signals. The negative output pulse from DL3 (TP16.09) is further amplified and inverted by EF2-IV3A and the positive output pulse (TP16.10) is fed to the reset terminals of the two counters.

When the character counter has been reset, the logic requirements of the $\overline{\overline{G}H\overline{P}4}$ pulse resetting the address memory circuit (TP15.09) are not fulfilled any longer and the pulse is turned negative. The pulse length, determined by internal delays of the various circuits, is of the order of 2 μs.

3.4.2.4 Missing start pulse detector

The address memory circuit and the counters will always be reset by the P4 signal when correct messages are received. When, however, a faulty message or only interference is received, the normal reset action by the P4 signal may be disturbed. An additional reset possibility is therefore required.

The second reset pulse to the address and parity checking circuit is initiated by a long stop or MARK condition on the line. The line condition is sensed by a set/reset circuit SR1 located on card 9. SR1 is set by the P4 pulse in one teleprinter character and is reset by the P1 pulse in the next character. The output from SR1 (TP9.07) therefore consists of negative pulses of 35 ms duration, as may be seen by studying the pulses P1 and P4 in Figure 3.114. The negative pulses from SR1 are integrated with a time constant of 250 ms in IN4 and further amplified by emitter follower EF3. As long as a continuous sequence of teleprinter characters is received the integrated signal does not reach the trigger level of the Schmitt trigger circuit ST1. When, however, the last character has been received the SR1 circuit will not be reset since the P1 pulse is missing. The ST1 circuit is then triggered after a delay of approximately 50 ms. The negative output (TP16.08) is amplified by EF3 and fed back to a DC coupled reset terminal (j9.23) in SR1. SR1 is reset and the circuit is switched back to its quiescent state after a short delay. The obtained reset pulse (j16.22) is fed directly to a DC-coupled reset terminal (j9.22) in the address memory circuit. It is also transferred through the OR gate DL3 (TP16.09), amplified and inverted by EF2-IV3A circuits and fed as a second reset pulse to the counters. As shown in Figure 3.114 the final reset signal to the counters (TP16.10) therefore consists of two positive pulses.

3.4.2.5 Reset for faulty messages

The waveforms in Figure 3.114 indicate how the address and parity checking unit operates when a correct message is received. The behaviour of the system when a defective message is received will be illustrated by an example.

Assume that the first address character in the received teleprinter signal contains a wrong number (1, 2, 4 or 5) of MARK elements. The criteria for the positive control pulse $\overline{E}$ F G H are then not satisfied, and the output from the address logic chain (TP15.04) is negative inhibiting the setting of the address memory circuit by the P2 pulse. The address is therefore not approved, and the I output of SR1 is positive. The potential $\overline{I}$ at the input (j4.31) of DL1 is negative when the negative $\overline{P4}$ pulse arrives. $\overline{P4}$ is therefore transferred to the output of DL1 (TP4.07). Both the character counter, which has received one count by the P3 signal, and the address and parity counter are therefore reset at the end of the first teleprinter character.

The next character received contains the five most significant angle digits, but will by the system be checked for a possible address. Assume that the character as a worst case happens to contain three MARK elements. The character is then approved by the address memory circuit and the output I from the SR1 circuit becomes negative. Assume further that as a worst case the two last teleprinter characters together contain an uneven number of MARK elements. (This can only happen if also the angle information is defective). The parity requirement (the $\overline{E}$ signal shall be negative at the end of the last teleprinter character) will therefore be satisfied. The erase pulse and the set pulse to the data store are, however, still inhibited by the message logic since the character counter has received one count pulse too few, due to the resetting of the counters after the first teleprinter character. For the same reason the first reset pulse $\overline{G}$ H $\overline{P4}$ (TP15.09) to the address memory circuit is inhibited and since SR1 is not reset the first reset pulse to the counters will also be lacking. The address and parity checking circuits are, however, reset by the second reset pulse obtained from the Schmitt trigger ST1 as described earlier.

3.4.3 Data store and associated circuits

The basic element of the data store is an SR1A stage with an associated read-out gate G6, ref Figure 3.116. Each SR1A stage represents one bit of angle information, and as there are ten words each of nine bits, the complete store comprises 90 elements.

The store is connected as a matrix of ten lines and nine columns. Each line represents a certain word, each column represents a certain angle digit.

To select a word for setting or erasing information, the corresponding SELECT WORD line (left hand side of the diagram) is grounded. Information can then be set from the vertical SET φ lines from the top.

A word can be selected non-destructively for display or read-out by the application of a negative potential to the appropriate READ WORD line to the right in the diagram. The read-out gates G6 of the word selected are then opened, and the word information is made available on the vertical φ lines at the bottom. All gates G6 belonging to a given φ digit share a common collector resistor (10 kohm).

3.4.3.1 Word selection

When a complete message has been received by the shift register one of the ten words of the data store is selected. The address digits A1-A5, which are contained in the last five stages of the shift register, are fed as control potentials to the input terminals of a word selection unit through the EF2-IV1 circuits on card 6, Figure 3.115. If an address digit is ONE the corresponding input terminal of the word selection unit is negative, otherwise the input terminal is grounded.

A block diagram of the word selection unit is shown in Figure 3.27. The unit consists of ten identical diode logics DL1A acting as AND gates for negative signals. Each circuit has three input terminals which are connected to the input lines. Assume that address No 4 (by definition combination 01110) has been received by the shift register. The input terminals j10.03, j10.04 and j10.05 of the word selector unit are then negative while terminals j10.02 and j10.06 are grounded. The output from the fourth DL1A circuit from the right (j10.11) is accordingly negative while the other output terminals are grounded.

The outputs from the word selection unit are amplified and inverted in ten EF2-IV6 circuits and the outputs from the IV6 circuits are fed to the word selection lines of the data store as shown in Figure 3.115. Word selection line No 4 (j17.32) in the data store will be grounded while all the other word selection lines are negative. To avoid interference problems in the store the word selection signals are slightly integrated by the IV6 circuits.

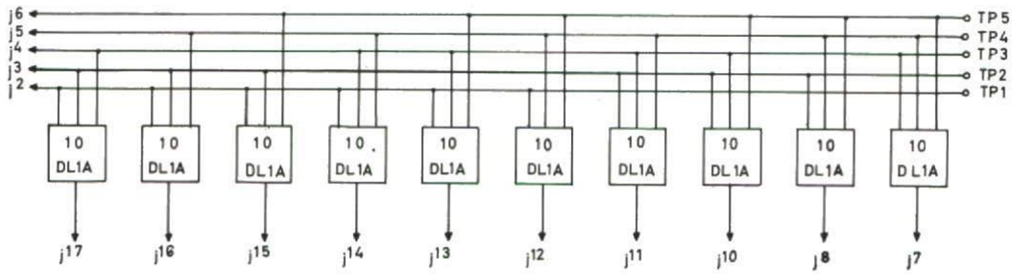


Figure 3.27 Word selection unit

3.4.3.2 Word erasure and setting

If the received message has been approved by the address and parity checking circuits, an erase pulse is fed to the erasure terminal (j18.02) of the store, and the selected word is reset, reference Figure 3.116. When for example word No 4 is selected, input wire No 4 is grounded, and only the SR1A circuits connected to that line are reset by the erase pulse being applied to all stages.

The set pulse, which is lagging the erasure pulse by some 200 μs, is fed to the emitter terminals of nine gates G4 as shown in Figure 3.115. These gates are controlled by the received angle information φ1-φ9 in the shift register. If, for instance, φ1 is a ONE, the output from the second SH1 stage is negative. This negative potential is fed to the input terminal (j17.04) of the emitter follower EF2 and transferred to the gate base terminal. When the gate emitter terminal (j17.14) is grounded by the set signal from the address and parity checking unit a positive set pulse is transferred to the output terminal of the gate (TP17.03) and fed to the φ1 set line (j2.04) of the data store. If the received φ1 digit is a ZERO, the base terminal of the gate is grounded, and the set pulse to the φ1 set line is inhibited.

Assume that the angle 010101010 has been received by the shift register. Positive set pulses are then fed to the φ2, φ4, φ6 and φ8 set lines of the data store while the set lines φ1, φ3, φ5, φ7 and φ9 receive no pulses. The received angle thereby sets the appropriate SR1A stages of the store word selected by the word selection line, the other words being unaffected due to the negative bias, reference Figure 3.116.

3.4.3.3 Automatic readout

The stored information may be read out by the application of negative pulses to the read lines of the data store. During normal operation, read-out pulses R1-R10 are applied in time sequence from the read-back system as will be described in Section 3.5. These pulses are fed to the read lines of the store via control circuits IV1C-EF2, Figure 3.115. A detailed diagram of the circuits controlling the read out of word No 1 is shown in Figure 3.28.

When the WORD SELECTOR switch SW9 is in the NORMAL position, the control terminal (j17.06) of IV1C is grounded. Transistor Q2 is then cut off and may be regarded as disconnected from its collector load. A negative read-out pulse R1 may then be transferred to the read line No 1 of the data store through a series resistor of 10 kohm and the emitter follower EF2. Gates G6 of line No 1 (ref Figure 3.116) are therefore opened, and the states of set/reset circuits SR1A of word No 1 are read out through the gates on to the vertical common lines. The gates of the other word lines receiving positive control potentials are closed. Gates G6 are non-inverting, the output of a gate being positive (0 V) when the right hand output of the associated SR1A is positive (indicating that the information stored is a ONE).

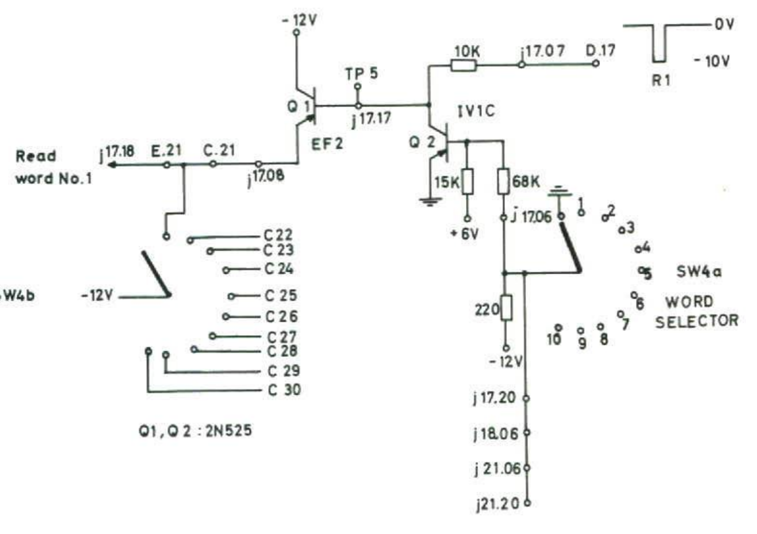


Figure 3.28 Read-out circuit for word No 1

3.4.3.4 Manual word selection

If the WORD SELECTOR switch SW4 is turned out of the NORMAL position, all IV1C stages (ref Figures 3.115 and 3.28) become saturated, and the read-out pulses R1-R10 are inhibited. If SW4 is in position WORD No 1, the read word No 1 line is directly connected to a negative potential through SW4b. Word No 1 gates G6 are all open (ref Figure 3.116) and the word content is read out onto the vertical common lines. The angle information is displayed on the indicators of card M (ref Figure 3.115). Gates G6 of all other words are closed.

Similarly, if any other word is selected by SW4, the information content of that particular word is read out onto the vertical common lines and displayed.

3.5 Read-back system

In order to present the stored angles on the AVA display, the rotor of a resolver (RS3) is rotated in synchronism with the common 1600 c/s clock signal in such a manner that one complete revolution is accomplished during $2^9 = 512$ full clock cycles (ref Part I, Figure 2.17 and Part II, Figures 3.106 and 3.107). Whenever the resolver rotor angle coincides with an angle in the store, a readback pulse is required to the display multiplexing equipment to enable the resolver output signals to be passed on to the AVA display.

In order to accomplish this task, the 1600 c/s master oscillator clock signal is also fed to a nine bits counter such that the counter state and the resolver angle bear a 1:1 relationship. After each count, the counter state is compared with every stored word in turn. If full identity is found between the state of the counter and one or more of the stored words, a coincidence pulse is generated.

The parts of the read-back system described below are contained on cards 1-14 of the GH panel and cards 1-2 of the K panel.

3.5.1 Pulse sequence generator

The description is given with reference to Figures 3.117-3.118. A 1600 c/s signal from the multiplexing circuits of the display system (j16.02) is fed as a count signal to a 9 bits angle counter (j8.16). The signal is also amplified and inverted by the EF2-IV1 circuits on card 3, and the output (TP3.08) is applied to the right hand set terminal (j7.30) of a counter stage CO1. CO1 is here employed as a pure set/reset circuit. The negative output of CO1 (TP7.13) is amplified and inverted as shown and the control terminal (j12.12) of a clock generator CG2 becomes grounded. The clock generator starts, and the obtained 80 kc/s clock signal (TP12.03) is fed to the input terminal of the counter stage CO1A. The 1:2 frequency divided signal (TP12.04) is further amplified and inverted by EF2A-IV3B.

The S signal obtained from the inverter IV3B (TP12.05) is applied as a count signal to a four stage counter. The output signals from the right hand side of the counter stages, which are accessible on test points, are designated A, B, C and D. All counter signals are amplified and inverted by the circuits EF2-IV1 on card 2-3 to avoid excessive loading of the counter. The amplified counter signals and the S signal from the IV3B circuit are connected to the input terminals of eleven diode logics of the type DL1, operating as AND gates for negative signals. With the input combinations shown, a series of negative pulses R1-R10 is obtained on the DL1 outputs, the time difference between adjacent pulses being 25 μs, equal to one cycle of the 40 kc/s S signal.

The output from the upper DL1 (TP4.02) is amplified and inverted by EF2-IV1. The obtained positive pulse (TP3.07) is fed to the right hand reset terminals (j1.10, j1.28) of stages 2 and 3 of the four stage counter and also to the reset terminal (j7.33) of the clock controlling circuit CO1. This alters the input conditions of the upper DL1 circuit, and the output of IV1 (TP3.07) becomes negative. The stop pulse is thus a positive spike of only a few microseconds duration.

The output pulses R1-R10 from the ten remaining DL1 circuits are amplified by emitter followers EF3 and fed as read-out pulses to the ten words of the data store via the control circuits IV1C-EF2 in the receiver (ref Figure 3.115). As shown in Figure 3.117 word No 4 is read out first, then word No 5 and so forth, the last word read out being word No 3. It is, however, of no importance where the read-out sequence starts since the only requirement is that all store words shall be read out during the negative part of the 1600 c/s waveform.

3.5.2 Angle counter and coincidence circuits

The nine bits angle counter on cards 8-10 counts the positive edges of the 1600 c/s clock signal from the multiplexing circuits as described above (ref Figures 3.117-3.118). At all times the counter state corresponds to the angular position of the read-back resolver rotor. For each count of the angle counter the ten words of the data store are read out in turn as explained above and the read-out angle digits φ1-φ9 are amplified and inverted by EF2-IV1 circuits.

Each digit is fed to one of the inputs of a coincidence gate G2. If the φ digit is a ONE, the input is negative, while a ZERO is represented by ground potential. The other input is taken from the right hand side of the corresponding stage of the angle counter, obeying the same voltage versus information rule. Each coincidence gate G2 delivers a negative output only if both inputs are equal (both ONE or both ZERO), otherwise the output is at ground potential.

The outputs of the nine G2 gates are fed to the inputs of a DL2 circuit acting as an AND gate for negative signals. Thus a negative output of DL2 can only occur for full coincidence in all nine G2 gates.

To discriminate against extraneous pulses near the pulse edges the output combination from the G2 circuits is sampled by a strobe pulse of approximately 7 µs duration. The strobing is obtained by feeding the 80 kc/s clock signal from CG2 and the frequency divided signal from CO1A to the input terminals j12. 23 and j12. 24 of the DL2 circuit. To ensure that a coincidence pulse is obtained only during the read-out period of the data store, the negative clock controlling signal from CO1 (TP7. 13) is further fed to terminal j12. 34 of DL2.

As described in Section 3. 3, the angle combination 000000000 is reserved as an erase message. To prevent that this combination is shown as a readback strobe on the display an inhibit pulse must be generated. As shown, all signals from the left hand sides of the angle counter stages CO1 are fed to the input terminals of a DL1 circuit on card 5. When the counter state equals the erase combination a negative pulse is obtained from the output of DL1 (TP5. 05, TP5. 06). The pulse is amplified and inverted as shown and the input terminal j12. 35 of the DL2 circuit is grounded. A possible coincidence at 000000000 is thereby inhibited.

The negative coincidence pulses obtained from DL2 are amplified and inverted by EF2-IV1, the inverted signal (TP12. 07) being fed to the set terminal (j7. 28) of a CO1 stage, which here is used as a pure set/reset circuit. If CO1 has been set, the control terminal (j12. 19) of the gate G1 is grounded and the subsequent positive half cycle of the incoming 1600 c/s clock signal is transferred to the output of G1. The regenerated signal is fed as a set pulse to the shift register (j17. 14) of the multiplexing circuits (ref Figure 3. 107). The CO1 circuit is next reset by the subsequent inverted set pulse (TP14. 09).

3.5.3 Read-back resolver drive and North reset

A block diagram of the readback resolver RS3 drive is given in Figure 3. 29. Motor M4 is driven at a synchronous speed of 8000 rpm by a 400 c/s signal derived from the main clock signal 1600 c/s, the 400 c/s being amplified in motor amplifier MA1. Through proper gears the resolver RS3 rotor is driven at a speed of 187. 5 rpm, which corresponds to one full rotation per 512 cycles of the 1600 c/s clock signal. The input of RS3 is fed with a constant amplitude 1600 c/s sine wave and the outputs reproduce the input signal multiplied by the sine and cosine of the rotor angle.

Mechanically ganged to the drive system are three discs each with an eccentric hole. The three holes are in line every third time the resolver rotor reaches the North position. The light from a lamp is then permitted through the holes on to a photocell, the output of which is amplified and regenerated in synchronizer SY1. SY1 thus produces a North reset pulse via card plug contacts K. 19 and G. 21 to the angle counter in the readback circuits in Figure 3. 118

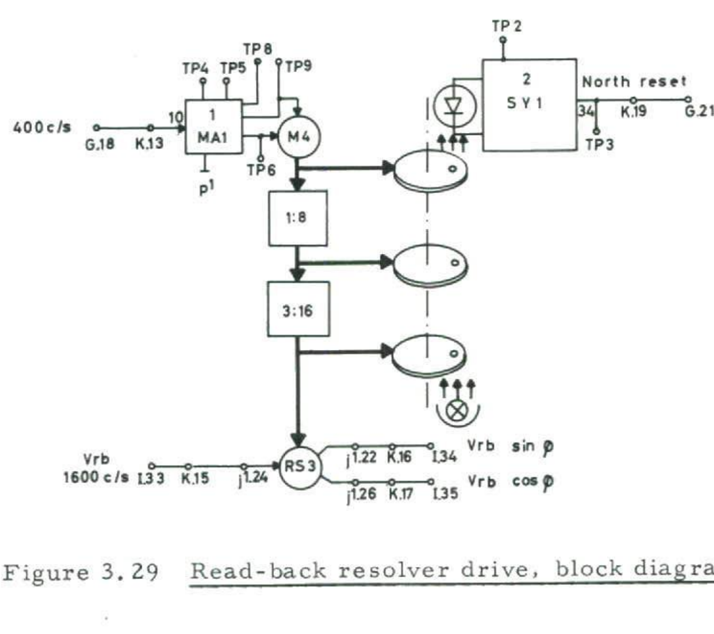


Figure 3. 29 Read-back resolver drive, block diagram

for every third revolution of RS3. The North reset pulse is by mechanical adjustment phased to occur near a negative going edge of the angle counter input waveform (j16.02 in Figure 3.117), such that reset does not take place near a counting edge of the counting waveform.

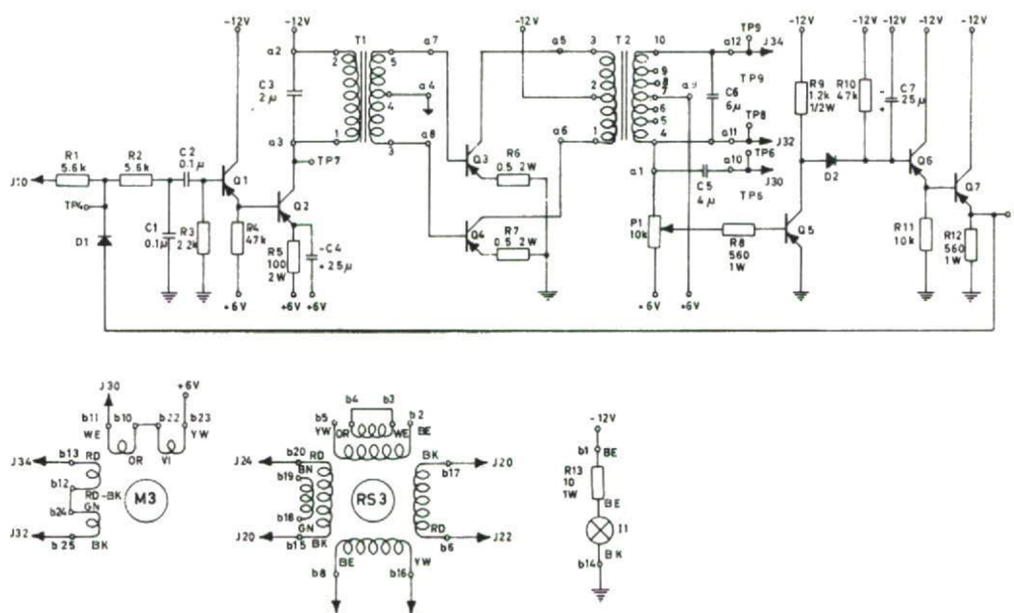
The arrangement shown in Figure 3.29 is fitted on a dual card, one card containing MA1 and the other SY1. All mechanical parts (M4, RS3, gears etc) are housed in a mechanical structure mounted between the cards. The dual card is located in card positions 1-2 of panel K.

3.5.3.1 Motor drive amplifier MA1

The motor drive amplifier is shown in Figure 3.30. The 400 c/s input square wave is slightly filtered by the input circuit and further by the collector load of transistor Q2. Transistors Q3-Q4 operate in Class B, delivering a push-pull signal to transformer T2. One motor phase is connected to T2 terminals 4 and 10 in parallel with capacitor C6, giving a parallel tuned LC circuit with the motor phase winding acting as the inductive element. The other motor phase is connected to a tap on the transformer T2 secondary through capacitor C5, giving a series resonant LC circuit. The two motor phases are thus fed with voltages of approximately 90° phase difference.

A fraction of the transformer output is fed through potentiometer p1 to the base of transistor Q5. When the AC input exceeds the base DC bias, Q5 conducts and its output is peak rectified by D2, R10, C7. The DC output is amplified in emitter followers Q6-Q7, and fed back to the input through diode D1, opposing the input square wave signal. An automatic volume control is thereby obtained.

The same card also contains the electrical connections to the read-back resolver RS3, and the light source for the photocell circuit.



D1 - D2 : OA202
Q1, Q5, Q7 : 2N525
Q2 - Q4 : 147T1 (w/heat sinks)
Q6 : 2S302
I1 : Philips 8089N
M3 : Kearfott R172-002
RS3 : Kearfott R980-41A

Figure 3.30 Motor amplifier MA1 and associated circuits

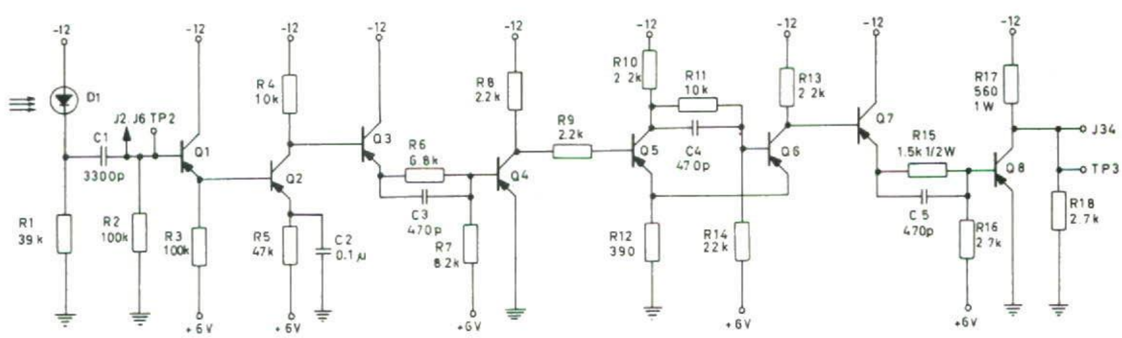
3.5.3.2 Synchronizer SY1

The synchronizer SY1 is shown in Figure 3.31. When light falls on the photocell D1, a negative pulse results at the cathode. The pulse is amplified by emitter follower Q1, linear inverting amplifier Q2 and emitter follower Q3. After inversion in Q4 the pulse is regenerated by the Schmitt trigger circuit Q5-Q6, the latter output being amplified and inverted by emitter follower Q7 and inverter Q8. A positive output North reset pulse of sharp edges is thus obtained.

The reset pulse must be properly timed. First, it shall occur near a negative going edge of the angle counter waveform (j16.02 in Figure 3.117). This is achieved by mechanical adjustment of the stator of motor M4 in Figure 3.30. Secondly, the readback strobes must occur at the angles initially set. For this purpose the cursor resolver is orientated in any convenient angular position and an angle information transmitted in a normal manner. The rotor of resolver RS3 is next mechanically turned until the readback appears in the direction transmitted. By this procedure all circuit delays are fully compensated for.

For the above adjustment the angle having the binary combination 000000000 must be avoided, because this particular combination is automatically transposed to 000000001 during transmission.

For practical purposes the North reset pulse occurs once for every three rotations of the readback resolver. Once reset, the angle counter (ref Figure 3.118) will remain in proper phase.



D1 : OAP12
Q1 : 2S302
Q2 - Q8 : 2N525

Figure 3.31 Synchronizer SY1

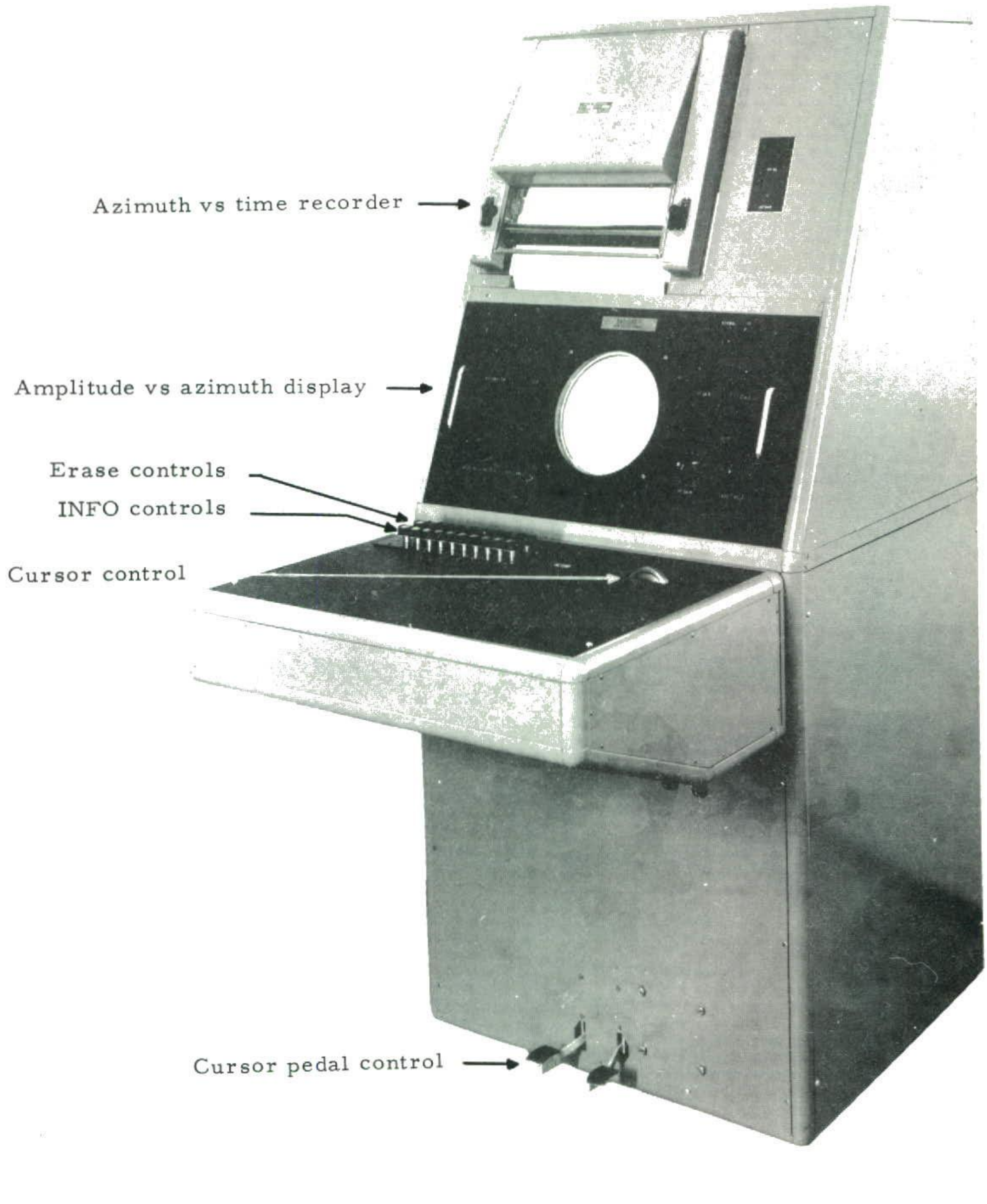


Figure 3.101 Strobe reporting station SRS-1

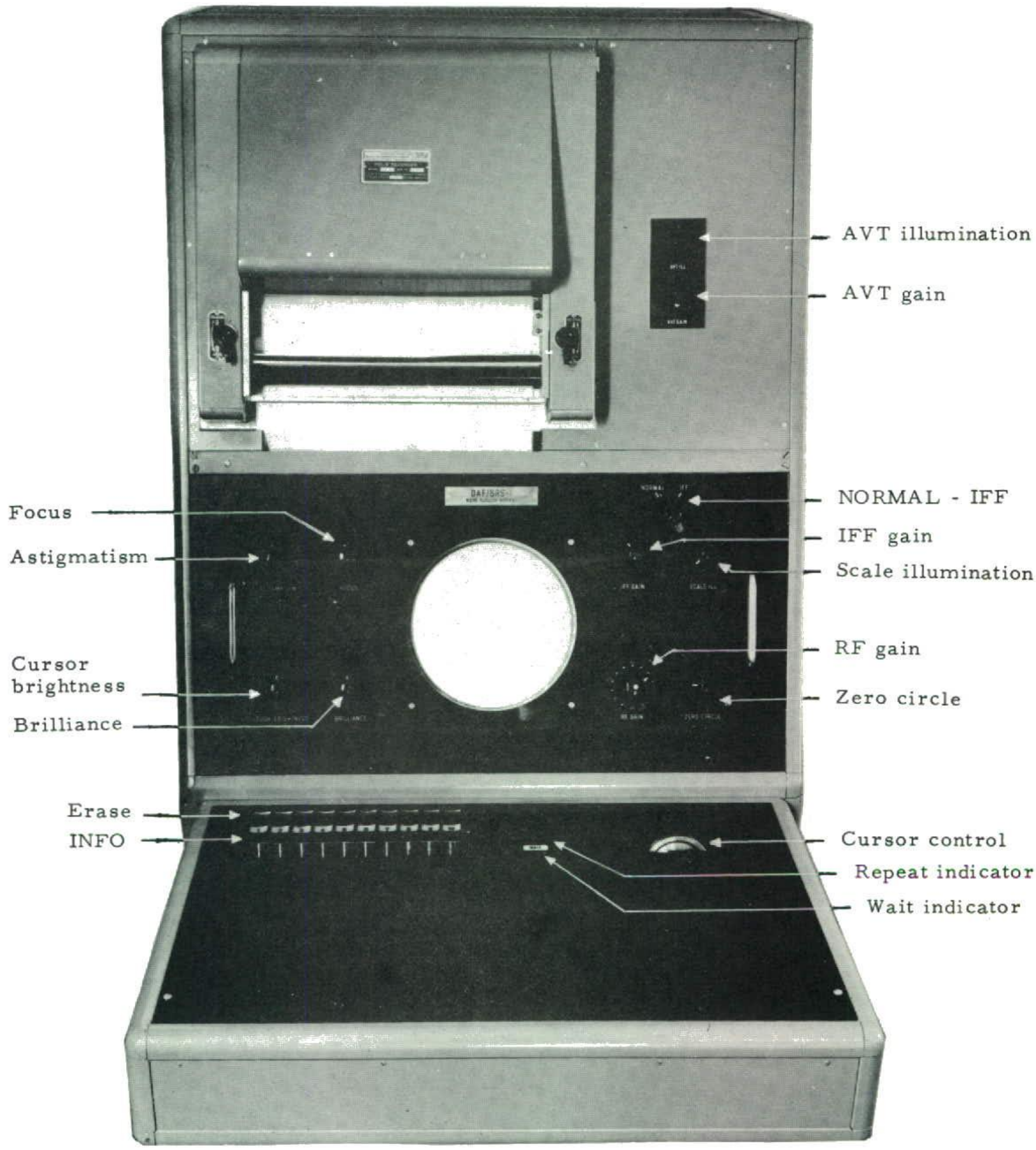


Figure 3.102 SRS operator controls

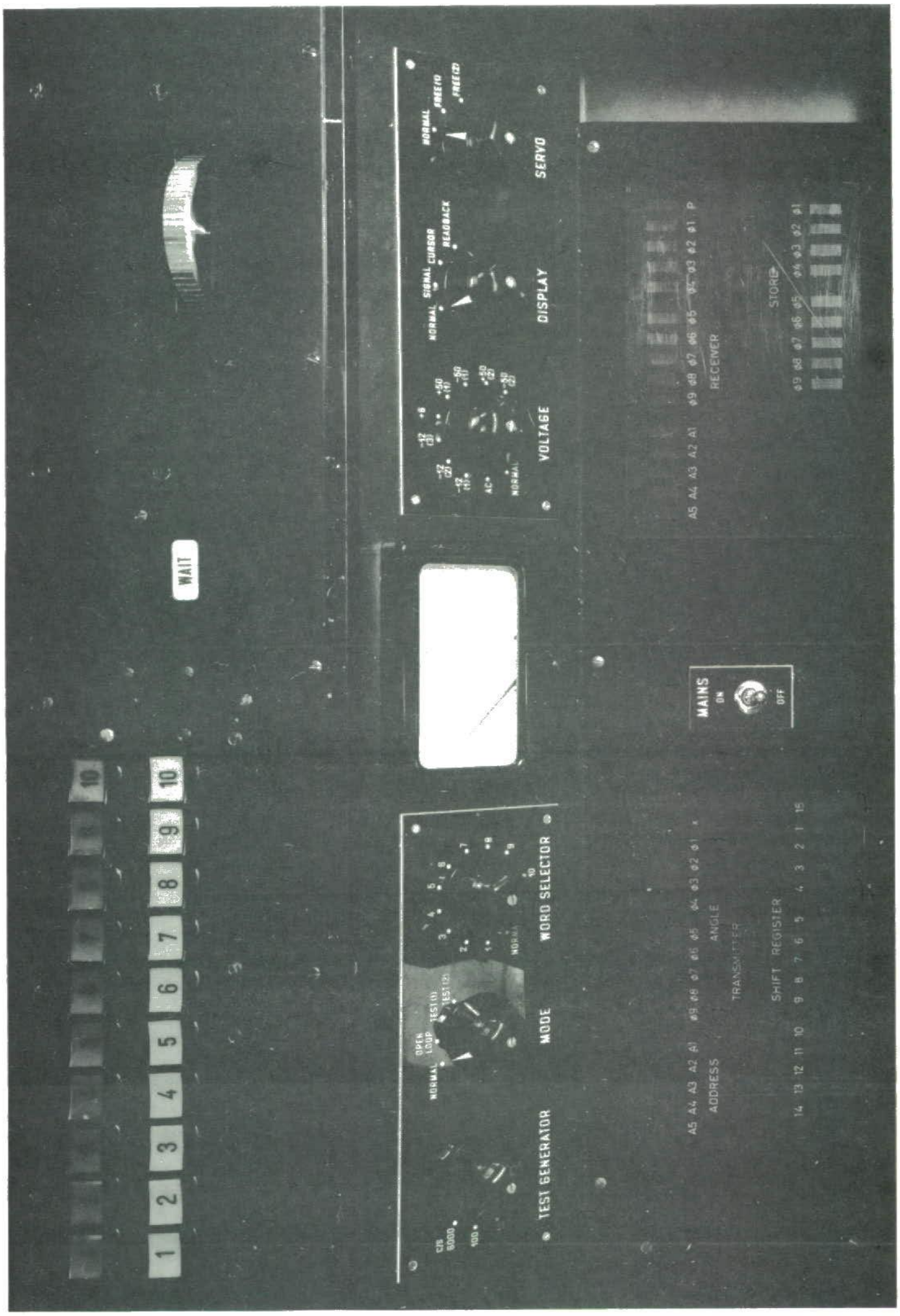
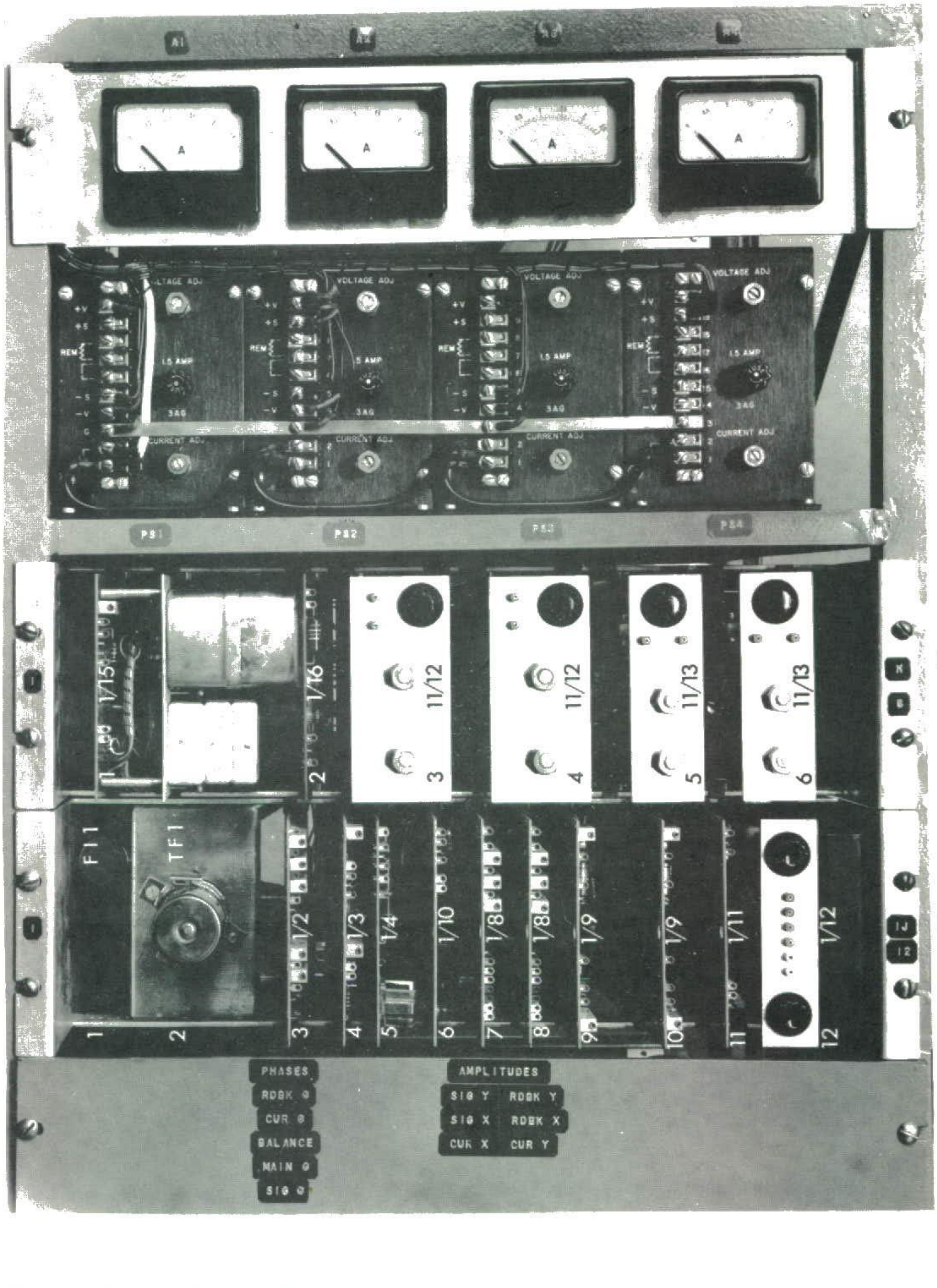


Figure 3.103 SRS control panel



Panel K

Panel IJ

Figure 3.104 SRS right hand door

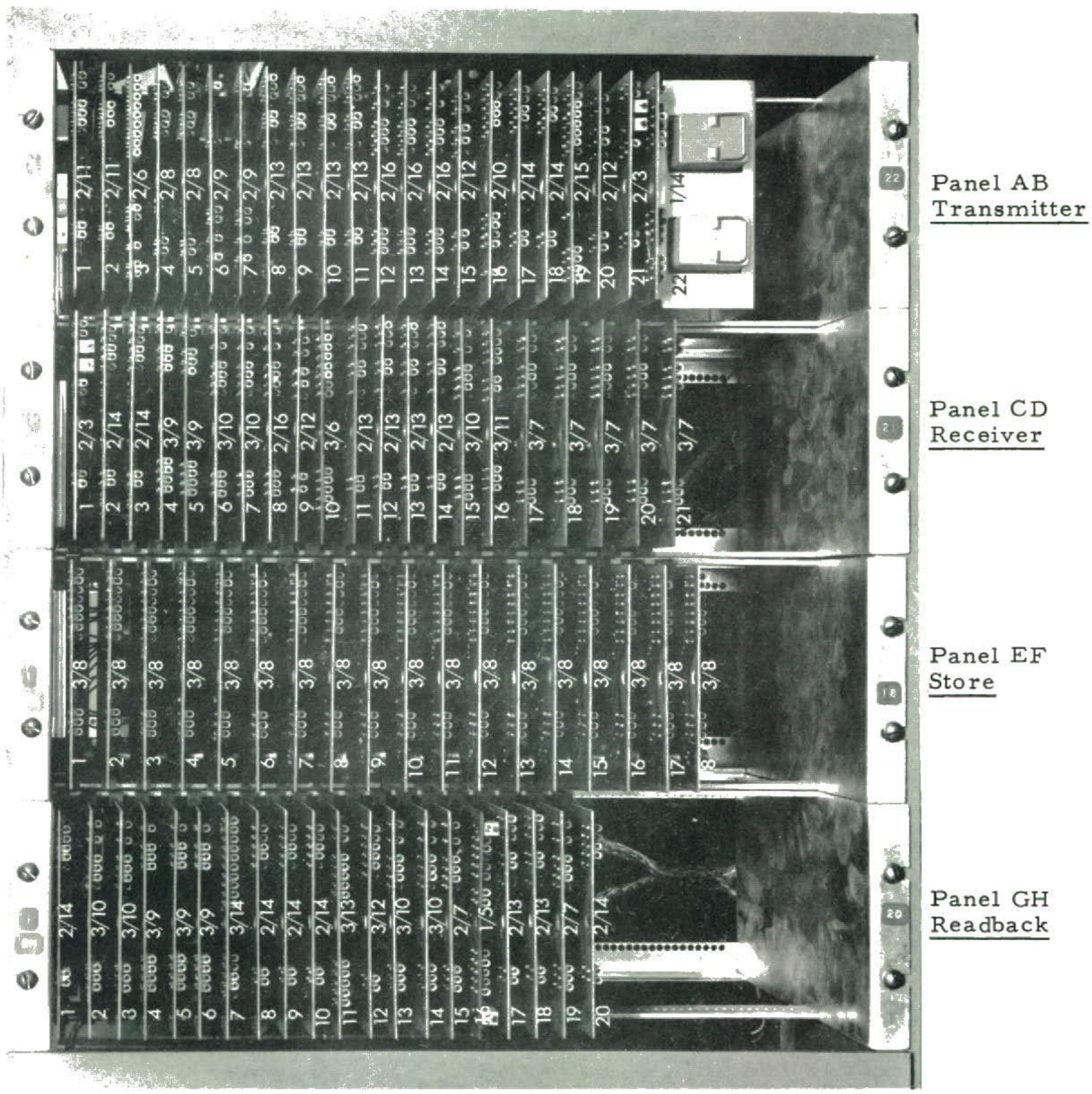


Figure 3.105 SRS left hand door

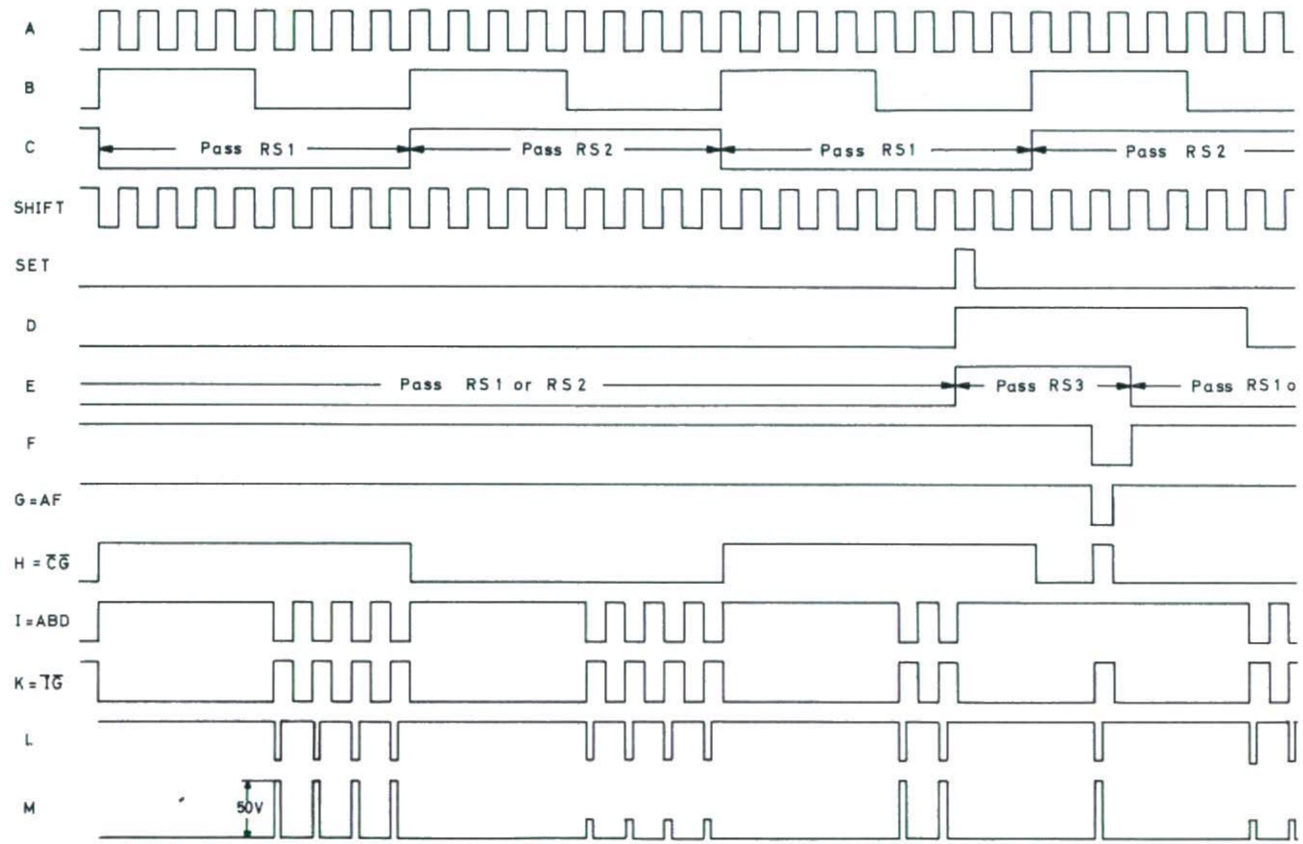


Figure 3.106 SRS display system.

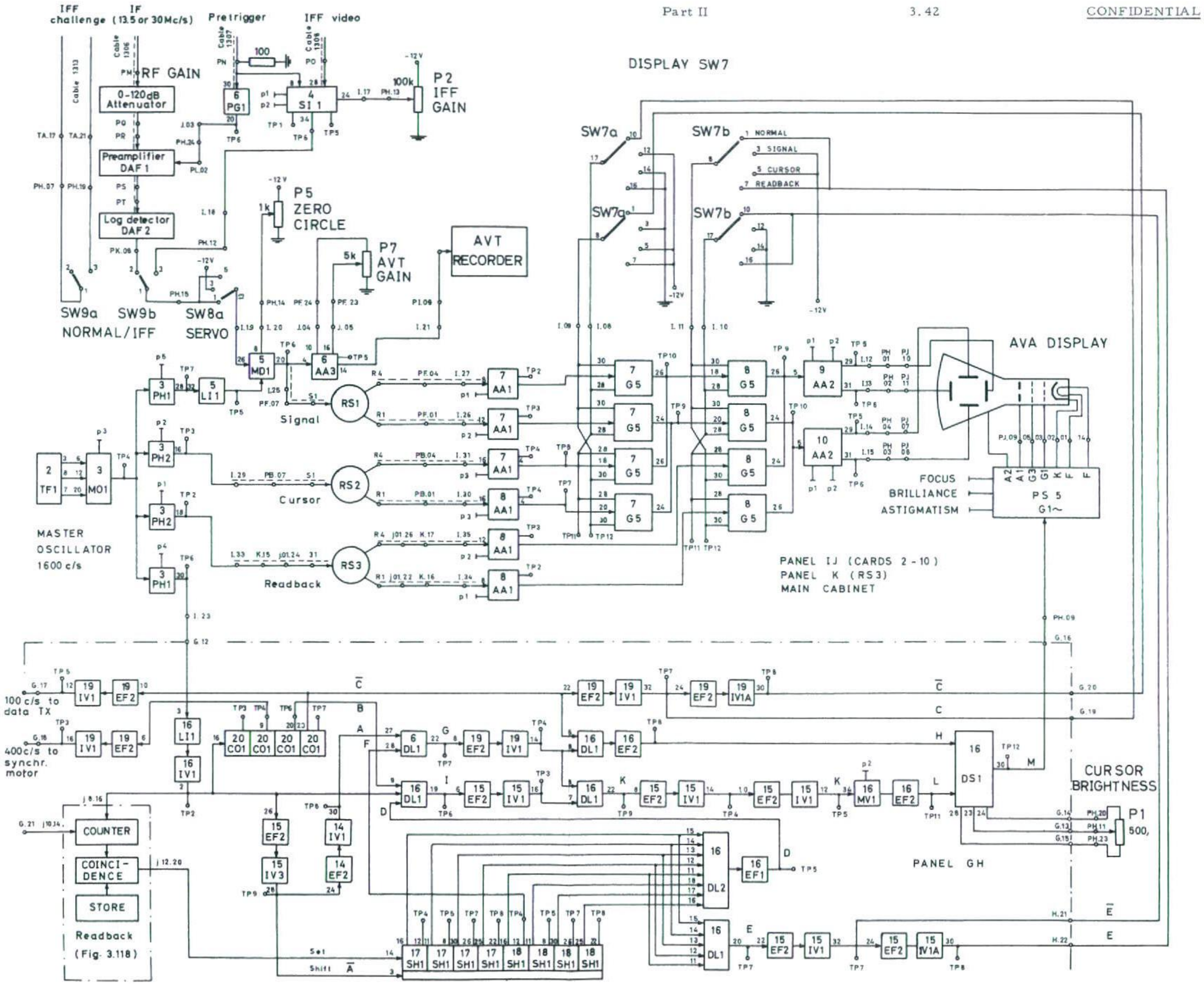


Figure 3.107 SRS display system, block diagram

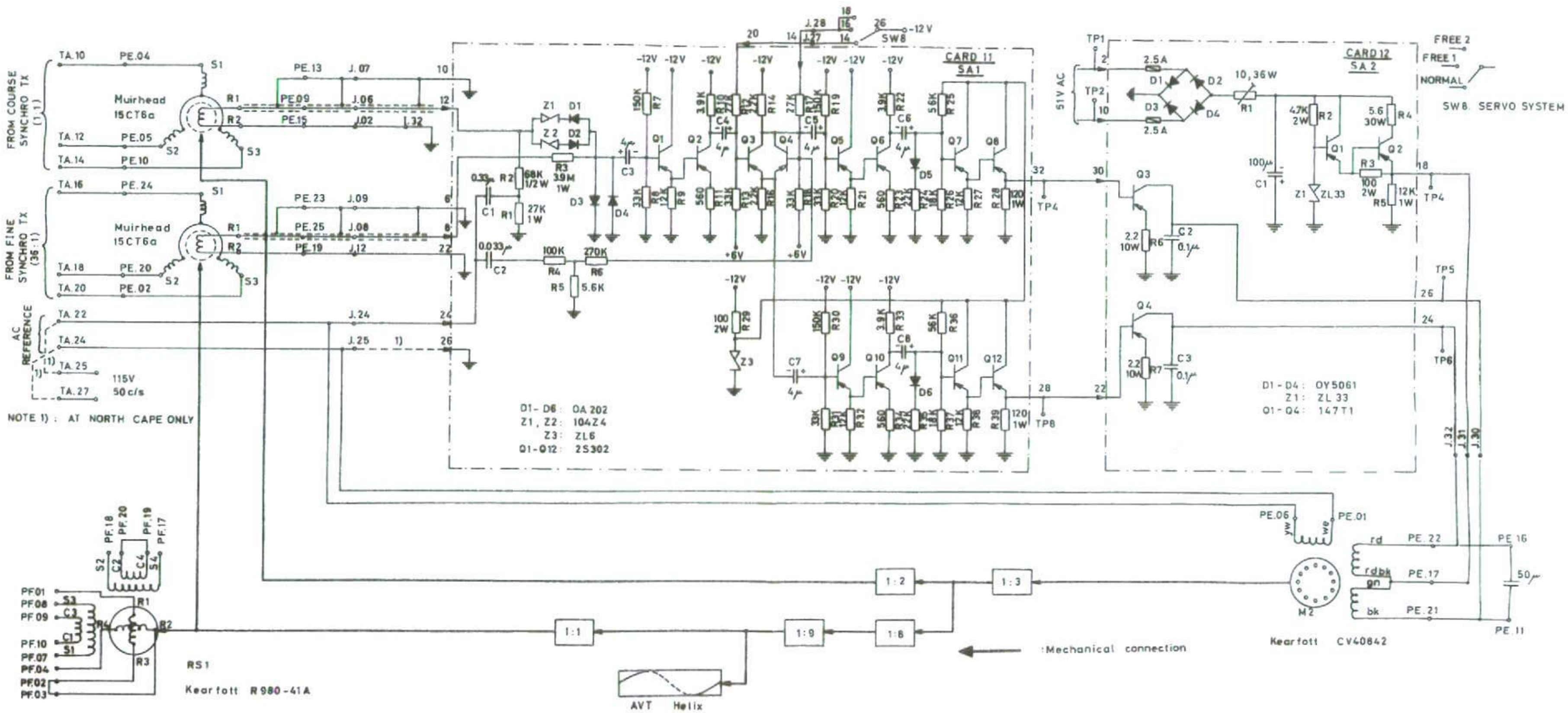


Figure 3.108 SRS servo system

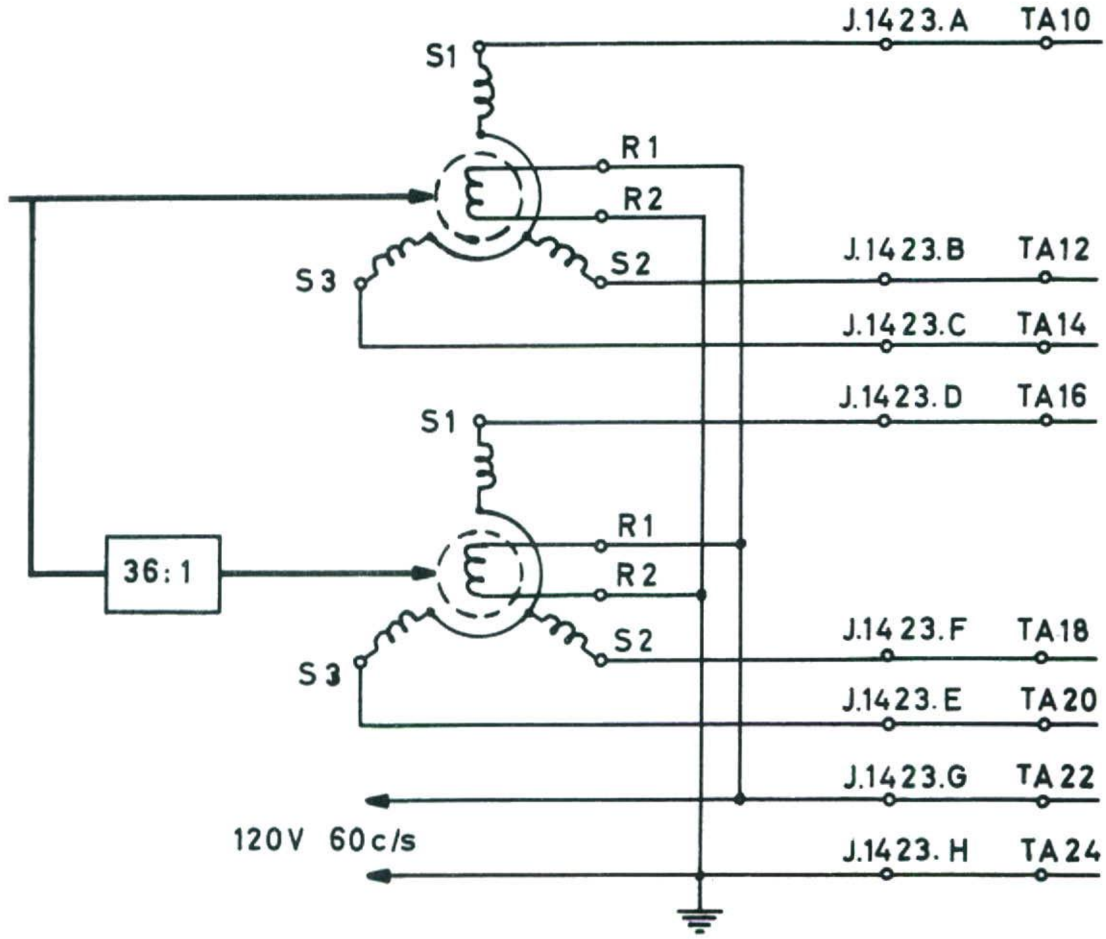


Figure 3.109 AN/FPS-8 servo system

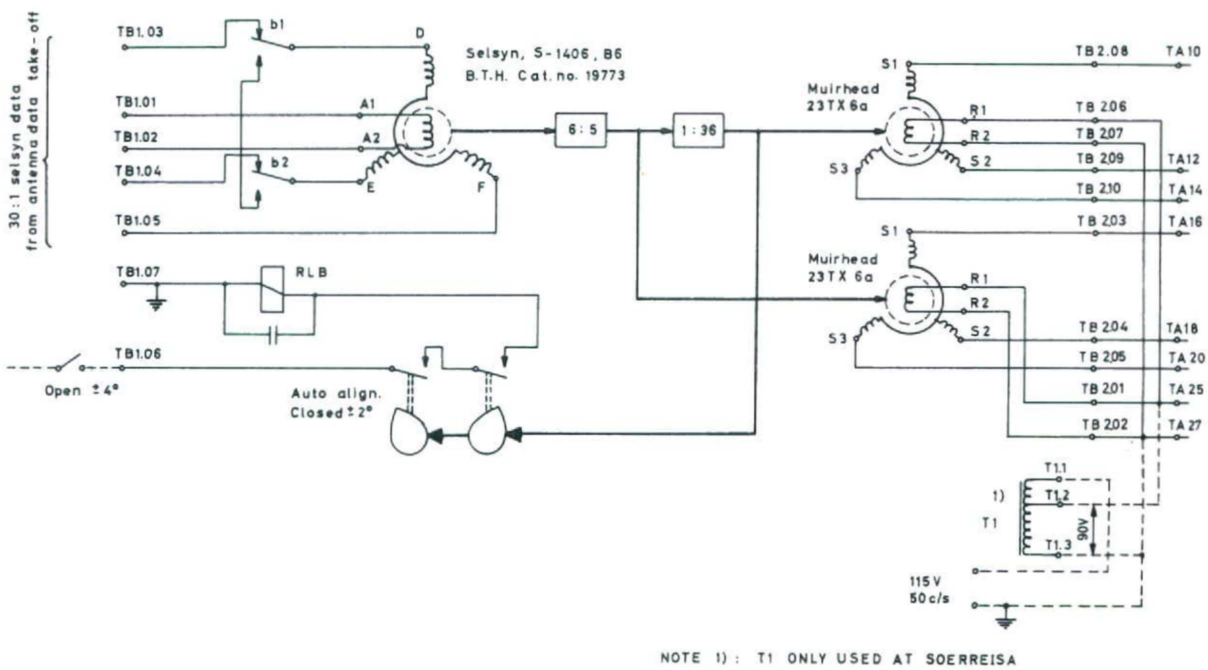


Figure 3.110 Servo system adaptor at S-266 stations

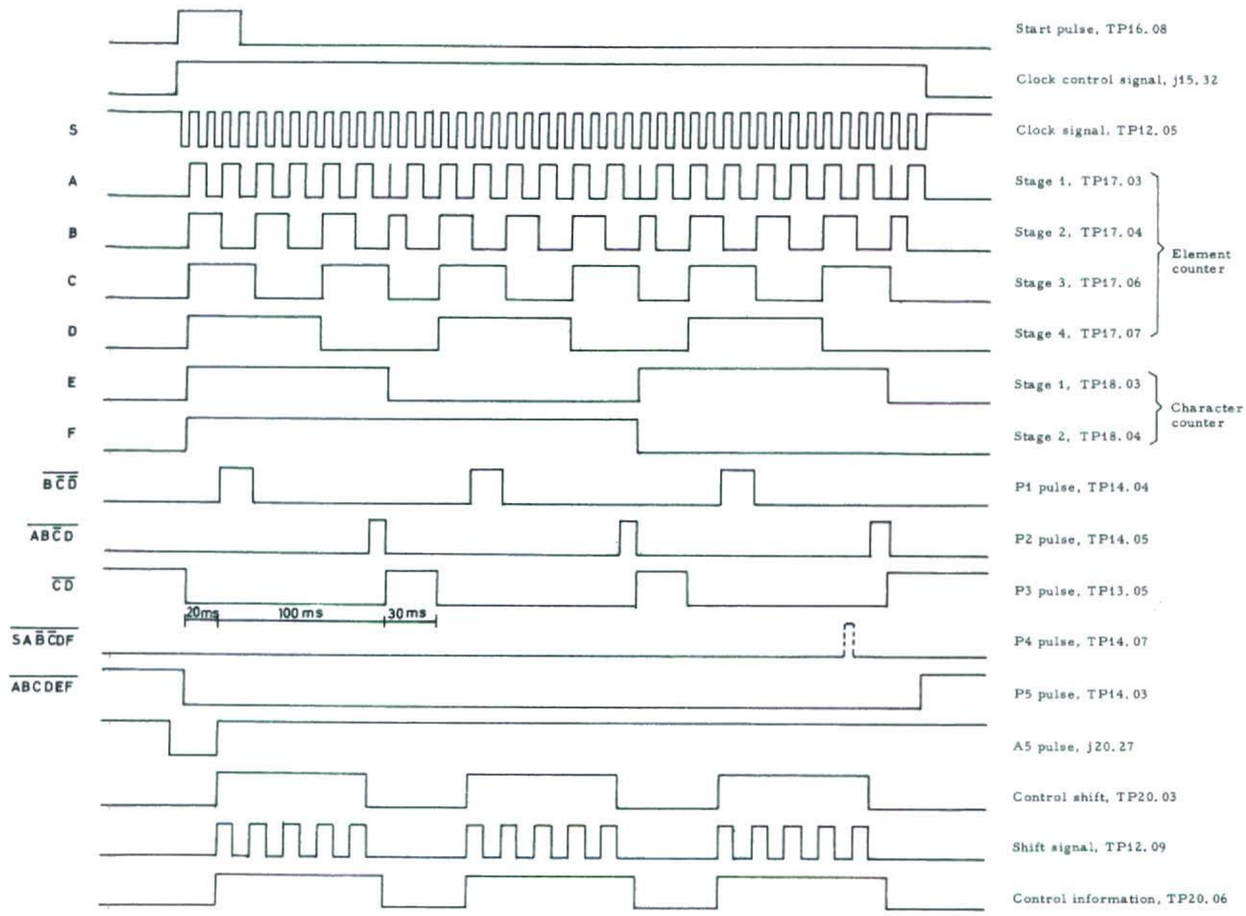


Figure 3.111 SRS data transmitter,
waveforms in pulse sequence generator

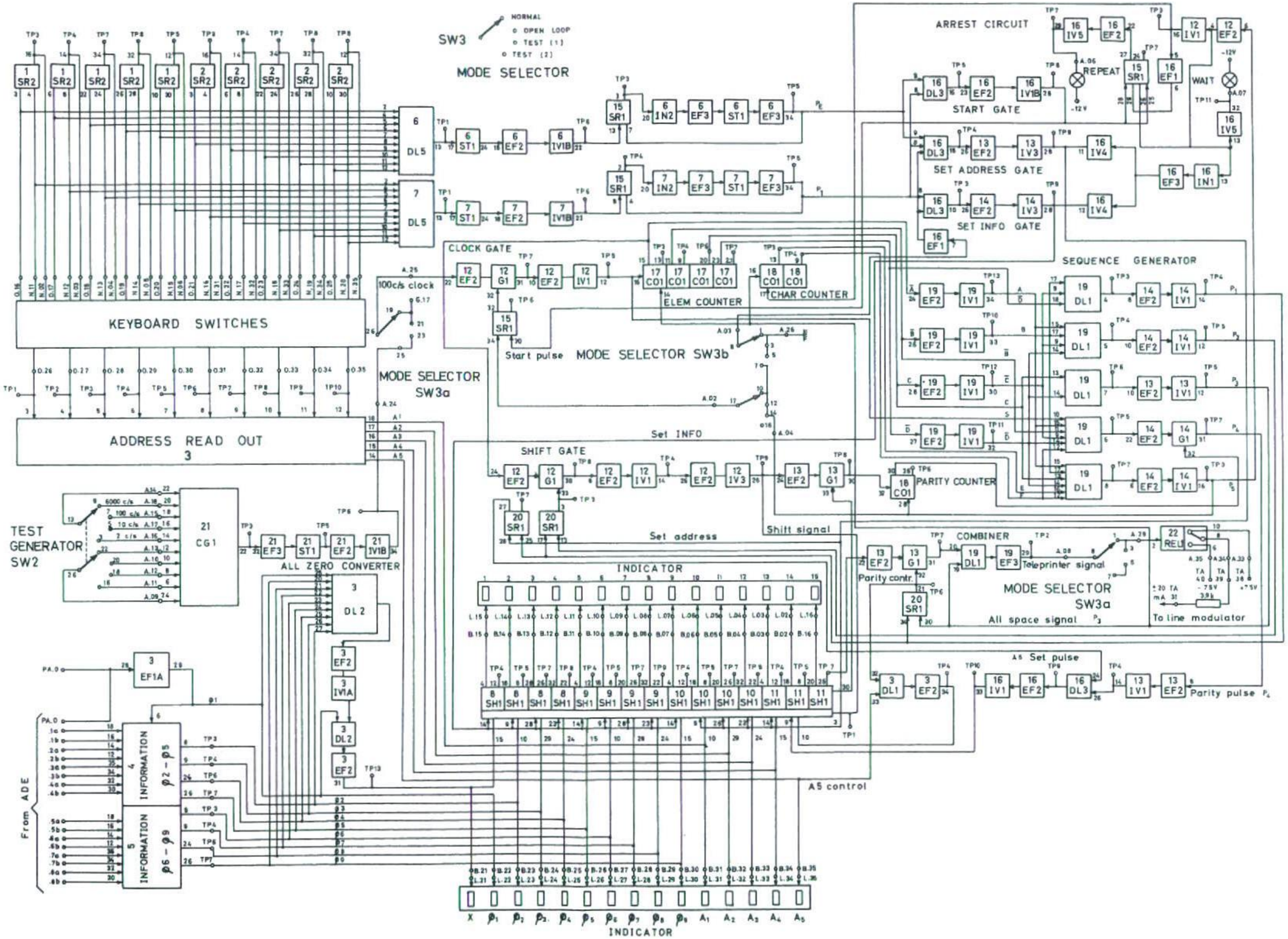


Figure 3.112 SRS data transmitter, block diagram

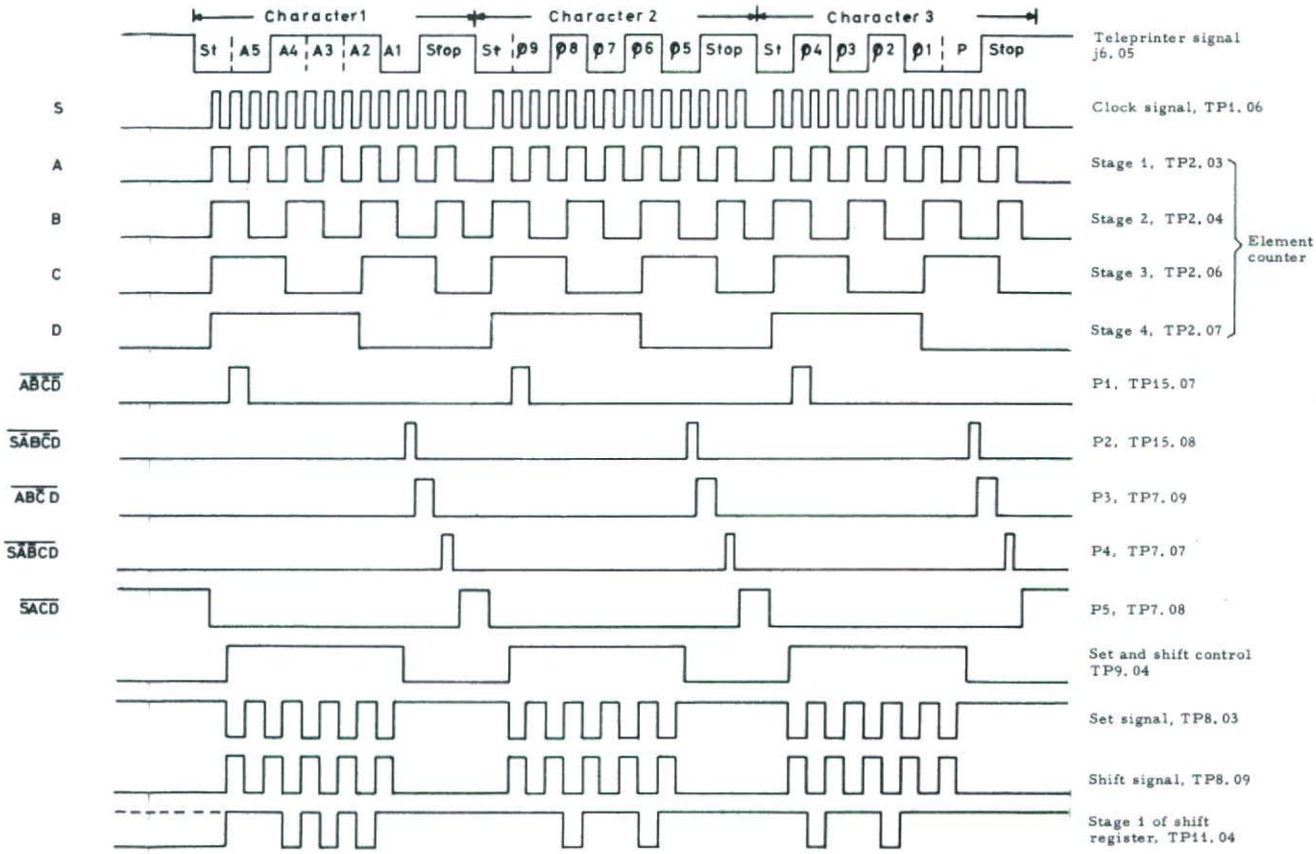


Figure 3.113 SRS data receiver, waveforms in pulse sequence control unit

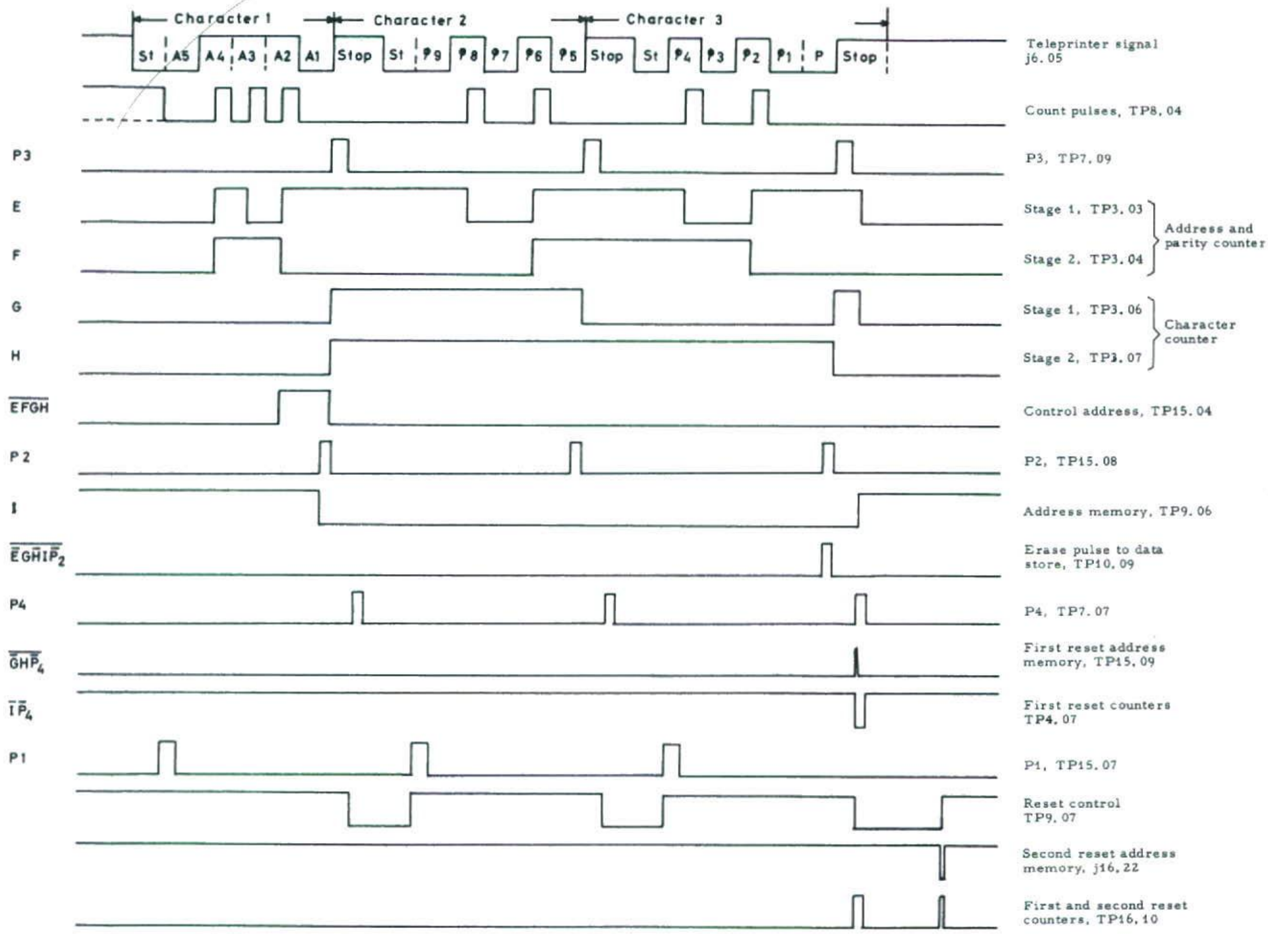


Figure 3.114 SRS data receiver, waveforms in address and parity checking circuits

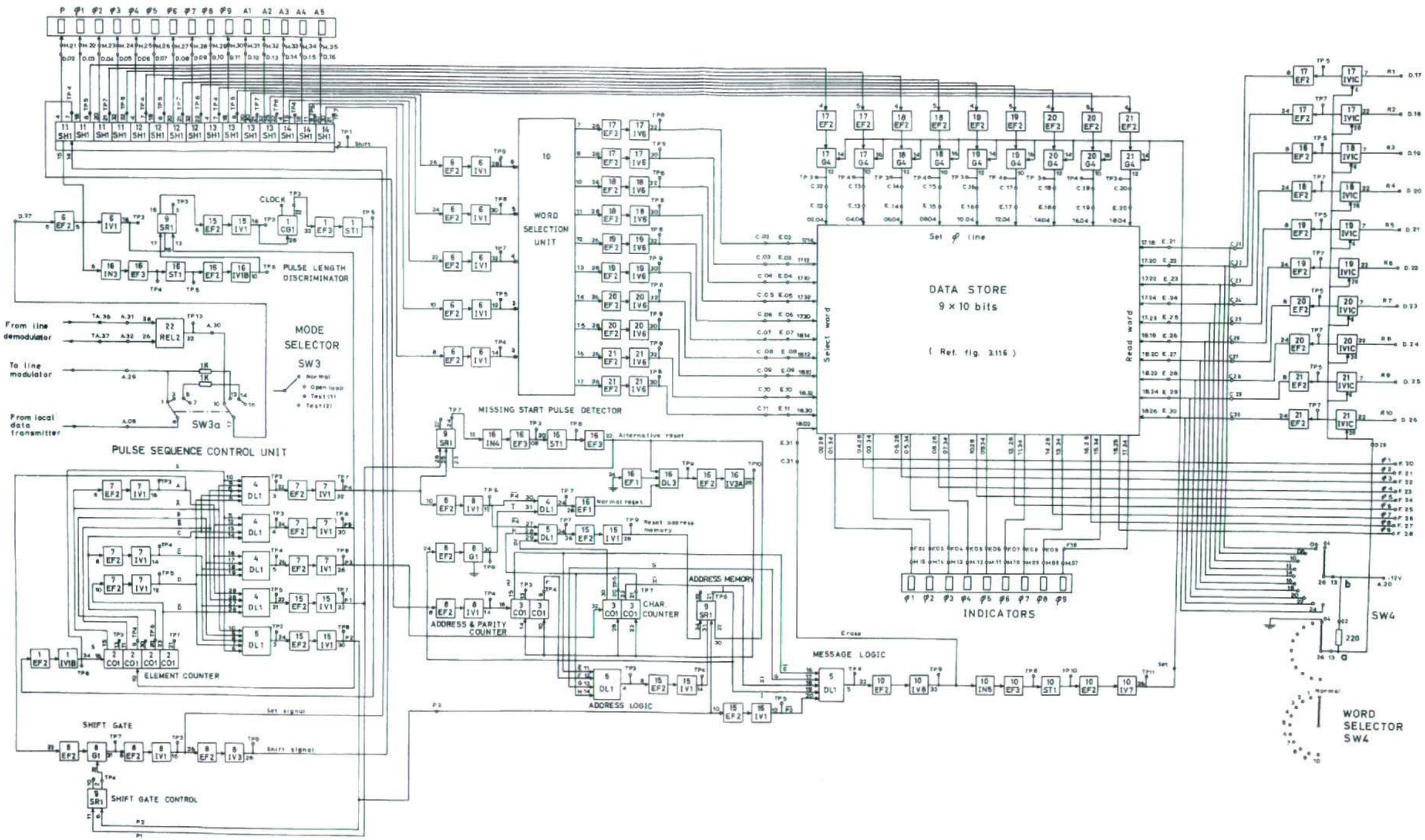


Figure 3.115 SRS data receiver, block diagram

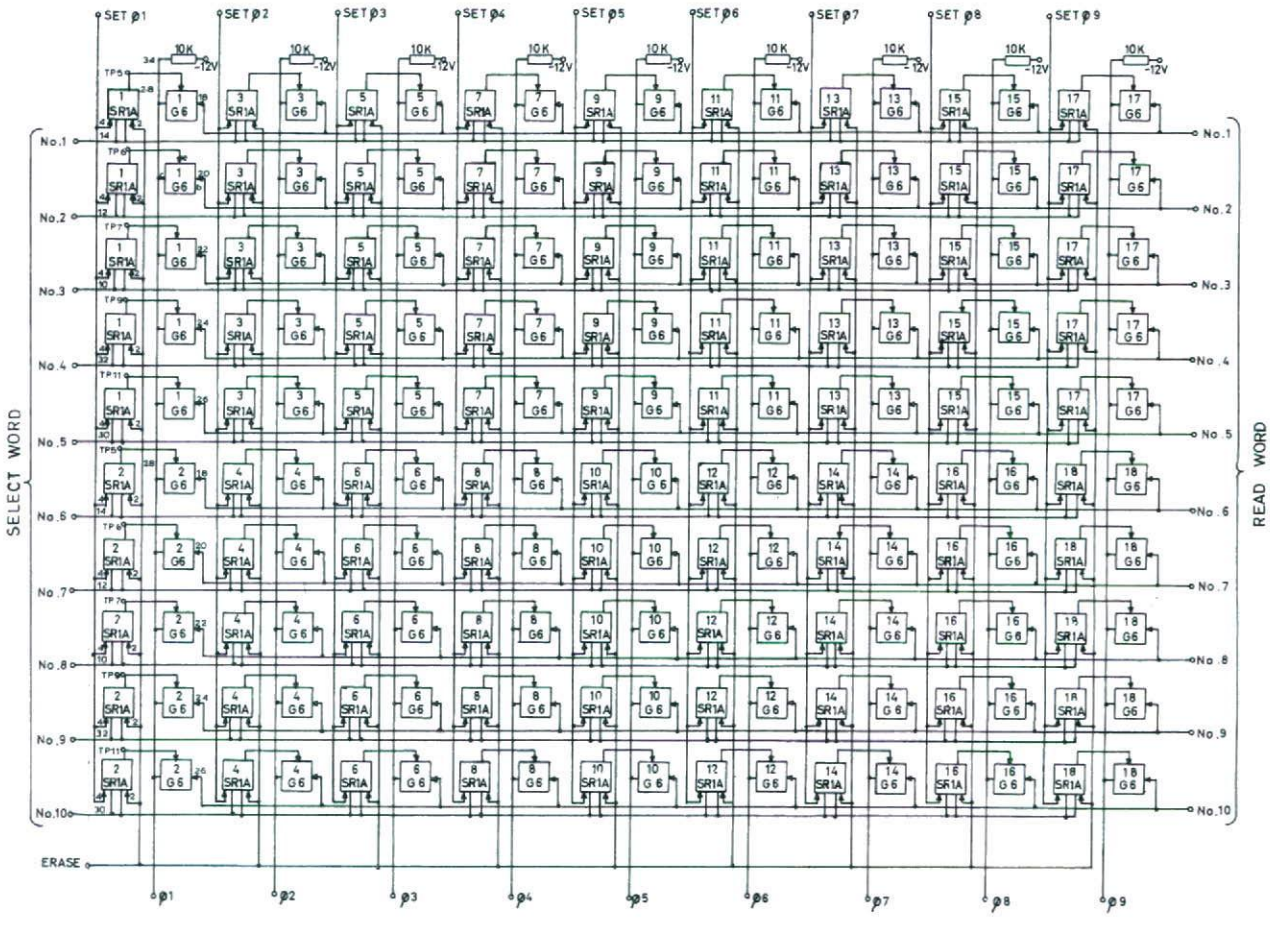


Figure 3.116 SRS data store, block diagram

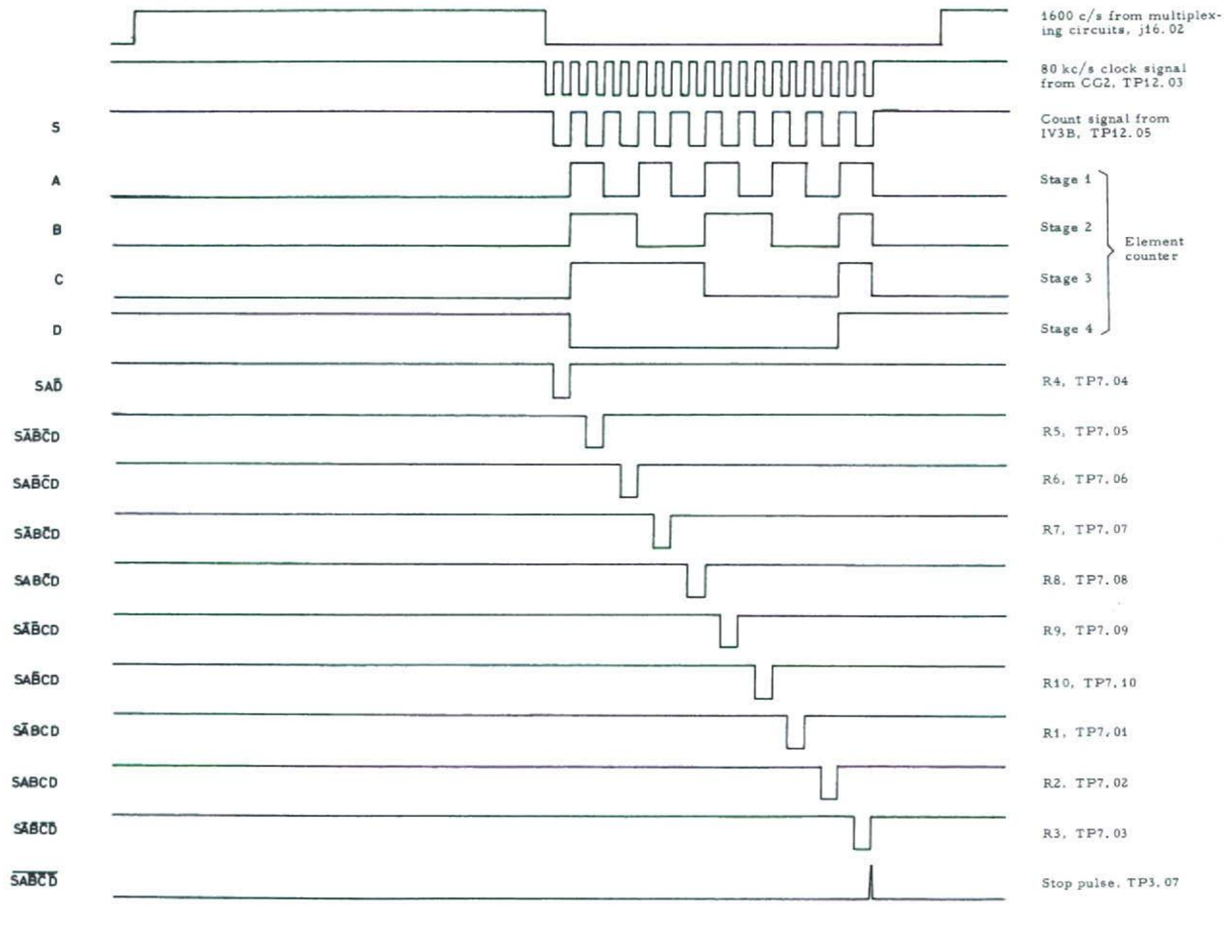


Figure 3.117 SRS readback system, waveforms

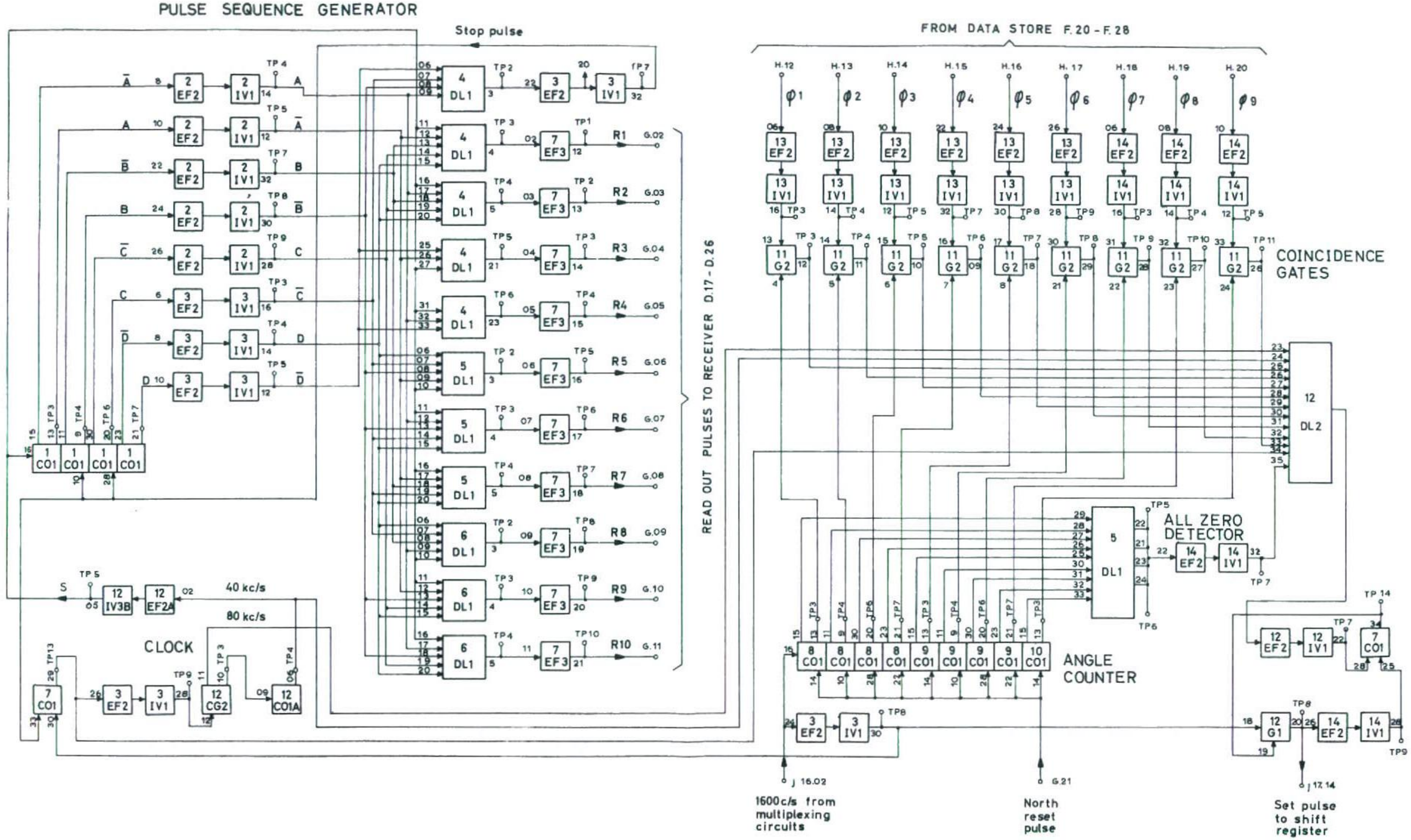


Figure 3.118 SRS readback system, block diagram

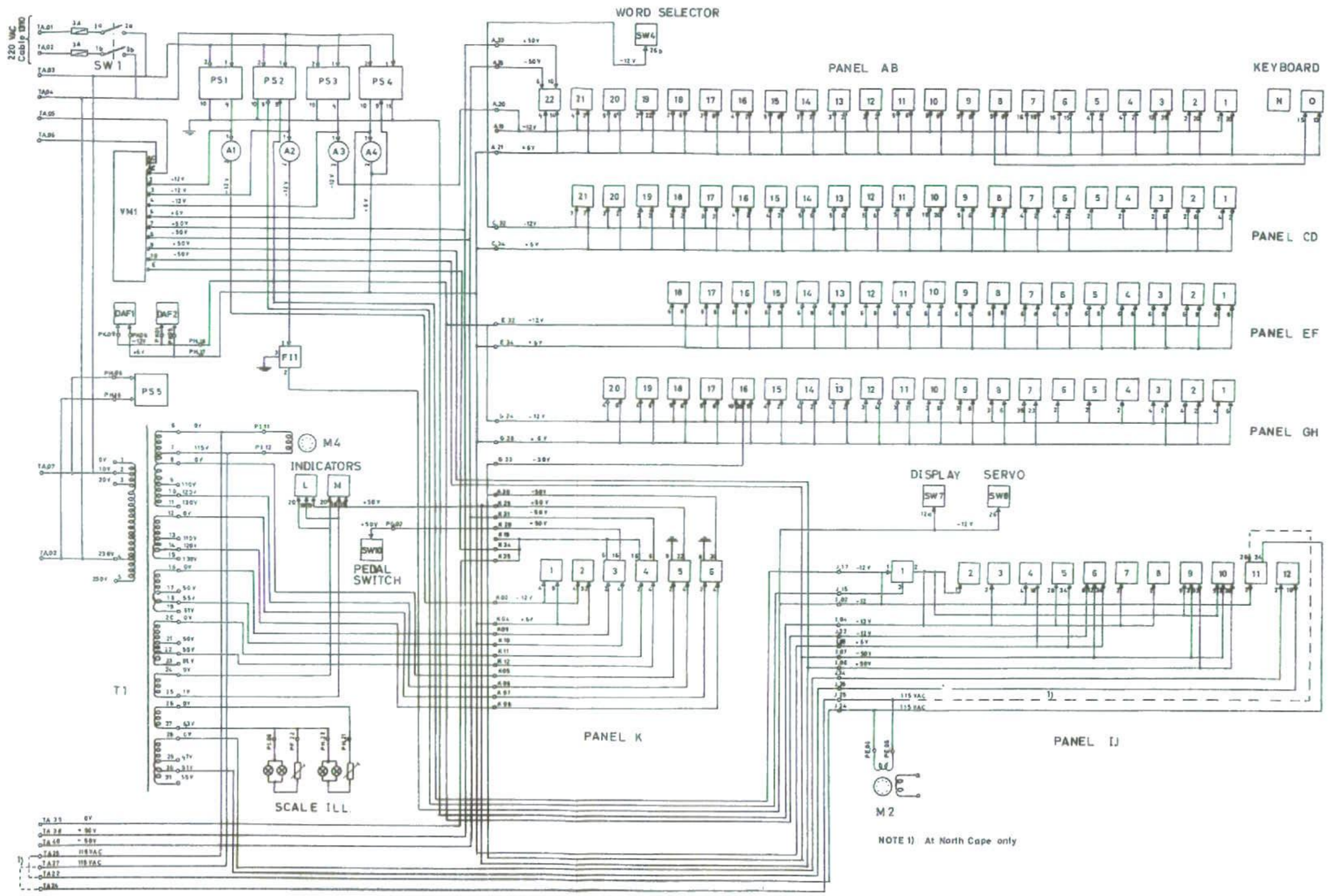


Figure 3.119 SRS power supply system

4 CENTRAL STROBE RECEIVING STATION CRS-1

The main principles of the central strobe receiving equipment have been outlined in Part I Section 2.3, and will not be repeated here. It is also assumed that the reader is familiar with Part II Chapters 1 - 2.

For the location of the various circuits and controls reference is made to Figures 4.101 - 4.104 at the end of this chapter.

4.1 Strobe receivers and stores

A block diagram of the receivers and stores at the CSR station is shown in Figure 4.105. Receiver A receives messages from the local SRS while the receivers B, C and D receive angle messages from three remote strobe reporting stations. The receiver and store panels are in most respects identical to the corresponding panels in an SRS, and reference is given to the description in Section 3.4. Some minor modifications which have been introduced are discussed below.

4.1.1 Receiver input circuits

A relay card type DAF 1/14 which in an SRS is located in the transmitter panel, has been mounted in card position 22 in each of the receiver panels at the CSR. The receiving relay circuits REL 2 receive double current either from the local SRS (receiver A) or from the line demodulators (receivers B, C and D) via the Y plint and terminals j22.26 and j22.28 in each receiver. The REL 1 circuits on the relay card are not employed at the CSR and the A, T and Z connections on the Y plint are therefore unused.

The regenerated teleprinter signals from the REL 2 circuits (j22.32) are fed to the LOCAL RECEIVER switch SW3 as shown. When switch SW3 and the NORMAL-SIMULATOR switches SW5 - SW8 are in the NORMAL positions, the regenerated teleprinter signal (j22.32) from each REL 2 circuit is fed back to the input terminal (j6.06) of the same receiver. When the LOCAL RECEIVER switch is in positions B, C or D the regenerated teleprinter signal from REL 2 in receiver A is connected to the inputs of receiver B, C or D respectively, while the signals received from the line demodulators are disconnected. By this arrangement all the receivers at the CSR may be tested locally by feeding test messages from the local SRS to the input of the various receivers.

By means of the NORMAL-SIMULATOR switches SW5 - SW8 the input signals to the receivers may be taken either via the LOCAL RECEIVER switch or from a tape simulator, a description of which is given in Section 4.4.

The input regenerated signals (j6.06) are treated by the receivers as described in Section 3.4, and the angle information is transferred to the data stores. All connections between receivers and stores are unmodified and will therefore not be described here.

4.1.2 Read-out control circuits

All words of stores A - D may be read out in sequence by means of time multiplexed read pulses R1 - R10 and station selecting pulses SA - SD supplied from a read-out unit. The store words may also be selected manually by means of STATION SELECTOR switch SW1 and WORD SELECTOR switch SW2.

When the STATION SELECTOR switch is in the NORMAL position, the station selecting pulses SA - SD are distributed to the control terminals j21.20 of the four receivers via the switch segments SW1b and SW1c as shown. The ten read pulses R1 - R10 are fed in parallel to the read-out control circuits of all receivers. The WORD SELECTOR switch is floating and may therefore be regarded as disconnected from the input read lines.

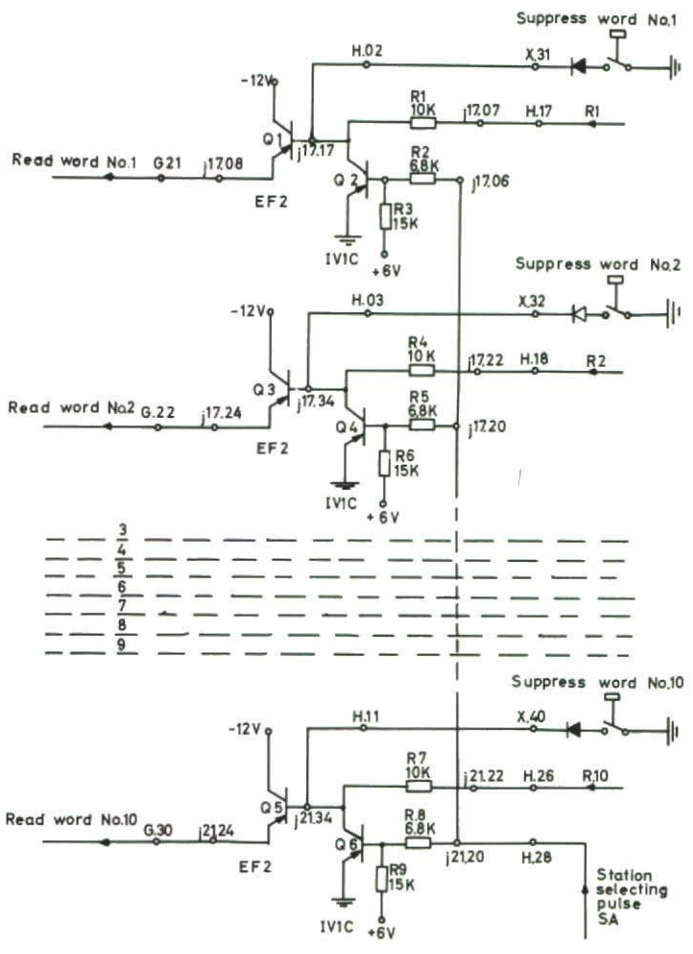


Figure 4.1 Read-out control circuit for receiver A

A detailed diagram of the read-out control circuits in receiver A is shown in Figure 4.1. Assume that station A has been selected for readout. Station selecting pulse SA is then at ground potential (0 V) while the three other station selecting pulses SB - SD are negative. Since control terminal j21.20 of receiver A is grounded, the transistors in the IV1C circuits are all cut off and may be regarded as disconnected from their collector loads. The readout pulses R1 - R10 are then transferred to the read lines of store A via the 10 kohm series resistors and the emitter followers EF2.

When store B, C or D has been selected for readout, station selecting pulse SA is negative and the transistors of the IV1C circuits are saturated. The input terminals of the emitter followers EF2 are thereby grounded and the read pulses R1 - R10 are inhibited.

During normal operation the four stores A - D are selected in turn by the station selecting pulses SA - SD and the contents of the 40 store words are read out in time sequence. As shown in Figure 4.105 output $\varphi 1$ - $\varphi 9$ lines from the four stores have been strapped together on card plugs F, J, N and R. In stores A, B and C the common collector load of the G6 gates, which are located on cards 1, 3, 5 ... 17, have been disconnected (ref Figure 3.116) while store D is unmodified. All forty G6 gates for a given φ digit therefore share a common collector resistor. The binary angles read out from the stores are presented in sequence to the input of a sine/cosine converter as shown.

4.1.3 Strobe erasure panel

A strobe can be selectively blanked by suppression of the normal readout of the store word. This is obtained by grounding of the collector of appropriate inverter IV1C, as indicated in Figure 4.1.

A selective strobe erasure panel is located at the triangulation table. The panel contains one row of twelve push-buttons for each strobe reporting station (48 push-buttons altogether). Figure 4.2 shows the circuit diagram for the station A erasure controls. All switches are two pole double throw switches. Each switch has a built-in lamp which is weakly illuminated in the unoperated position, and more strongly illuminated when the switch is operated.

Switches sw1 - sw10 are engaged when pushed once and disengaged when pushed twice. Switches sw11 - sw12 are mechanically interlocked such that if one switch is slightly pressed the other switch is released.

If sw11 and sw12 are both unoperated, switches sw1 - sw10 independently control the blanking of the ten store A words. When for example sw1 is unoperated, diode D1 is floating, and transistor Q2 in Figure 4.1 is active. If sw1 is engaged, diode D1 shorts the Q2 collector to ground. If sw11 is operated, switches sw1 - sw10 are overruled whether they are engaged or not, as the common earth return is removed, and all store A words are displayed. If sw12 is operated, all diodes D1 - D10 will have their anode earthed whether sw1 - sw10 are operated or not, and all store A words are blanked.

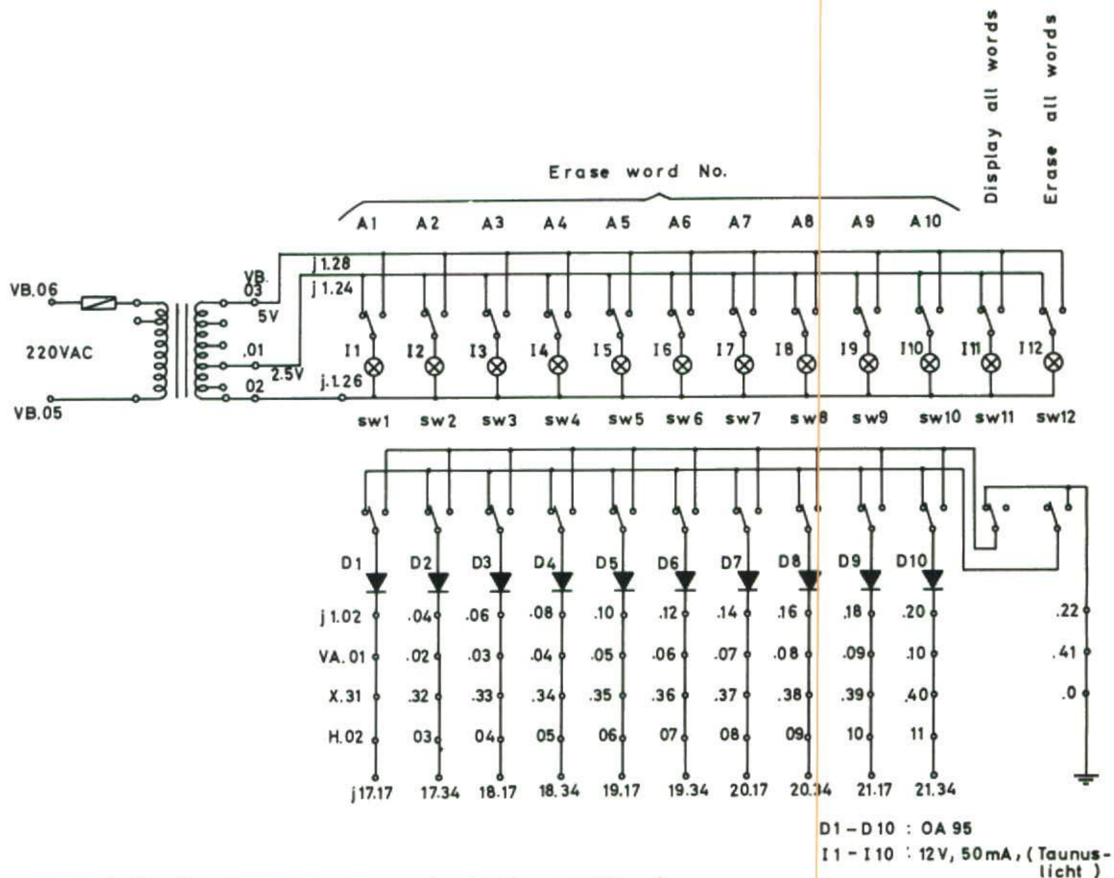


Figure 4.2 Strobe erasure controls for station A

4.1.4 Manual readout

The content of all store words may for test purposes be read out manually by the STATION SELECTOR and WORD SELECTOR switches, the read out angle digits $\varphi 1$ - $\varphi 9$ being presented on indicator card U on the control panel (ref Figure 4.105). When the STATION SELECTOR switch is turned out from the NORMAL position the read pulses R1 - R10 from the readout units are inhibited, the inhibit terminal of the readout unit being grounded from contact 13 on SW1a as shown. At the same time -12 V is fed to the WORD SELECTOR switch via contact 26 on SW1a. When the STATION SELECTOR is turned to the A position, the station selection terminal j21.20 of receiver A is grounded via terminal 13 of SW1b while the corresponding terminals of the other receivers are connected to -12 V via the SW1b and SW1c segments. The ten words of the A store may then be selected for manual readout by turning the WORD SELECTOR to any of its ten positions. When the STATION SELECTOR is turned to the B position, station selection terminal j21.20 of receiver B is grounded, the corresponding terminals of receivers A, C and B being negative. Any word of the B store may then be selected for manual readout, and so forth.

4.2 Readout unit and coordinate selection

The readout unit supplies the readout control circuits of receivers A - D with readout pulses R1 - R10 and station selecting pulses SA - SD while the Xo, Yo origin coordinates corresponding to the geographical position of the four participating stations are presented to the display system by the coordinate selecting circuits. The origin coordinates are shifted in synchronism with the station selecting pulses but in a slightly different phase as will be made clear below. Blanking pulses for strobes and origins to the display system are also provided by the readout unit.

The readout unit and coordinate selecting circuits are located on cards 1 - 15 in the AB panel. The description is given with reference to the diagram of waveform Figure 4.106 and the block diagram Figure 4.107.

4.2.1 Pulse sequence generator

The readout unit receives positive SYNC SWEEP, "40 nm" and STOP LINE pulses from the main radar display system via the Z plint as shown. The pulses, of amplitude 1 - 2 V and duration 4 - 10 µs, are amplified in pulse amplifiers PA1, as shown in Figure 4.3. When a positive pulse is received on the input the grounded base circuit transistor is saturated and a positive pulse of 12 V amplitude is obtained from the output.

The amplified "40 nm" pulses are frequency divided in a counter stage CO1 on card 7 while the amplified SYNC SWEEP pulses are fed to the reset terminal j7.30 of the same counter (ref Figure 4.107). The CO1 stage is reset by the very first SYNC SWEEP pulse received and will thereafter remain in step with this signal. The frequency divided waveform from CO1 (TP7.13) is amplified and inverted by the circuits EF2 - IV1 and the output from IV1 (TP3.16) is fed as a clock signal to a four stage counter. The amplified counter waveforms together with the clock signal S are connected to the input terminals of eleven diode logics DL1 acting as AND gates for negative signals. A time sequence of ten read pulses R1 - R10 is thus obtained. The pulses are fed to the readout control circuits of the four receivers as described in Section 4.1.2. A reset pulse obtained from the lower DL1 circuit in the block diagram (TP4.02) is applied to the reset terminals of stages 2 and 3 of the counter via the EF2 - IV1 circuits. For detailed description reference is made to the pulse sequence generator described in Section 3.5.1, which is identical apart from the difference in frequency.

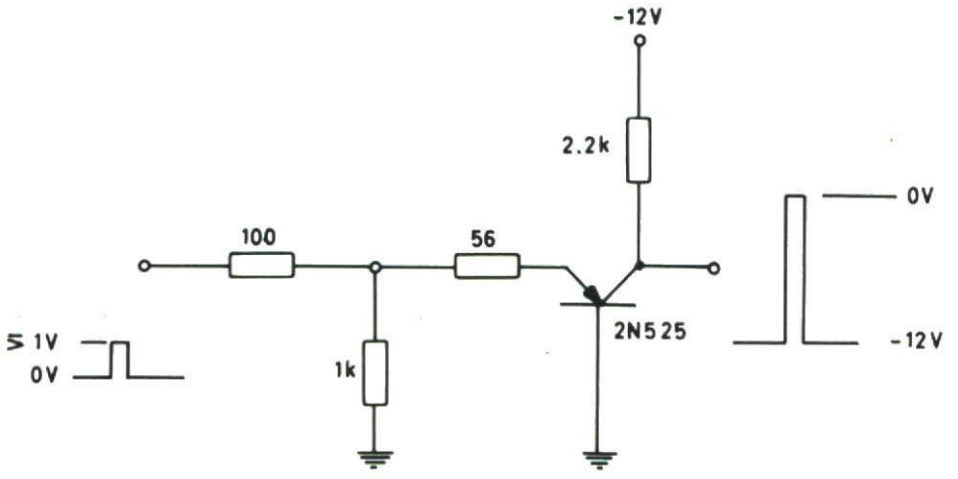


Figure 4.3 Pulse amplifier PA1

When the STATION SELECTOR switch SW1 on the control panel is turned out from its NORMAL position the input terminal of the four stage counter (j1.16) is grounded and the clock signal S is inhibited. The R1 - R10 output terminals of the pulse sequence generator are then grounded and the store words may be read out manually by operating the WORD SELECTOR switch as described in Section 4.1.4.

The amplified STOP LINE pulse (j13.23) which arrives at the end of the display of each triangulation strobe, is further amplified by EF2 - IV1 and EF2 - G1 as shown. The G1 circuit is here used as an inverter. The negative pulse obtained from IV1 (TP11.05) is applied as a sampling pulse to a blanking circuit DL2 in the CD panel while the positive pulse from G1 (TP11.07) is fed as a start pulse to the pulse generator of the sine/cosine converter via the NORMAL-MANUAL TRIGGER switch on the control panel. The application of these pulses is further described in Section 4.3.

4.2.2 Station selection unit

The R10 pulse from the pulse sequence generator is amplified by two EF2 - IV1 circuits, and the negative output pulse (TP3.09) is fed to the input terminal (j8.16) of a station selection counter, counting the positive edges of the R10 pulses. The output waveforms from the counter (E, $\overline{E}$, F and $\overline{F}$) are connected to the inputs of four DL1 circuits acting as AND-gates for negative signals. If for example $\overline{E}$ and $\overline{F}$ are both negative, a negative waveform is obtained from the upper DL1 circuit (TP4.06). This waveform is further amplified and inverted by the circuits EF2 - IV1 - EF2, and the positive output pulse SA is fed to the readout control circuits of receiver A (ref Figure 4.1). The ten words of the A store are then read out by the read pulses R1 - R10 (ref Figure 4.105).

When word No 10 of store A has been read out, the station selection counter receives a count from the R10 pulse as described above, and now the counter outputs E and $\overline{F}$ become negative. A positive SB pulse is then generated and store B is selected for readout. The station selection pulses SC and SD are generated in a similar manner and the information stored by stores C and D is read out.

During each radar sweep four store words are read out (ref Figure 4.106), and the time taken for a complete readout cycle (forty words) is thus 45 ms. Each angle message is therefore sampled approximately 22 times per second, and the triangulation strobes are displayed essentially without flickering.

4.2.3 Origin coordinates selecting circuits

The read pulse R2 is amplified and inverted by the circuits EF2 - IV1, and the positive output pulse (TP11.04) is fed to a coordinate selection counter. The counter waveforms (G, $\overline{G}$, H and $\overline{H}$) together with P6 pulses derived from the sine/cosine converter are fed to the input terminals of four DL1 circuits as shown. The P6 pulse arrives approximately 150 µs after a STOP LINE pulse.

If for example the waveforms $\overline{G}$ and $\overline{H}$ are both negative, the negative P6 pulses are permitted through the upper DL1 circuit (TP5.07) and are further amplified and inverted by EF2 - IV1. The first positive output pulse from IV1 (TP9.05) which has the logic designation $\overline{\overline{G}\,\overline{H}\,P6}$ sets the upper SR3 circuit controlling the station A coordinates and resets the lower SR3 circuit on the diagram which controls the station D coordinates.

The two G7 gates controlling the coordinates X_A and Y_A are then opened and all other G7 gates closed. When the next R2 pulse is received by the coordinate selection counter the G7 gates controlling the X_B and Y_B coordinates are opened, and so forth. The X and Y coordinates of the four stations are thus read out in a sequence (ref Figure 4.106). The outputs of the gates are amplified by emitter followers EF4 and EF5 as shown, and fed to the display system via the Z plint. In the circuit combination EF4 - EF5 two complementary transistors (pnp and npn) are employed to reduce drift due to temperature effects.

To ensure that the angles read out from for instance the A store are presented as strobes from the A origin, the station selection counter and the coordinate selection counter must be interlocked. When the G and H waveforms of the coordinate selection counter both become negative, a negative pulse is obtained from a DL1 circuit on card 6 (TP6.06) which is amplified and inverted by EF2 - IV1. The positive output pulse from IV1 (TP11.03) is connected to the reset terminals of the station selection counter as shown. The correct phase relationship between the counters is established by the first reset pulse received and the station selection counter is thereafter normally not affected by the reset pulses.

4.2.3.1 Coordinate adjustments

The X and Y coordinates of the four stations may be adjusted by means of potentiometres p1 - p8 on card 13. As shown, the potentiometres are strapped together at one end and connected to the main reference voltage of the display system. The other end of the potentiometres is either grounded or connected to a stabilized -1 V source as shown[1].

As described above, the whole readout cycle is stopped when the STATION SELECTOR switch is turned out from the NORMAL position. It is therefore possible to select the X and Y coordinates of any of the four stations manually by alternating the STATION SELECTOR switch between the NORMAL and "A" positions while the outputs from the SR3 circuits are observed. When the output from the upper SR3 circuit (TP12.03) is negative (-20 V) and the outputs from the other SR3 circuits (TP12.04 - TP12.06) are positive (+20 V), the coordinates of the A station are selected. The coordinates X_A and Y_A may then be measured with a high precision voltmeter at the outputs of the emitter followers EF5 (TP13.02 and TP13.01 respectively). The coordinates are adjusted to their correct values by means of potentiometer p1 and p2 as shown. The selection and adjustment of the other coordinates are done in a similar manner.

For the present reference voltage of 15.347 V, which corresponds to 320 nm on the display, the correct values of the coordinates are indicated in the waveform diagram, Figure 4.106. If the reference voltage is altered the origin coordinate voltage values must be altered proportionally. The coordinates are adjusted with an accuracy better than ± 10 mV, corresponding to a positional error less than ± 0.2 nm.

4.2.4 Blanking circuits

The R2 pulse is amplified and inverted by the circuits EF2 - IV3 and the positive output (TP14.08) is fed as a blanking pulse to the display system via the Z plint. This blanking pulse prevents the display of a minute origin marker (not shown in the diagram) when the coordinates are being switched (ref Figure 4.106).

The blanking of strobes is initiated from a blanking circuit located in the CD panel. Due to the inherent delay due to the data handling in the sine/cosine converter the blanking signal must also be delayed. The set blanking pulse received from the CD panel is therefore connected to the set terminal (j15.14) of the first stage of a shift register as shown. The negative P6 pulses are amplified and inverted by EF2 - IV1 and fed to the shift terminal (j15.03) of the shift register. The delayed negative pulse obtained from the third stage of the shift register is inverted by EF2 - IV3 circuits (TP11.09) and connected to the display system via the Z plint. When the sine/cosine converter is operated in one of the test modes STAR or INCREMENT the set terminal of the shift register is grounded from the SINE TABLE switch SW4 on the control panel and the blanking of strobes is thereby inhibited.

4.3 Sine/cosine converter

The angles stored contain each nine binary angle digits $\varphi 9$ - $\varphi 1$. For display purposes each angle must be converted into analog sine and cosine voltages. This conversion is accomplished by first determining the digital sine and cosine values by means of a pre-wired ferrite matrix with associated circuits, and then converting the digital values into analog voltages through digital-to-analog converters.

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[1] Due to the geographic locations, all origin coordinates are zero or positive. The -1 V is here only used to bias out the base-emitter voltage drop. For geographic locations requiring negative coordinates, a negative reference voltage derived from the main reference voltage must be incorporated.

4.3.1 Basic trigonometric rules

The ferrite matrix holds all sine values for the $2^7 = 128$ possible first quadrant angles. The cosine value of a first quadrant angle may be found by taking the sine of the complement angle. The sine and cosine values of angles outside the first quadrant can be found by means of usual trigonometric rules as given below.

In a binary angle

$$\varphi = (\varphi 9, \varphi 8, \varphi 7, \varphi 6, \varphi 5, \varphi 4, \varphi 3, \varphi 2, \varphi 1)$$

the two most significant bits $\varphi 9$ and $\varphi 8$ represent the quadrant in the following manner:

First quadrant :	$\varphi 9 = 0$,	$\varphi 8 = 0$
Second quadrant :	$\varphi 9 = 0$,	$\varphi 8 = 1$
Third quadrant :	$\varphi 9 = 1$,	$\varphi 8 = 0$
Fourth quadrant :	$\varphi 9 = 1$,	$\varphi 8 = 1$

For data handling reasons, the quadrant information bits $\varphi 9$ and $\varphi 8$ will be designated Q2 and Q1 respectively.

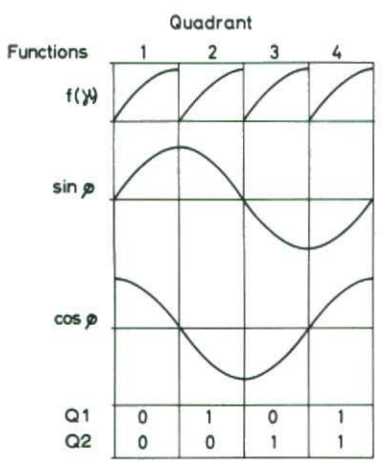
The remaining bits $\varphi 7$ - $\varphi 1$ define the location of the angle within the given quadrant, and will be designated the first quadrant angle, defined by

$$\gamma = (\varphi 7, \varphi 6, \varphi 5, \varphi 4, \varphi 3, \varphi 2, \varphi 1)$$

A nine bit angle φ is therefore given by

$$\varphi = (Q2, Q1, \gamma)$$

The digital trigonometric rules can then be laid down as shown in Figure 4.4 where $f(\gamma)$ is the matrix function.



$$\sin \varphi = (\overline{Q1} \cdot \overline{Q2})\, f(\gamma) - (\overline{Q1} \cdot Q2)\, f(\gamma) + (Q1 \cdot \overline{Q2})\, f(90^{\circ} - \gamma) - (Q1 \cdot Q2)\, f(90^{\circ} - \gamma)$$

$$\cos \varphi = (\overline{Q1} \cdot \overline{Q2})\, f(90^{\circ} - \gamma) - (\overline{Q1} \cdot Q2)\, f(90^{\circ} - \gamma) - (Q1 \cdot \overline{Q2})\, f(\gamma) + (Q1 \cdot Q2)\, f(\gamma)$$

Figure 4.4 Logical relationship between the trigonometric functions and the matrix function

For the conversion equivalent to $90^{\circ} - \gamma$, the following digital rule applies

$$10000000 - \gamma = \overline{\gamma - 1}$$

where

$$\overline{\gamma} = (\overline{\varphi 7}, \overline{\varphi 6}, \overline{\varphi 5}, \overline{\varphi 4}, \overline{\varphi 3}, \overline{\varphi 2}, \overline{\varphi 1})$$

The complement angle is thus found by subtracting the least significant digit from the angle, and then taking the inverted angle digits.

Example:

$$\gamma = 1110011$$
$$\gamma - 1 = 1110010$$
$$\overline{\gamma - 1} = 0001101$$
$$\gamma + \overline{\gamma - 1} = 10000000$$

There is one exception from the rule, for $\gamma = 0000000$. In this particular case, one should take $\overline{\gamma} = 1111111$ instead of $\overline{\gamma - 1}$.

as otherwise the quadrant is changed. This exception from the rule does not involve any display inaccuracy, as $\sin \gamma = 0$ makes one of the output deflection voltages zero.

$\sin \gamma$ is read out with eight digits, where $\sin 90^{\circ} = 11111111$. The least significant digit thus represents

$$\frac{1}{256 - 1} = \frac{1}{255}$$

4.3.2 Data flow, principles

A complete block diagram of the converter is given in Figure 4.109. Data processing takes place in several steps, governed by pulses derived from a pulse sequence generator. The angle digits are first inserted in an input α-register. The γ part of the angle is next used to select the appropriate ferrite matrix core or cores, and $\sin \gamma$ is obtained and stored in an intermediate I-register. The digital $\sin \gamma$ is next routed to a sine or cosine register according to the quadrant information, and a sign digit is added.

Partly during the above processing, a ONE is subtracted from γ (if $\gamma \neq 0000000$) in the α-register and the complement angle $\overline{\gamma - 1}$ digits select the appropriate ferrite core or cores to give $\cos \gamma$. The digital $\cos \gamma$ is then transferred to the I-register and next routed to a cosine or sine register in accordance with the quadrant, and a sign digit is added.

The sine and cosine registers directly drive two digital-to-analog converters.

4.3.3 Pulse se uence generator

All control waveforms (ref Figures 4.108 - 4.109) are derived from the outputs of a twelve stage shift register located on cards 19 - 21 in panel CD. Shift pulses are obtained from an 80 kc/s free running clock generator CG2 after a frequency division by 2 in a counter stage CO1A (TP18.04) and amplification in an emitter follower - inverter EF2A - IV3B chain (TP18.05).

The pulse sequence is started by an amplified STOP LINE pulse obtained from the readout unit.

This pulse is fed to the set terminal (j27.13) of an SR1 circuit via the NORMAL-MANUAL TRIGGER switch on the control panel as shown. The outputs from SR1 are connected to the shift controlling terminals of the first SH1 stage. On arrival of the first shift pulse this stage is set to ONE and the SR1 circuit is reset from the output terminal (j19.16) of the first stage of the shift register.

The ONE condition of the first SH1 stage is shifted downwards in the shift register and a pulse sequence is generated. The pulses obtained from the lower output terminals of stages 2 - 11 (i e the outputs accessible on test points) are designated P1 - P10 while the inverted outputs from the upper terminals are $\overline{P1}$ - $\overline{P10}$.

The pulses $\overline{P1}$, P2, $\overline{P3}$, $\overline{P4}$, P5, P6, P8, $\overline{P8}$ and P10 shown in Figure 4.108 are taken either directly from the shift register or via emitter followers and inverters. The $\overline{P3}$, $\overline{P4}$ and $\overline{P9}$ pulses from the shift register are connected to the three input terminals (j22.16, j22.17, j22.18) of a DL1 circuit. The output of DL1 (TP22.04) is further amplified and inverted, and the waveform P3 + P4 + P9 (TP8.09) is finally obtained.

The waveforms $\overline{P4 + P7}$ and $\overline{P4 + P8}$ are generated in a similar way, the outputs from the DL1 circuits (TP22.05 and TP22.06) being inverted twice. The control terminals of all gate circuits G1 in the sine/cosine converter are grounded and these circuits therefore act as simple inverters.

The negative P4 + P8 waveform obtained from G1 (TP24.07) is connected to the input of a DL1 circuit together with the shift signal $\overline{B}$. As the DL1 circuit acts as an AND gate for negative signals, the P4 and P8 pulses are transferred to the out-

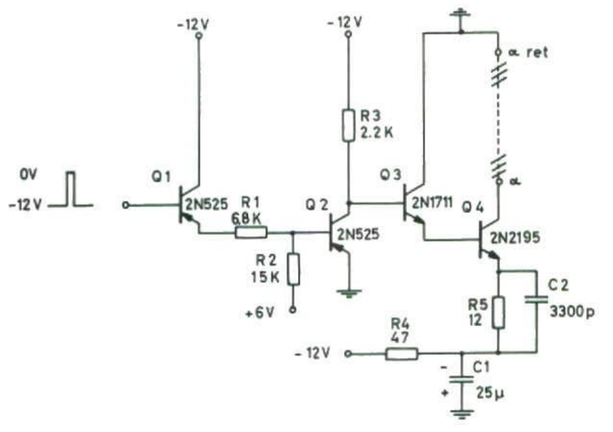


Figure 4.5 Core driver CD2

put only during the negative half cycles of the shift signal. The output waveform from DL1 (TP22.07) is amplified in a core driver CD2 which delivers current pulses $P4^* + P8^*$ to the read wire of the ferrite matrix. A diagram of the CD2 circuit is shown in Figure 4.5.

A $P6^*$ pulse is obtained by combining the P6 pulse from the shift register (TP20.07) with the inverted shift signal B and the clock signal A in a DL1 circuit. A negative pulse of duration approximately 6 μs (the second quarter of the P6 pulse) is obtained from the output (TP22.03). The pulse is further amplified in the circuits EF2-G1 and EF2 - IY1 as shown.

A $P10^*$ pulse (TP23.04) is generated in a similar manner.

The $\overline{P9^*}$ pulse (TP10.05) is generated by combining the P9 pulse (TP21.05) with the shift signal in a DL1 circuit. The output pulse (TP12.05) is amplified and inverted as shown.

4.3.4 Input α-register and blanking logic

In the description below, the data handling of the B1 word will be treated in some detail. The principal events will be given with reference to Figure 4.108.

The read out angle digits φ1 - φ9 are fed to the set controlling terminals of the input α-register and also to an ALL ZERO detecting logic DL2. If φ = 000000000, all DL2 inputs are negative and on arrival of the first STOP LINE pulse, the pulse is permitted through DL2 and emitter follower-inverter EF2 - IV1 as a set blanking pulse to the readout unit (event 1). In the readout unit the blanking is delayed to occur when the strobe in question is to be displayed (ref Section 4.2.4).

Under normal conditions (i e with the SINE TABLE switch SW4 in the NORMAL position) the α-register is cleared of old information by the $\overline{P3}$ pulse (event 2). The α-register is next set with the new φ1 - φ9 information by a $\overline{P4}$ pulse (event 4). As the α-register is connected as a backwards counter, counting operation during setting is inhibited by the waveform P3 + P4 + P9 (event 3).

The α-register now contains the first quadrant angle γ in its upper seven stages and the quadrant information in the two lower stages.

The γ information (α1 - α7, $\overline{\alpha 1}$ - $\overline{\alpha 7}$) is fed to the inputs of seven diode logics DL4. The upper six logics are also fed with P6 and P10 pulses. The seventh diode logic is fed with $P6^*$ and $P10^*$ pulses. Upon arrival of the pulses P6 (event 5) and and $P6^*$ (event 6) the γ information is transferred to the core selection circuits as will be described in Section 4.3.5.

Upon arrival of the $\overline{P8}$ pulse a ONE is subtracted from γ if $\gamma \neq 0000000$ (event 9). The $\overline{P8}$ pulse is controlled by $\overline{\alpha 1}$ - $\overline{\alpha 7}$ in the following manner: All $\overline{\alpha 1}$ - $\overline{\alpha 7}$ outputs are fed to a DL1 stage giving a negative output (TP11.04) only if $\overline{\alpha 1}$ - $\overline{\alpha 7}$ are all negative. The output is amplified and inverted by EF2 - G1, G1 being used as an inverter. The G1 output (TP10.07) is fed to one input (j11.26) of an AND gate DL1 together with the P8 pulse (j11.25). The P8 pulse is thus permitted through DL1 (TP11.05) and the EF2 - G1 chain (TP10.08) if $\gamma \neq 0000000$, and is otherwise inhibited.

The γ - 1 (or γ) information is next passed on to the core selection circuits upon the arrival of the P10 and $P10^{*}$ pulses (events 13 - 14).

Note on North correction

Due to the curvature of the earth, the various strobe reporting stations may have true North directions differing from the North direction of the central strobe receiving station. In the present closed system this effect is taken care of by adjustment of the SRS analog-to-digital shaft encoders such that all transmitted angles are referred to the CSR North direction.

For a system where an SRS reports to more than one CSR, North correction at a CSR may be required. Such correction can be carried out by suitably processing the α-register contents prior to the sin γ core selection. This requires some additions to the pulse sequence generator and a few additional logics.

4.3.5 Core selection circuits

The core selection circuits consist of seven diode logics DL4, each with two output terminals, followed by emitter followers and inverters EF2 - IV1 and core driver circuits CD1 as shown. A detailed diagram of the DL4 circuit controlled by the first stage of the input register is shown in Figure 4.6. For negative signals the DL4 circuit acts as two pairs of AND gates, each pair being followed by an OR gate.

If the first CO2 stage of the input register contains a ONE the $\alpha 1$ output is negative and the negative P6 pulse from the pulse sequence generator is transferred to the upper output terminal (TP4. 02) of the DL4 circuit. If the CO1 stage contains a ZERO, the P6 pulse is transferred to the lower output terminal (TP4. 03). When the subtract ONE pulse ($\overline{P8}$) is received by the α-register the state of the first stage is changed and the $\alpha 1$ and $\overline{\alpha 1}$ outputs change signs. The following P10 pulse which shall feed the ferrite matrix according to the inverted angle combination $\overline{\gamma - 1}$ is therefore transferred to the same output as was the case for P6. The stages 2 - 6 of the input register which contain more significant angle digits may or may not be affected by the subtract ONE action, dependent upon the binary combination. If a digit is unaffected the P6 and P10 pulses are transferred to opposite outputs of the DL4 circuits.

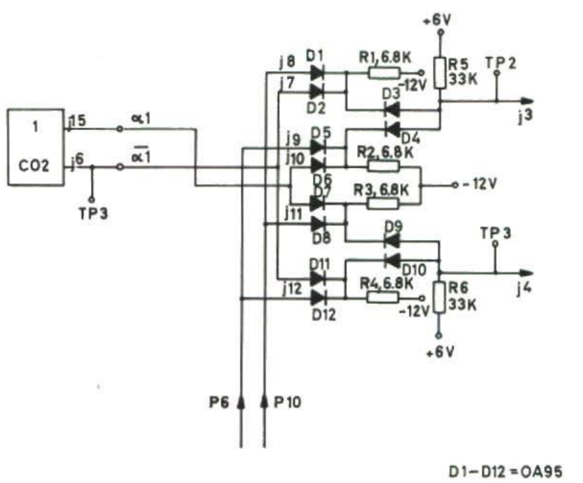


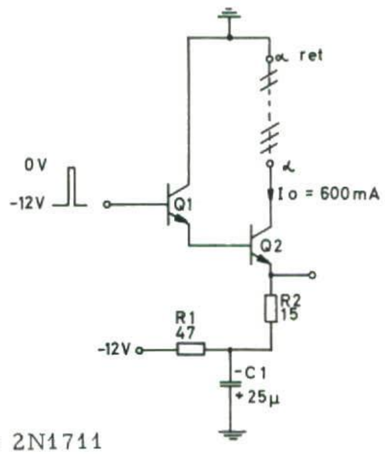
Figure 4.6 Core selection logic

The P6 and P10 pulses are transferred to the outputs of the six least significant DL4 stages according to the following rules:

a) Transfer the P6 pulse to the upper output terminal if α is negative and to the lower output terminal if $\overline{\alpha}$ is negative.

b) Transfer the P10 pulse to the lower output terminal if α is negative and to the upper output terminal if $\overline{\alpha}$ is negative.

The most significant DL4 stage receives the $P6^{*}$ and $P10^{*}$ pulses together with $\alpha 7$ and $\overline{\alpha}7$ as shown. The connections of $P6^{*}$ and $P10^{*}$ are opposite to those of P6 and P10 and the pulses are therefore transferred to the outputs of DL4 according to the opposite rules, i e $P6^{*}$ is transferred according to the P10 rule and $P10^{*}$ is transferred according to the P6 rule.



Q1 : 2N1711
Q2 : 2N2195

Figure 4.7 Core driver CD1

The negative pulses obtained from the DL4 circuits are inverted by the EF2 - IV1 circuits and positive pulses are fed to the input terminals of the core driver circuits CD1. A diagram of the CD1 circuit is shown in Figure 4.7. The circuit consists of two cascaded emitter followers (Darlington circuit). As the current drain is high and of low duty cycle the -12 V is supplied via an RC filter. The collector current I_0 from the last emitter follower is fed through the corresponding selection wire α in the ferrite matrix as shown.

4.3.6 Ferrite matrix

For a full description of the ferrite matrix FM1 reference is made to the wiring diagrams of card type DAF 4/5 given in the Appendix.

The matrix consists of 128 main cores and eight auxiliary cores. The cores are organized in eight columns and seventeen rows. The main cores are located in the rows 0 - 15 while the auxiliary cores are located in the x row. A core located in for instance column 6 and row 1 is designated $C_{6,1}$.

Each main core is coupled to seven of the selection wires while the remaining seven wires bypass the core. If for instance the $\alpha 3$ wire passes through the core the $\overline{\alpha 3}$ wire passes outside the core and so forth. The auxiliary cores are coupled only to the more significant selection wires.

The matrix is arranged in such a manner that the wires selected for the six least significant wires always bypass the selected core (or cores). The current direction for the said wires corresponds to core resetting. Other cores being coupled to $\alpha 1$ - $\alpha 6$ or $\overline{\alpha 1}$ - $\overline{\alpha 6}$ current carrying wires will therefore be reset. The wire ($\alpha 7$ or $\overline{\alpha 7}$) corresponding to the most significant digit always passes through the selected core or cores, and carries core setting current. This wire will also pass through other cores, but without setting them as reset current will be present in one or more $\alpha 1$ - $\alpha 6$, $\overline{\alpha 1}$ - $\overline{\alpha 6}$ wires. It is thus seen that the selection process leads to the setting of only one main core plus possibly one or more auxiliary x-cores.

Assume as an example that the angle is given by $\gamma = 0110011$, i e $\varphi 7 = 0$, $\varphi 6 = 1$, $\varphi 5 = 1$, $\varphi 4 = 0$, $\varphi 3 = 0$, $\varphi 2 = 1$, $\varphi 1 = 1$. According to the rules given in Section 4.3.5 the selection wires $\alpha 6$, $\alpha 5$, $\overline{\alpha 4}$, $\overline{\alpha 3}$, $\alpha 2$ and $\alpha 1$ will be pulsed by the P6 pulse (event 5) and $\alpha 7$ is thereafter pulsed by P6* (event 6). The seven remaining selection wires receive no pulses.

As shown in Figure 4.8 main core No 51 ($C_{3,2}$) and one auxiliary core ($C_{3,x}$) are selected. $\alpha 1$, $\alpha 2$, $\overline{\alpha 3}$, $\overline{\alpha 4}$, $\alpha 5$ and $\alpha 6$ bypass these cores, and inhibit all cores through which the $\alpha 7$ wire is passing (plus a number of cores not coupled to $\alpha 7$).

The P6* pulse thus sets only cores $C_{3,2}$ and $C_{3,x}$.

The matrix also contains eight read wires X1 - X8, corresponding to the eight digits of sin γ, plus a read/reset wire. A read/reset wire bypasses the selected core if the corresponding sine digit is a ONE. Output pulses will thus during readout only occur on the wires corresponding to ZERO digits.

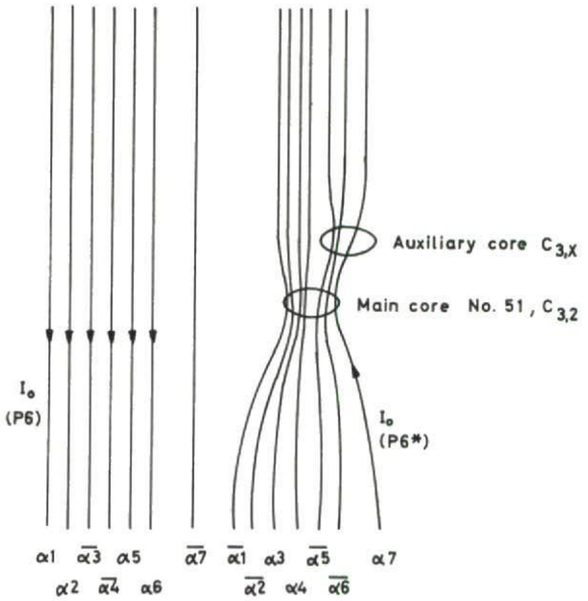


Figure 4.8 Core selection

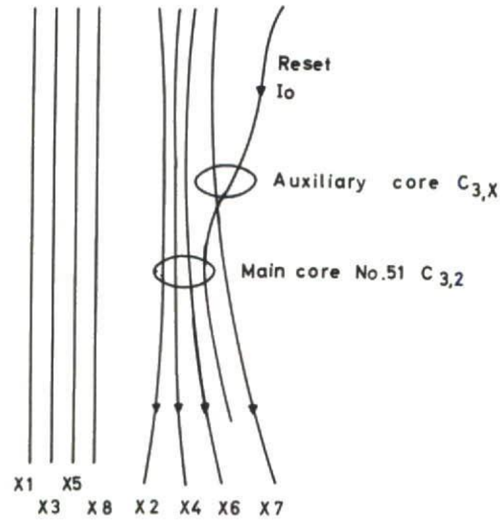


Figure 4.9 Core readout

The digital sine of the angle exemplified above is 10010101. Thus read wires X8, X5, X3 and X1 bypass the selected cores, ref Figure 4.9. The P8* pulse of the P4* + P8* waveform resets the selected cores (event 10) and produces pulses on read wires X7, X6, X4 and X2. All other cores are reset prior to the arrival of the reset pulse. The output pulses are amplified in eight read amplifiers RA1 and fed to the I-register as described later.

At a later instance the proper wires $\alpha 1$ - $\alpha 7$, $\overline{\alpha 1}$ - $\overline{\alpha 7}$ corresponding to the complement angle $\overline{\gamma - 1}$ (or $\overline{\gamma}$) are selected (events 13 - 14), and sin $\overline{\gamma - 1}$ (or sin $\overline{\gamma}$) is read out by a P4* pulse (event 19) in a similar manner.

4.3.7 Read amplifiers RA1

The pulses on the read wires have an amplitude of 150 - 200 mV. For noise cancellation purposes the X wires are fed through the cores in alternate directions (according to a Gray code). The output pulses may therefore be of positive or negative polarity.

Each read wire is connected to a read amplifier RA1, ref Figure 4.10.

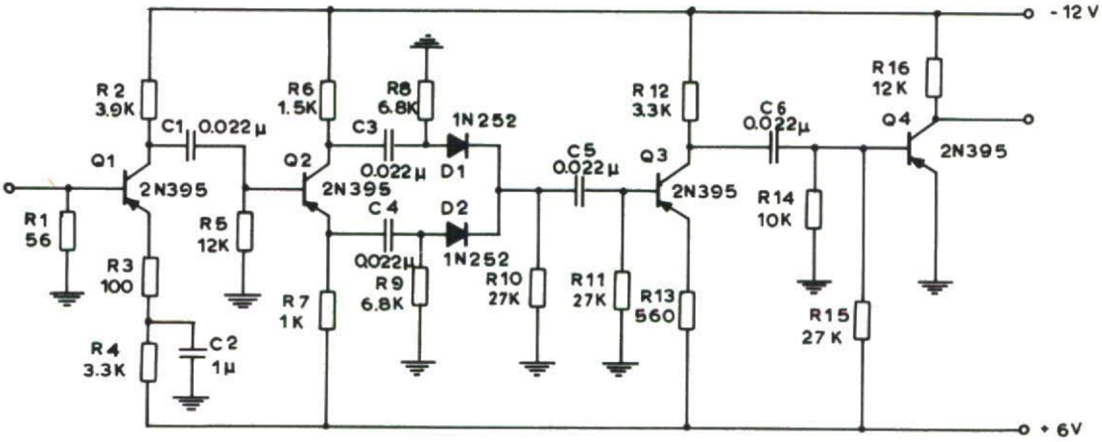


Figure 4.10 Read amplifier RA1

The signal from the matrix is fed to a linear amplifier Q1 followed by a phase inverter Q2. The Q2 emitter and collector outputs are fed through rectifying diodes such that regardless of the polarity of the input signal the phase inverter output is always positive. The positive output pulse is further amplified by transistor Q3 which is biased to the point of saturation. The last amplifying stage Q4 is biased beyond cut-off by the R14 - R15 combination such that the pulse from Q3 must exceed a certain level before Q4 can draw current. An input pulse which exceeds approximately 70 mV drives the output stage into saturation, yielding a 10 V output pulse.

4.3.8 Intermediate I-register

The I-register which is located on cards 16 - 17 in panel AB, contains eight CO2 stages connected as simple set/reset circuits.

The I-register is reset to the state 11111111 by the $\overline{P7}$ pulse of the $\overline{P4 + P7}$ waveform (event 7).

Upon application of the first ferrite matrix read pulse P8* the digital sin γ is set (event 10). This setting is controlled by the $\overline{P8}$ pulse of the $\overline{P4 + P8}$ waveform (event 8). The CO2 stages are thus set in accordance with sin γ (in the example 10010101), the upper terminal of a stage becoming negative if the corresponding digit is a ONE.

A P2 pulse transfers the I-register information to the sine or cosine register (event 16) as described later. The I-register is next reset by a $\overline{P4}$ pulse (event 17), and the cos γ information is entered in the I-register upon the application of the $\overline{P4}$ pulse of the $\overline{P4 + P8}$ waveform (event 18) and the read pulse $\overline{P4^*}$ (event 19) to the ferrite matrix.

4.3.9 Quadrant information Q-register

The Q-register contains two CO2 stages, the control terminals being connected to stages 8 and 9 of the α-register (TP2.07 and TP3.03). The Q-register is reset by the $\overline{P8}$ pulse (event 9), and is set in accordance with $\alpha8$ and $\alpha9$ upon arrival of the P9* pulse (event 12). Counting action during setting is inhibited by the P9 pulse of the P3 + P4 + P9 waveform (event 11). When set, the Q-register outputs Q1 and Q2 equal outputs $\alpha8$ and $\alpha9$ of the α-register.

4.3.10 Quadrant information converter

The quadrant information converter consists of eight DL1 circuits followed by EF2-G1 circuits, the G1 circuits being used as inverters. The G1 outputs are strapped together in pairs. The DL1 circuits act as AND gates for negative signals while each EF2 - G1 pair acts as a NOR gate. If a negative pulse is fed to either of the two EF2 - G1 circuits of a pair, a positive output pulse is obtained from the common output terminal of the G1 circuits.

Upon application of a P2 pulse to the DL1 circuits, one of the main four outputs will deliver a positive pulse $\overline{C}$- or $\overline{C}$+ or $\overline{S}$+ or $\overline{S}$- to guide the further processing of sin γ from the I-register (event 16). Similarly, a P5 pulse will provide a pulse for the further processing of sin $\overline{\gamma - 1}$ (or sin $\overline{\gamma}$) (event 20).

With the designation used, S and C represent sine and cosine respectively. An S pulse denotes that the sine value stored in the I-register should be routed to the sine register, and the polarity indicates the sign to be affixed. Similarly, a C pulse will route the I-register contents to the cosine register with the proper sign.

The rules are given in Table 4.1 which may be compared with Figure 4.4.

As an example, assume that the input angle φ belongs in the second quadrant, making Q1 = $\overline{Q2}$ = negative. The P2 pulse is then passed by the second DL1 circuit and a positive $\overline{C}$- pulse is obtained (TP7.07) indicating that the sin γ contained in the I-register should be treated as a cosine value of negative sign. The subsequent P5 pulse is passed by the sixth DL1 circuit and a positive $\overline{S}+$ pulse is obtained (TP8.08) indicating that the sine value now stored in the I-register (sin $\overline{\gamma - 1}$ (or sin $\overline{\gamma}$ if γ = 0000000)) belongs in the sine register with positive sign.

The positive $\overline{S}$- pulse is fed directly to the set terminal (j25.13) of the ninth stage of the sine register, and the $\overline{C}$- pulse to the set terminal (j27.08) of the ninth stage of the cosine register.

The negative S+, S-, C+ and C- pulses are fed to the eight diode logics DL4 in the sine/cosine selection circuit.

Quadrant No	Q2	Q1	P2 (event 16)	P5 (event 20)
1	0	0	S+ (TP12.03)	C+ (TP11.03)
2	0	1	C- (TP11.06)	S+ (TP12.04)
3	1	0	S- (TP12.07)	C- (TP12.02)
4	1	1	C+ (TP11.02)	S- (TP12.06)

Table 4.1 Generation of sine and cosine pulses

4.3.11 Sine/cosine selector

The sine/cosine selector comprises eight diode logics DL4, the two outputs of each being followed by emitter follower - inverter EF2 - IV1. The task of the sine/cosine selector is to transfer the I-register contents to the appropriate sine or cosine register upon the arrival of the first S or C pulse (event 16), and to the cosine or sine register when the next C or S pulse arrives (event 20).

A detailed diagram of the upper DL4 circuit is given in Figure 4.11. S1 is negative if the first CO2 stage contains a ONE, whereas a ZERO would make $\overline{S1}$ negative. Assume that S1 is negative and that a negative S+ pulse is received on arrival of the P2 pulse from the pulse sequence generator (ref Table 4.1). A negative pulse is then obtained from the upper output (TP18.02) of the DL4 circuit. This pulse is further amplified and inverted by EF2 - IV1 and the first stage of the sine register is set. If $\overline{S1}$ is negative, the S+ pulse is inhibited and no pulse is transferred to the outputs of DL4. If instead of the S+ pulse an S- pulse is received (third quadrant) the first stage of the sine register is set according to the inverted sine digit, i e the S- pulse is transferred to the upper terminal of the DL4 circuit if $\overline{S1}$ is negative while this pulse is inhibited when S1 is negative.

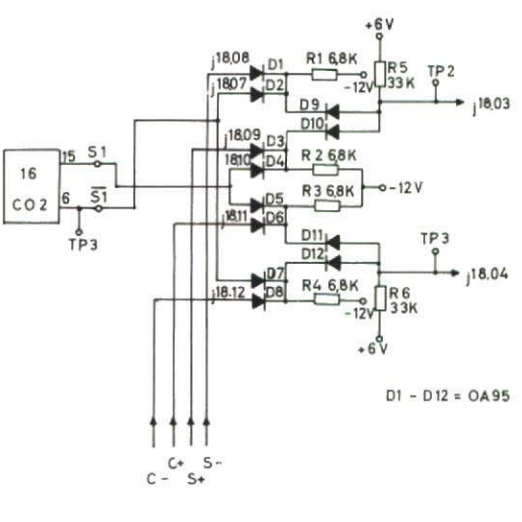


Figure 4.11 Sine/cosine selection logic

When a C+ or C- pulse is received, the pulse will be transferred to the lower terminal according to the same rules and the sine digit S1 or the inverted sine digit $\overline{S1}$ is transferred to the cosine register. When the S- or C- pulse is received, stage 9 of the sine or cosine register respectively is set to ONE as described above. The reasons for using the inverted sine combination when the sign is negative is made clear in Section 4.3.13.

When sin γ has been transferred to either the sine or cosine register by the P2 pulse as described above, the I-register is reset to 11111111 by the P4 pulse of the $\overline{P4 + P7}$ waveform (event 17). cos γ is next transferred to the I-register (events 18 - 19).

$\cos\gamma$ is now transferred to the cosine or sine register upon arrival of the P5 pulse to the quadrant information converter, according to the received S+, S-, C+ or C- pulse (event 20) in a similar manner as described for the $\sin\gamma$ transfer. A study of Table 4.1 will reveal that if the sine register is selected for $\sin\gamma$, the cosine register is selected for $\cos\gamma$, and vice versa.

4.3.12 Sine and cosine registers

The sine and cosine registers each contain nine set/reset circuits SR1. Each register is reset by a $\overline{\text{P1}}$ pulse (event 15) prior to the arrival of $\sin\gamma$ and $\cos\gamma$.

From the above discussion it will be seen that the following rules apply:

a) Angle φ in first quadrant

The sine register contains $\sin\gamma$, and the cosine register contains $\cos\gamma$. The ninth stage of each register is unset.

b) Angle φ in second quadrant

The sine register contains $\cos\gamma$ and stage 9 is unset. The cosine register contains the inverted $\sin\gamma$ combination, and stage 9 is set.

c) Angle φ in third quadrant

The sine register contains the inverted $\sin\gamma$ combination and stage 9 is set. The cosine register contains the inverted $\cos\gamma$ combination, and stage 9 is set.

d) Angle φ in fourth quadrant

The sine register contains the inverted $\cos\gamma$ combination and stage 9 is set. The cosine register contains $\sin\gamma$, and stage 9 is unset.

4.3.13 Digital-to-analog converters DA1

The sine and cosine registers directly feed two digital-to-analog converters DA1. A simplified diagram is given in Figure 4.12 together with a table indicating the sine and cosine register contents at the angles φ = 0, 90, 180, 270°. Note that if the sine or cosine value is negative, the corresponding register contains the inverted eight least significant digits.

The display requires a negative polarity input for a positive deflection, and -15 V corresponds to a deflection equivalent to 320 nm.

The DA1 includes a high gain DC amplifier with heavy negative feedback, making the input impedance a fraction of an ohm.

The input contains nine switches, a switch being closed when the corresponding digit is a ONE. Each switch controls through a high precision resistor an input current to the amplifier. The current is supplied from two temperature controlled highly stable Zener reference voltages (+18 V and -18 V).

When all switches are open, the amplifier input current is zero. When all switches are closed, the input current is given by

$$I = 18\left(\frac{1}{2R} + \frac{1}{4R} + \dots + \frac{1}{256\,R}\right) - 18\frac{1}{R+\Delta}$$

Δ is adjusted such that I equals zero.

The maximum output voltage is preset to the desired level by resistor R_f.

The detailed circuit diagram of DA1 is given in Figure 4.13. As switches are used transistors Q1 - Q9. The Zener diodes Z1 - Z9 serve to transfer the control voltages positively (15 V for 115Z4, 12 V for 112Z4). Potentiometer P5 serves for fine adjustment of Δ (ref Figure 4.12).

φ	sin φ	Contents of sine reg	sine DA1 output	cos φ	Contents of cosine reg	cosine DA1 output
000 000 000	0	000 000 000	0 V	1	011 111 111	-15 V
010 000 000	1	011 111 111	-15 V	0	111 111 111	0 V
100 000 000	0	111 111 111	0 V	-1	100 000 000	+15 V
110 000 000	-1	100 000 000	+15 V	0	000 000 000	0 V

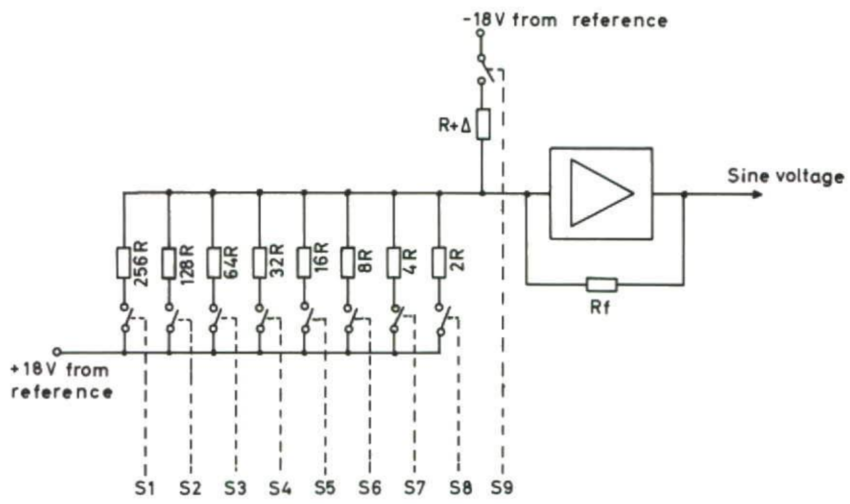


Figure 4.12 Digital-to-analog converter DA1, block diagram

The amplifier has an input balanced stage (transistors Q11 - Q12), being constant current fed from transistor Q14. Proper balance is obtained by adjustment of P3. The stabilized working point is controlled by P4, and the zero point by P1. For accurate zero setting, switch SW1 is pressed whereby the feedback is interrupted and full receiver gain is obtained.

The input stage is followed by a second push-pull stage Q10 - Q13, which also through feedback stabilizes the working point of the first stage. The two output cascaded emitter followers match the amplifier to the load presented by the display system. The overall gain is adjusted by P2.

The DA1 outputs are connected to the display system over coaxial cables connected to the Z plint (ref Figure 4.109).

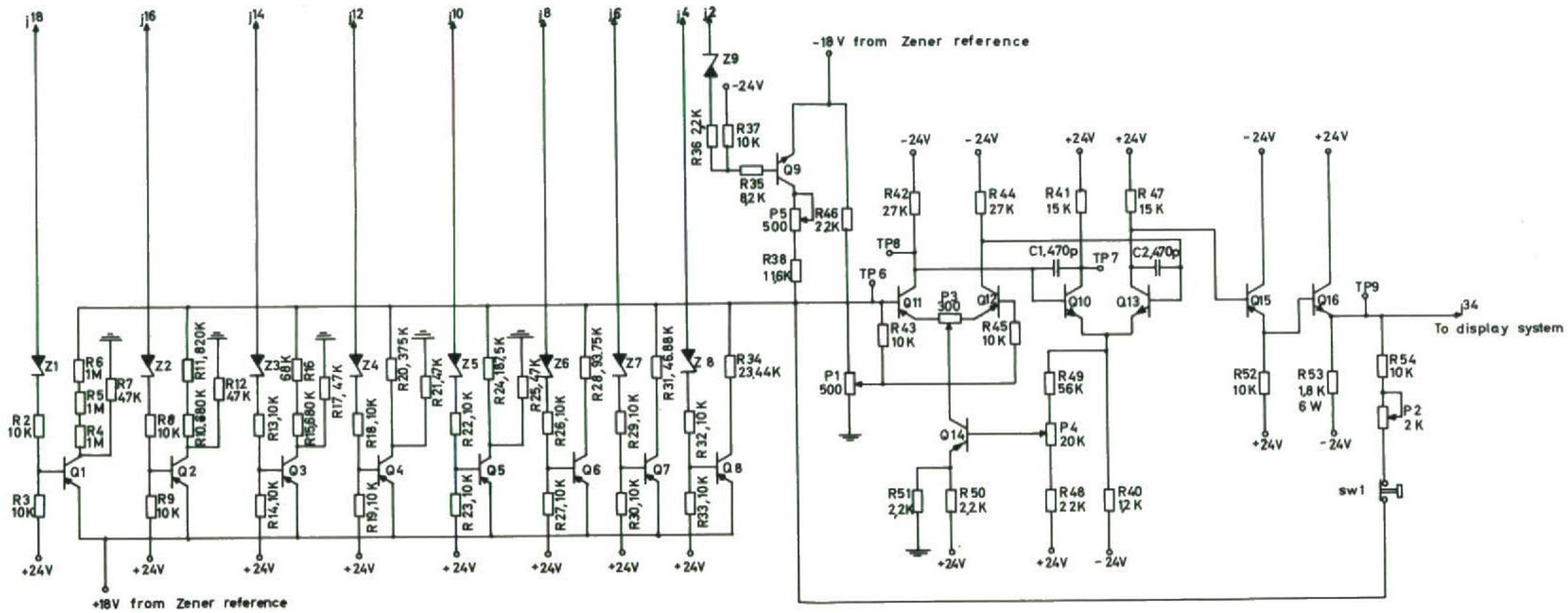
When the various waveforms are delivered to the display system, the further control is taken over by the latter system.

4.3.14 Test facilities

By means of controls and indicators located on the control panel the main functions of the sine/cosine converter may be checked, ref Figures 4.108 - 4.109.

4.3.14.1 Star test

Under normal operation the P2 pulse from TP24.03 is grounded by the SINE TABLE switch SW4. When SW4 is in the STAR position P2 is permitted to the DC coupled



Z1 - Z8 : 115Z4
Z9 : 112Z4
Q1 - Q8, Q14 : 2S303
Q9, Q10, Q13, Q16 : 2N1711
Q11, Q12, Q15 : 2S301

Figure 4.13 Digital-to-analog converter DA1, circuit diagram

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set terminal (j2.05) of stage 6 of the α-register. During this setting there is no count inhibition present, and a carry over is transferred to stages 7, 8 and 9.

When the reset pulse $\overline{P3}$ arrives, stages 1 - 6 are reset. Stages 7 - 9 are not reset, as their reset control terminals (j2.30, j2.25, j2.13) are now connected to -12 V via the SW4 switch.

The normal set pulse $\overline{P4}$ (TP10.09) is grounded via switch SW4. No transfer of angles into the α-register can therefore take place.

The list of events is therefore as given in Table 4.2. Note that the α-register is connected as a backwards counter.

i)	P2 sets $\alpha 6$	: 000 100 000	
	Due to carry over	: 111 100 000	
	$\overline{P3}$ resets $\alpha 1$ - $\alpha 6$	: 111 000 000	(315^{o})
ii)	P2 sets $\alpha 6$	: 111 100 000	
	Due to carry over	: 110 100 000	
	$\overline{P3}$ resets $\alpha 1$ - $\alpha 6$	: 110 000 000	(270^{o})
iii)	P2 sets $\alpha 6$	: 110 100 000	
	Due to carry over	: 101 100 000	
	$\overline{P3}$ resets $\alpha 1$ - $\alpha 6$	: 101 000 000	(225^{o})
iv)	P2 sets $\alpha 6$	: 101 100 000	
	Due to carry over	: 100 100 000	
	$\overline{P3}$ resets $\alpha 1$ - $\alpha 6$	: 100 000 000	(180^{o})
v)	P2 sets $\alpha 6$	: 100 100 000	
	Due to carry over	: 011 100 000	
	$\overline{P3}$ resets $\alpha 1$ - $\alpha 6$	: 011 000 000	(135^{o})
vi)	P2 sets $\alpha 6$	: 011 100 000	
	Due to carry over	: 010 100 000	
	$\overline{P3}$ resets $\alpha 1$ - $\alpha 6$	: 010 000 000	(90^{o})
vii)	P2 sets $\alpha 6$	: 010 100 000	
	Due to carry over	: 001 100 000	
	$\overline{P3}$ resets $\alpha 1$ - $\alpha 6$	: 001 000 000	(45^{o})
viii)	P2 sets $\alpha 6$	: 001 100 000	
	Due to carry over	: 000 100 000	
	$\overline{P3}$ resets $\alpha 1$ - $\alpha 6$	: 000 000 000	(0^{o})
ix)	As i)		

Table 4.2 STAR generation

It will be seen that all octant angles are generated in sequence. All other operations are normal. The star will therefore on the display be presented at all four origins.

If any word in the store happens to be 000000000, a blanking pulse would be initiated by the ALL ZERO detector. One of the octant angles would therefore be blanked. To avoid this the set blanking pulse is grounded via the SW4 switch (ref Figure 4.107).

4.3.14.2 Increment test

When the SINE TABLE switch SW4 is in the INCREMENT position, the setting of the sixth α-register stage by the P2 pulse is inhibited as during normal operation.

The α-register set and reset pulses $\overline{P4}$ and $\overline{P3}$ are grounded by SW4. The lower terminal (j11.27) of the subtract ONE inhibit logic DL1 is grounded by SW4. The subtract ONE pulse $\overline{P8}$ is therefore permitted whatever the α-register contents are. The α-register is thus connected as a pure backwards counter, subtracting a ONE for every $\overline{P8}$ pulse.

When the NORMAL-MANUAL TRIGGER switch SW9 is in the NORMAL position, the pulse sequence is governed by the STOP LINE trigger pulses. When SW9 is in the MANUAL TRIGGER position, trigger pulses can be obtained by pressing the TRIGGER push-button SW10. The shift waveform $\overline{B}$ is fed to the set and reset terminals (j27.34, j27.30) of an SR1 stage. The control reset terminal (j27.33) is normally grounded and the control set terminal (j27.31) is negative. When SW10 is pressed, the first arriving $\overline{B}$ pulse sets the SR1 stage and a positive trigger pulse is obtained from the SR1 amplified output (TP22.09). This pulse initiates one pulse sequence from the pulse sequence generator. The contents of the α-register is thereby reduced by a ONE whenever SW10 is pressed. By means of the indicators the operation of the α, Q and I-registers and the ferrite matrix may thus be studied in detail.

4.4 Tape simulator

Due to the data code used, the SRS can be fed by synthetic data from a tape transmitter. As one message lasts 0.45 s, 32 messages occupy 14.4 s or close to one antenna revolution period (15 s). It is thus seen that one single tape can furnish data for eight targets to each of the four receivers with real time updating, provided that a suitable multiplexing scheme is used.

The block diagram of the arrangement used is shown in Figure 4.110. For synchronization purposes a standard automatic tape transmitter has been fitted with a photocell receiving light through a hole in a disc mounted on the element sensing shaft. The synchronizing circuit as shown in Figure 4.14 is seen to amplify and regenerate the photocell pulse.

The disc rotates continuously whether the sensing clutch is operated or not. The disc has therefore been adjusted such that the photocell pulse coincides with the first part of the teleprinter start pulse, if present. The combination of the teleprinter characters (waveform A) and the regenerated photocell pulse C takes place in a diode logic DL1, acting as an AND gate for negative signals. The resulting pulse (TP26.06) is fed to a four stage counter which is initially reset by push button SW11 (RESET) located on the control panel. The counter will thus give a running count of the number of start pulses from the beginning of the simulator sequence.

The outputs of the first two counter stages are combined with the input pulse D to provide a reset pulse G for every third input pulse. The first two stages will therefore be a scale-of-three counter, while the last two stages represent a scale-of-four counter.

By logic combinations of the outputs of the last two stages with the train of teleprinter characters, the waveforms J, K, L, M result, and it will be seen that the teleprinter characters are divided in four time-multiplexed groups of three characters each suitable for distribution to the four receivers. The receivers may be connected individually to the simulator by means of switches SW5-SW8 (NORMAL-SIMULATOR selectors, ref Figure 4.105.

The first start pulse in each group is shortened equal to the time delay between the leading edge of the true start and the trailing edge of the regenerated photocell pulse. This delay is less than 5 ms. The remaining part of the pulse is sufficiently long to be recognized as a correct start pulse by the receiver.

Similarly, after the third teleprinter character a negative pulse appears. This pulse is so short that it will be disregarded by the receiver.

It is seen that at the beginning of the tape program two characters appear in the receiver D channel before the sequence starts properly. This is taken care of by placing the tape two character positions ahead of the desired sequence.

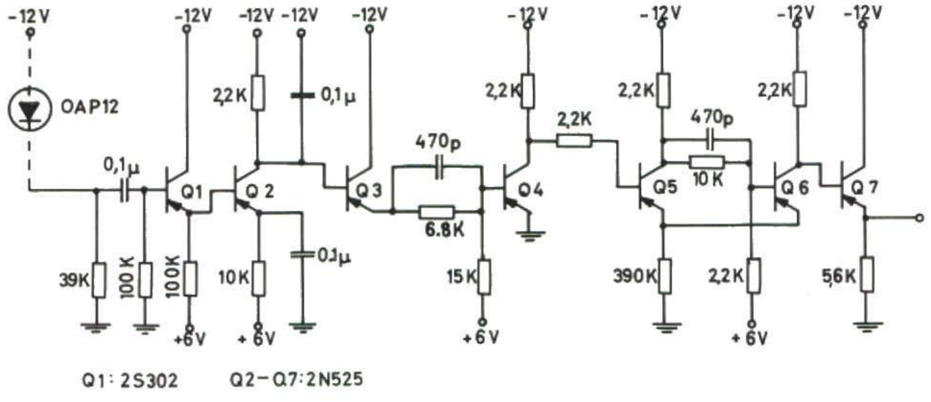

Figure 4.14 Teleprinter synchronizer SY2

4.5 Triangulation table

The triangulation table is a modified 40 cm early warning plan position indicator. Its operational functions have been described in Part I, Section 2.3.4, to which reference is made. Adjacent to the table is mounted a selective strobe erasure panel, which was described in Part II, Section 4.1.3.

The main synchronizing waveforms transmitted from the triangulation table and its associated equipments to the CSR-1 data handling equipment are:

a) +15.347 V reference

b) Sweep synchronization pulses

d) 40 nm markers

e) Stop line pulses

The CSR-1 equipment delivers the following waveforms:

f) X_o origin voltage

g) Y_o origin voltage

h) Blank origin waveform

i) X strobe deflection voltage

j) Y strobe deflection voltage

k) Blank strobe waveform

The waveforms and their timing are summarized in Figure 4.15.

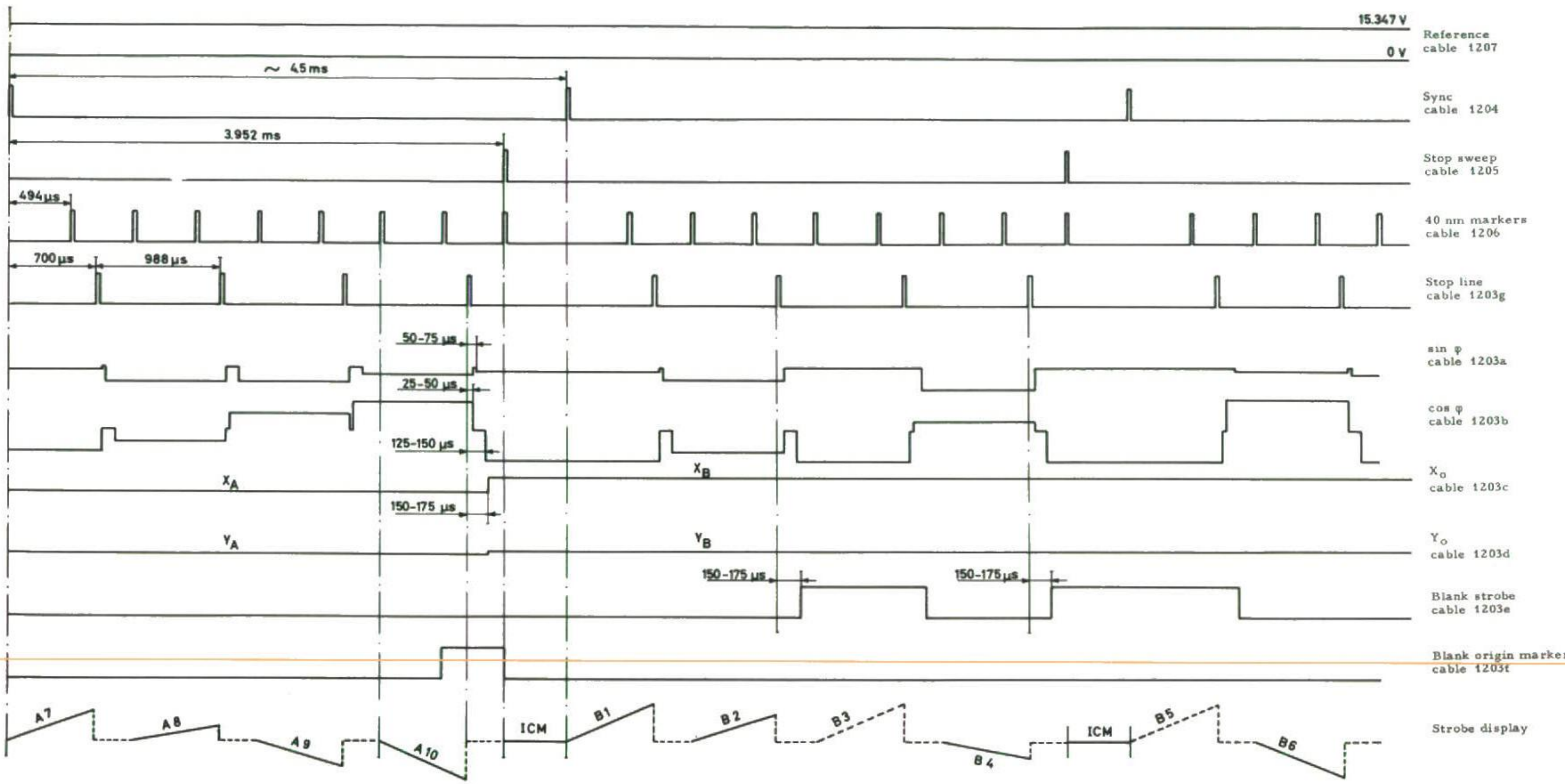

Figure 4.15 Waveforms connecting the CSR and the CRC semi-automatic system

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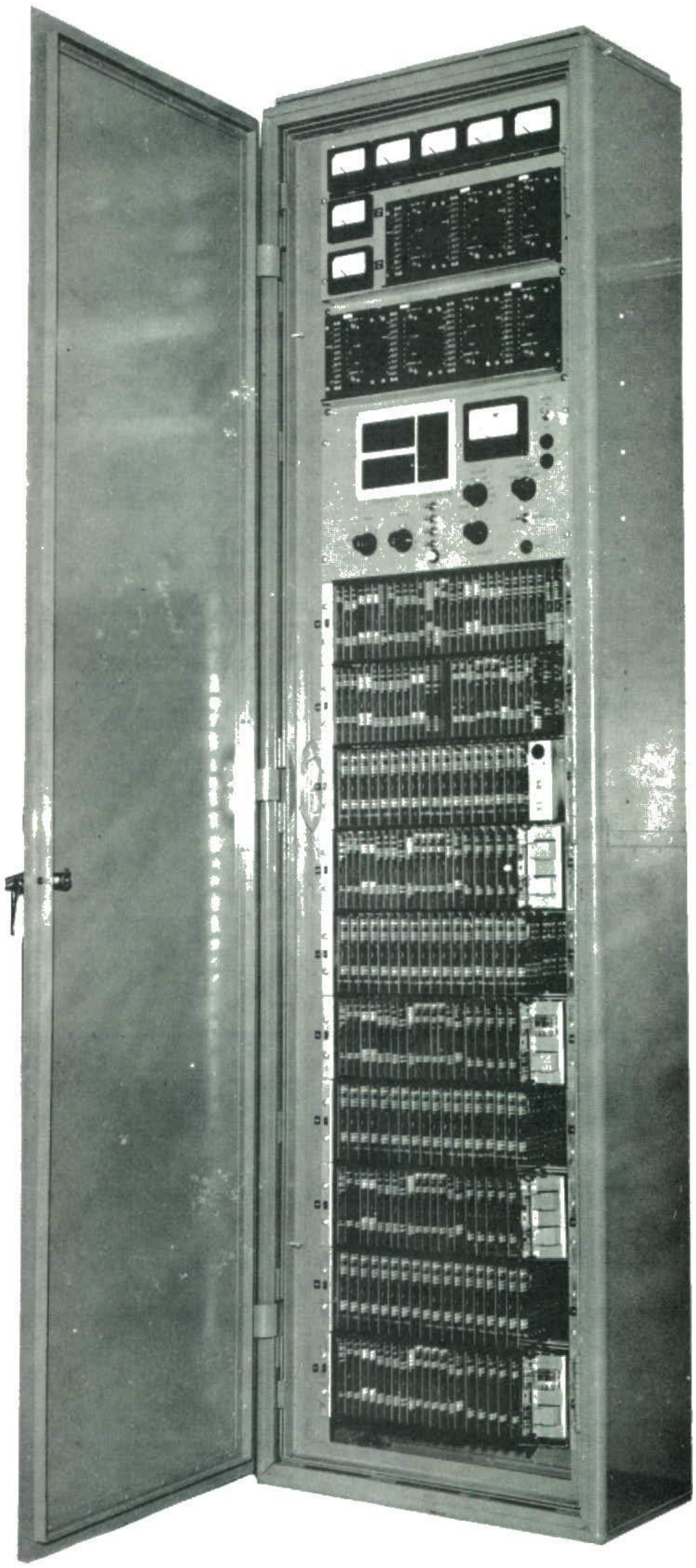

Figure 4.101 Central strobe receiving equipment CSR-1

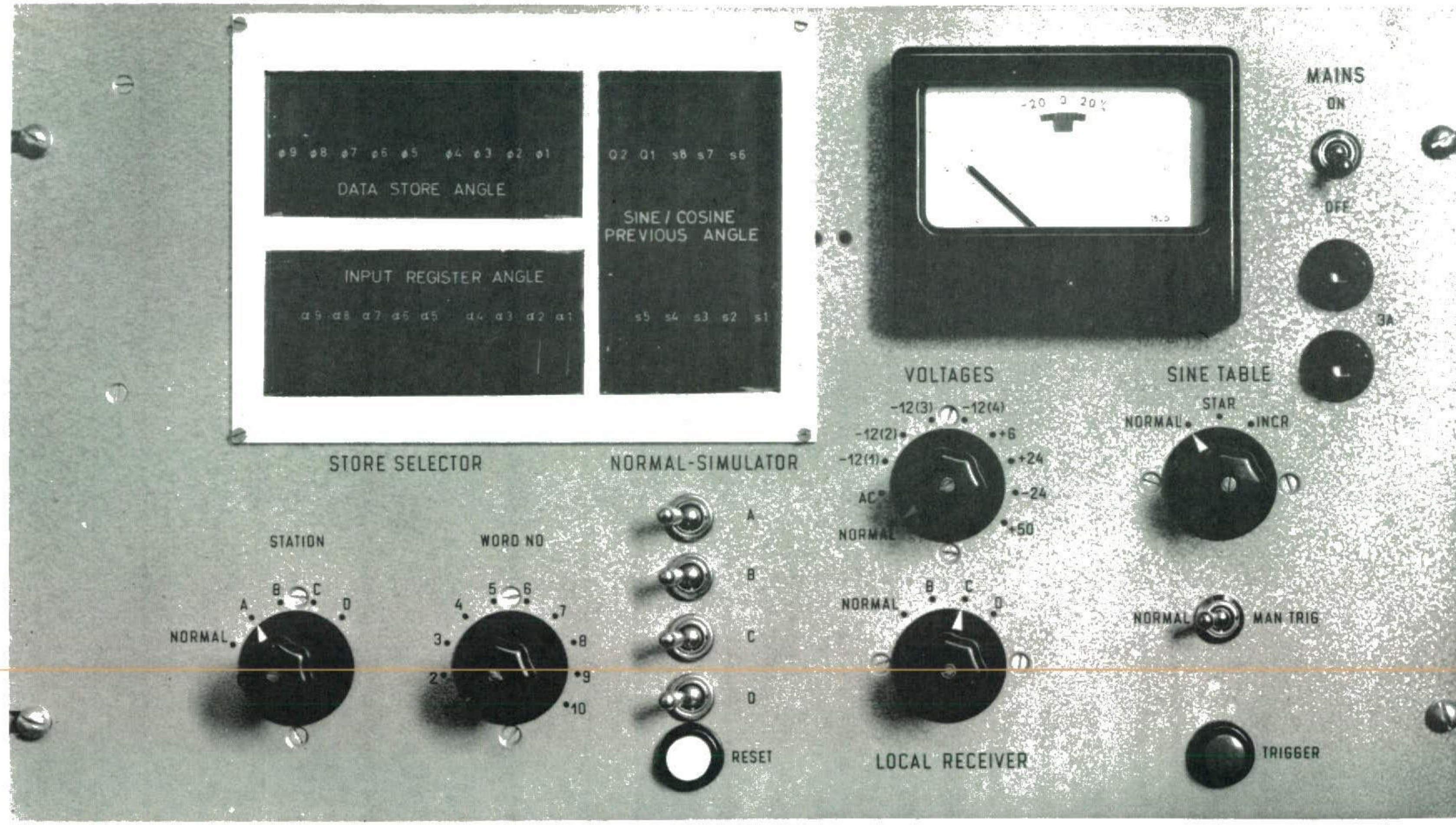

Figure 4.102 CSR control panel

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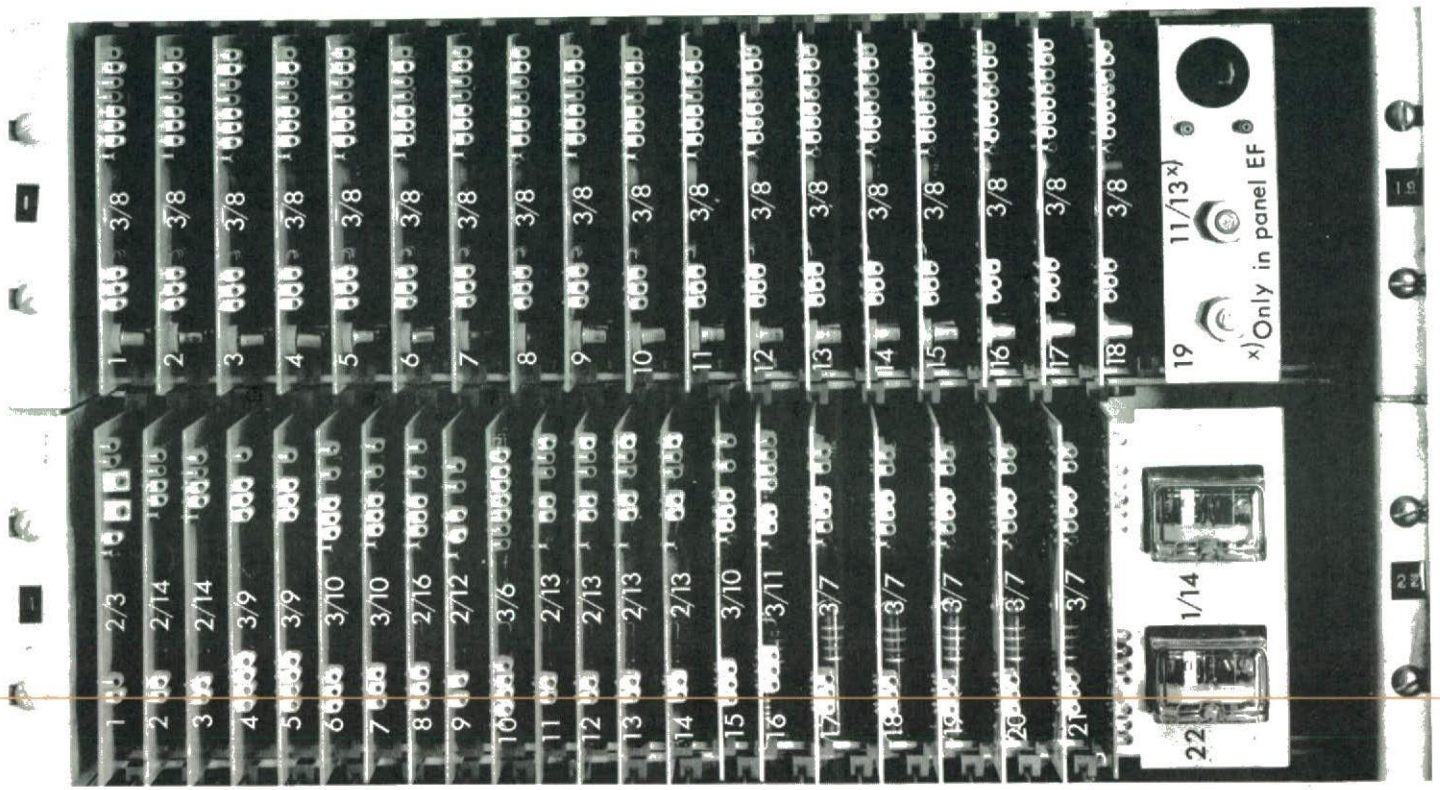

Panel EF
(IJ, MN, QR)
Store

Panel GH
(KL, OP, ST)
Receiver

Figure 4.103 CSR panels EF-ST: receivers and stores

Panel AB

Panel CD

Figure 4.104 CSR panels AB and CD: readout unit, sine/cosine converter, teleprinter simulator

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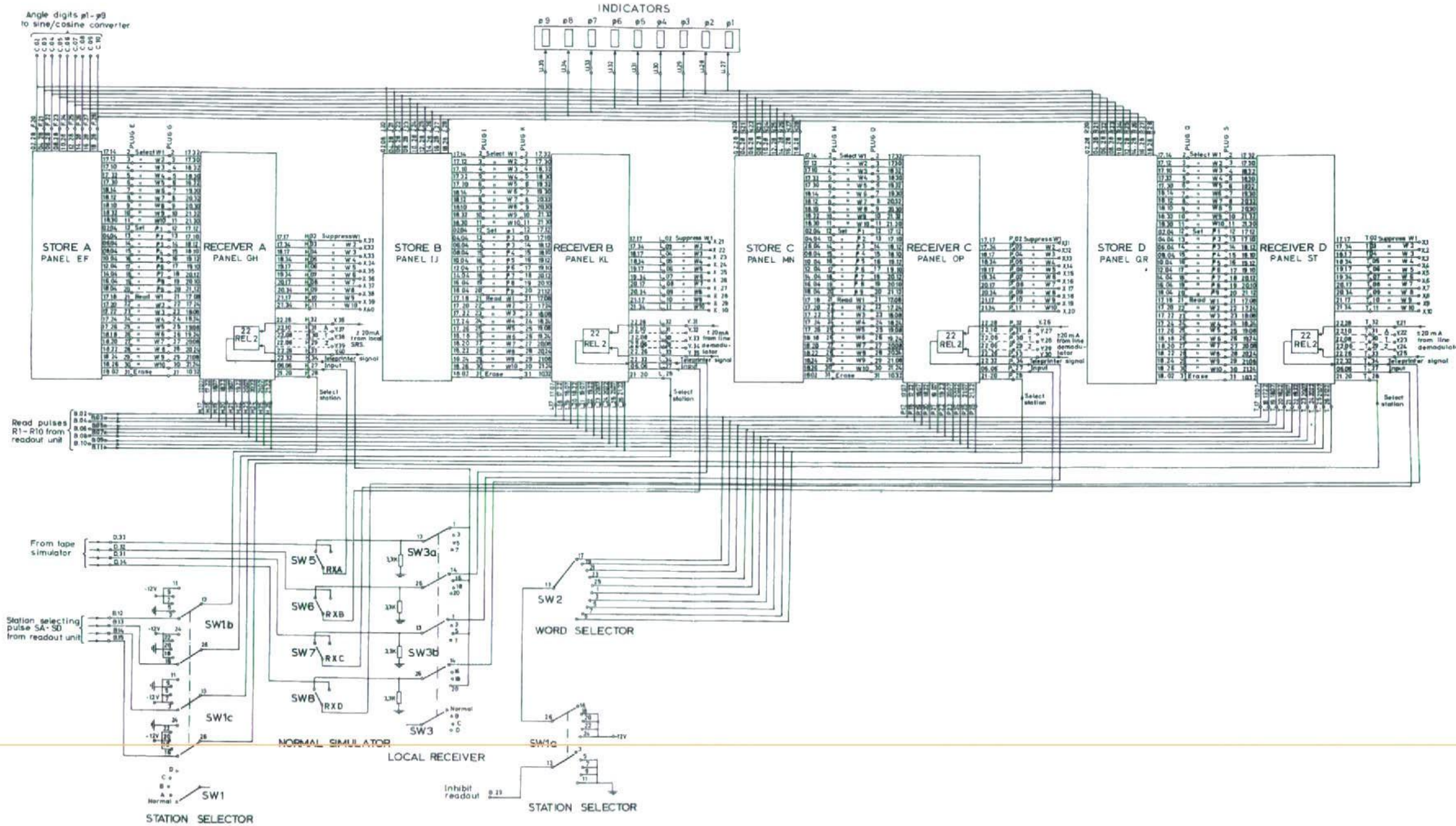


Figure 4.105 CSR receivers and stores, block diagram

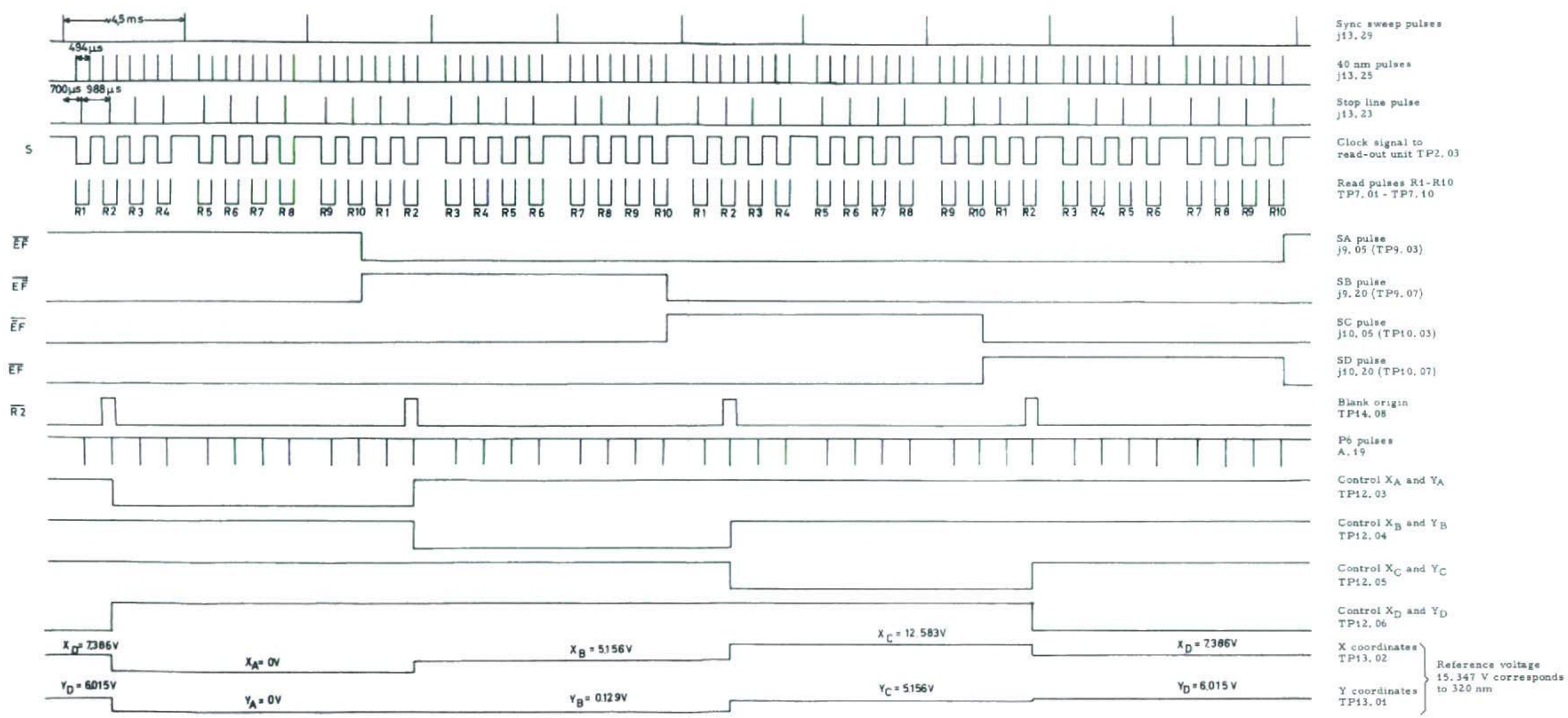


Figure 4.106 CSR readout and coordinate selection circuit, waveforms

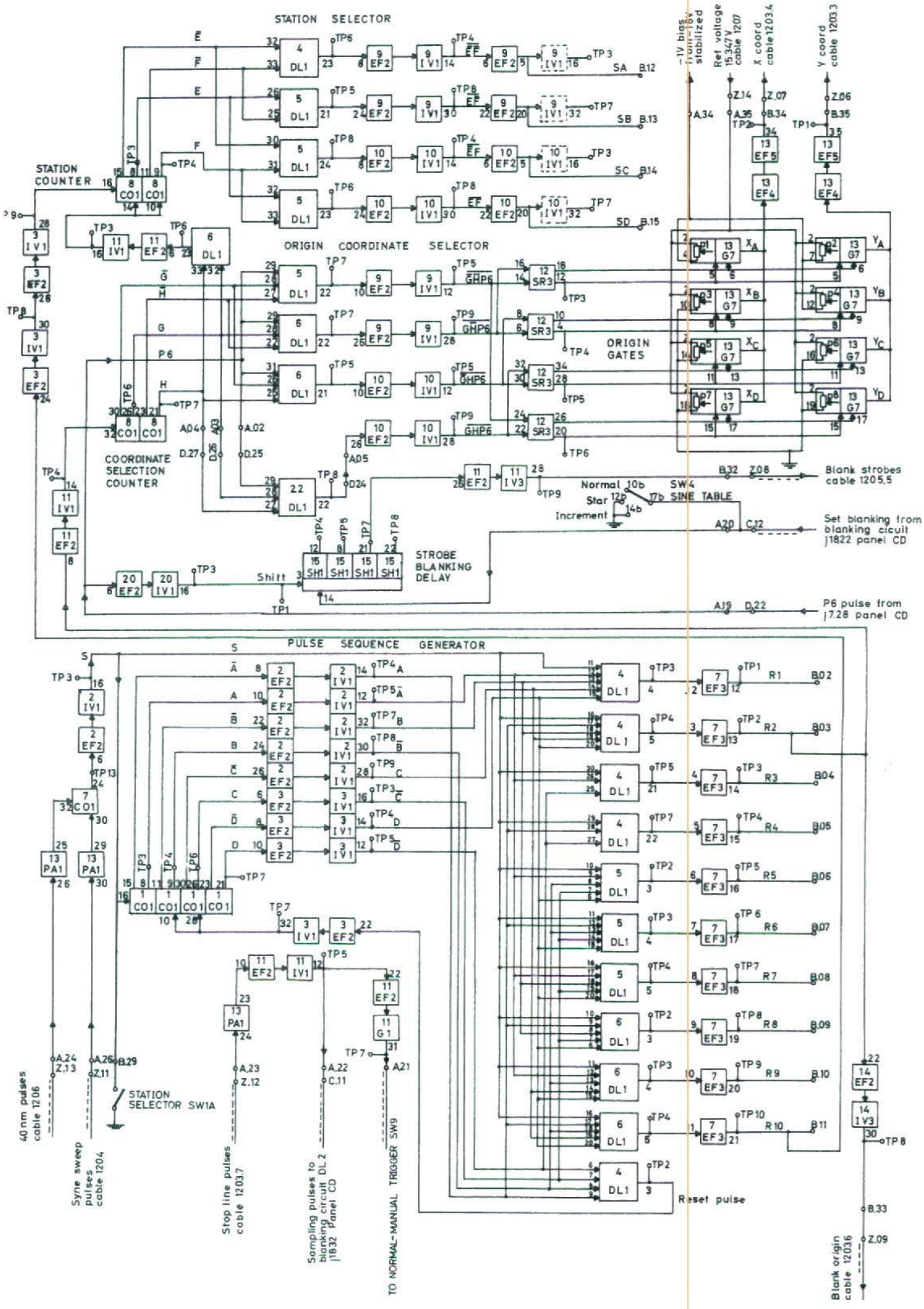
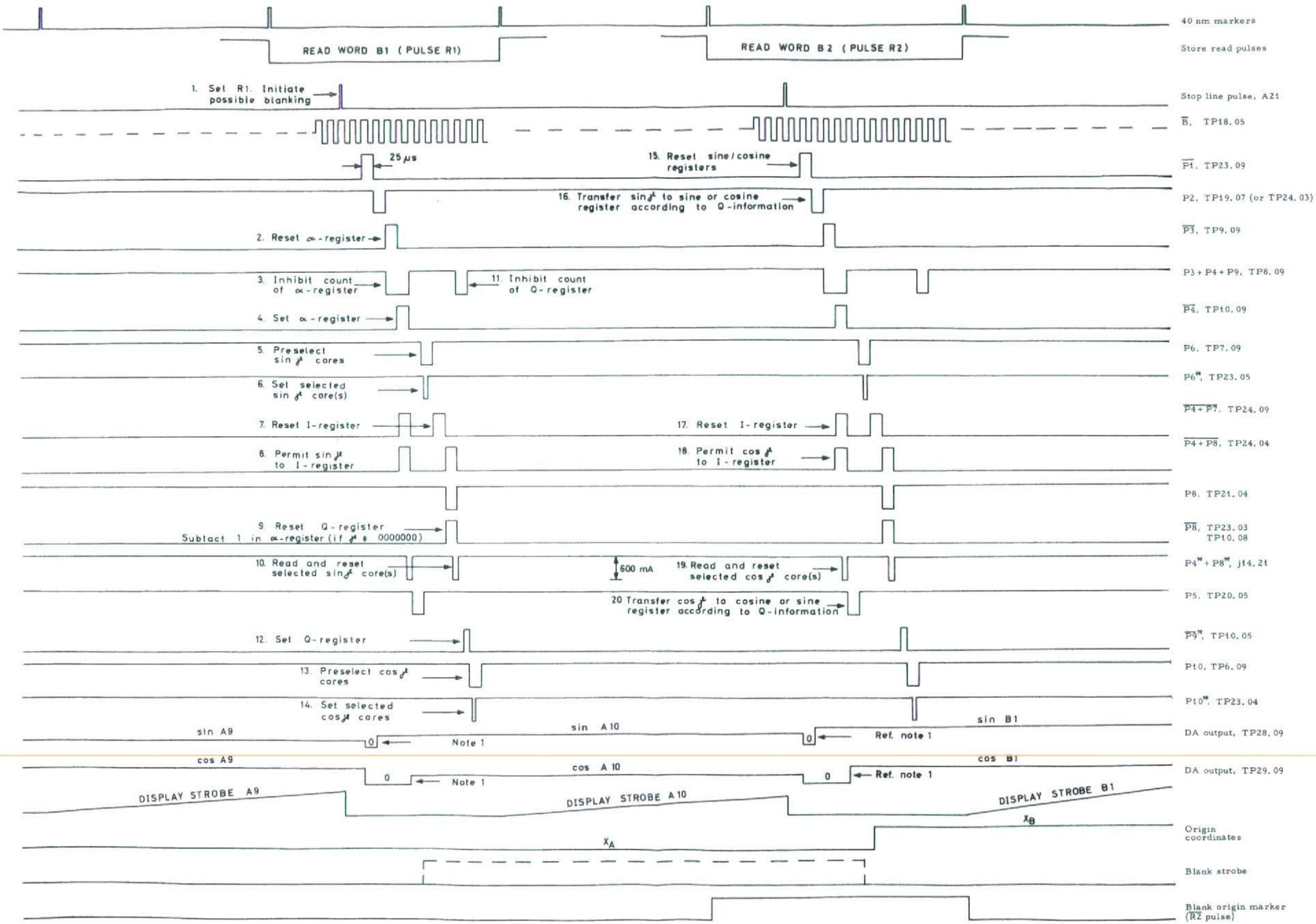


Figure 4.107 CSR readout and coordinate selection circuits, block diagram



Note 1: The starting times of sin φ and cos φ are interchanged if φ is in second or fourth quadrant.

Figure 4.108 CSR sine/cosine converter, waveforms

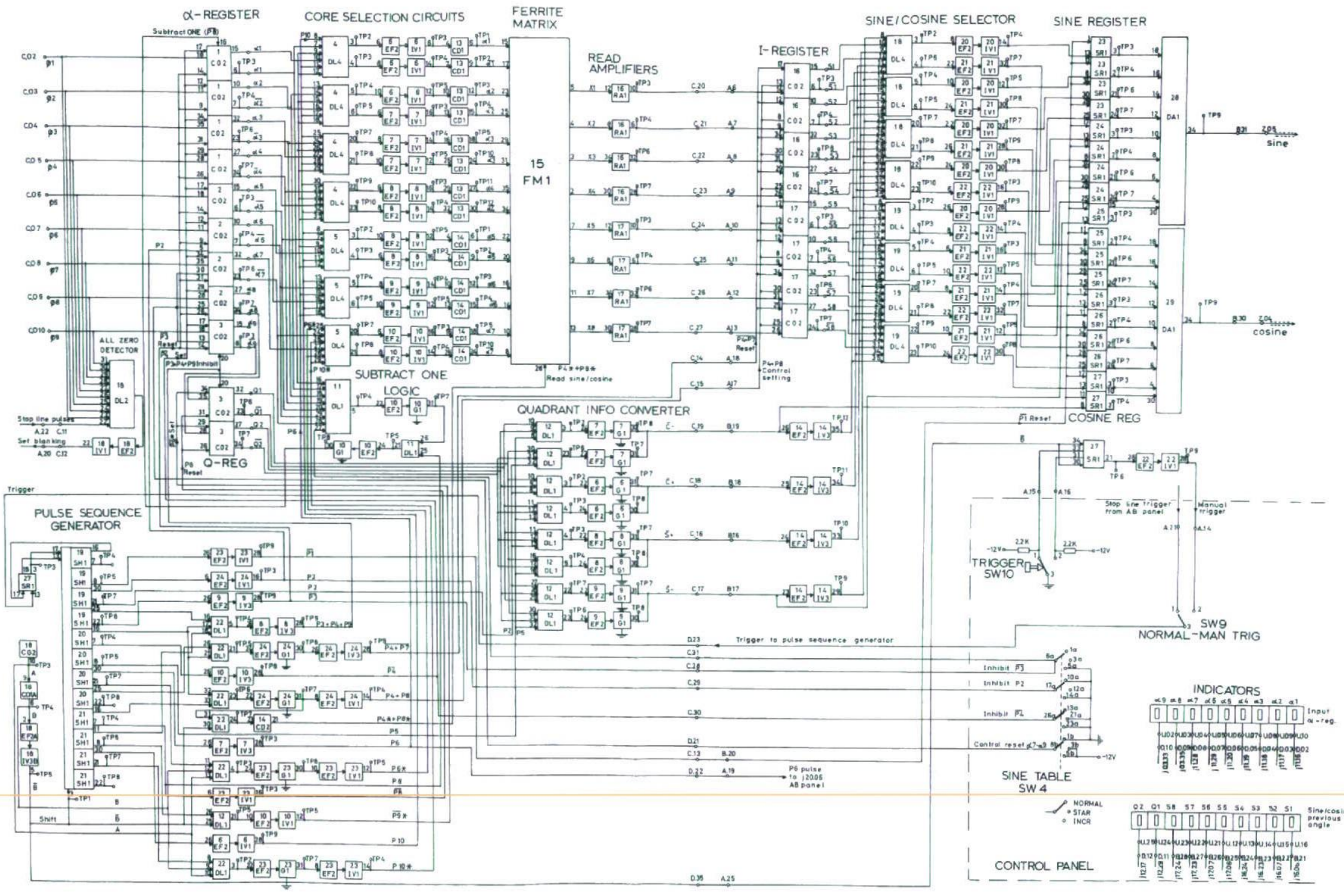


Figure 4.109 CSR sine/cosine converter, block diagram

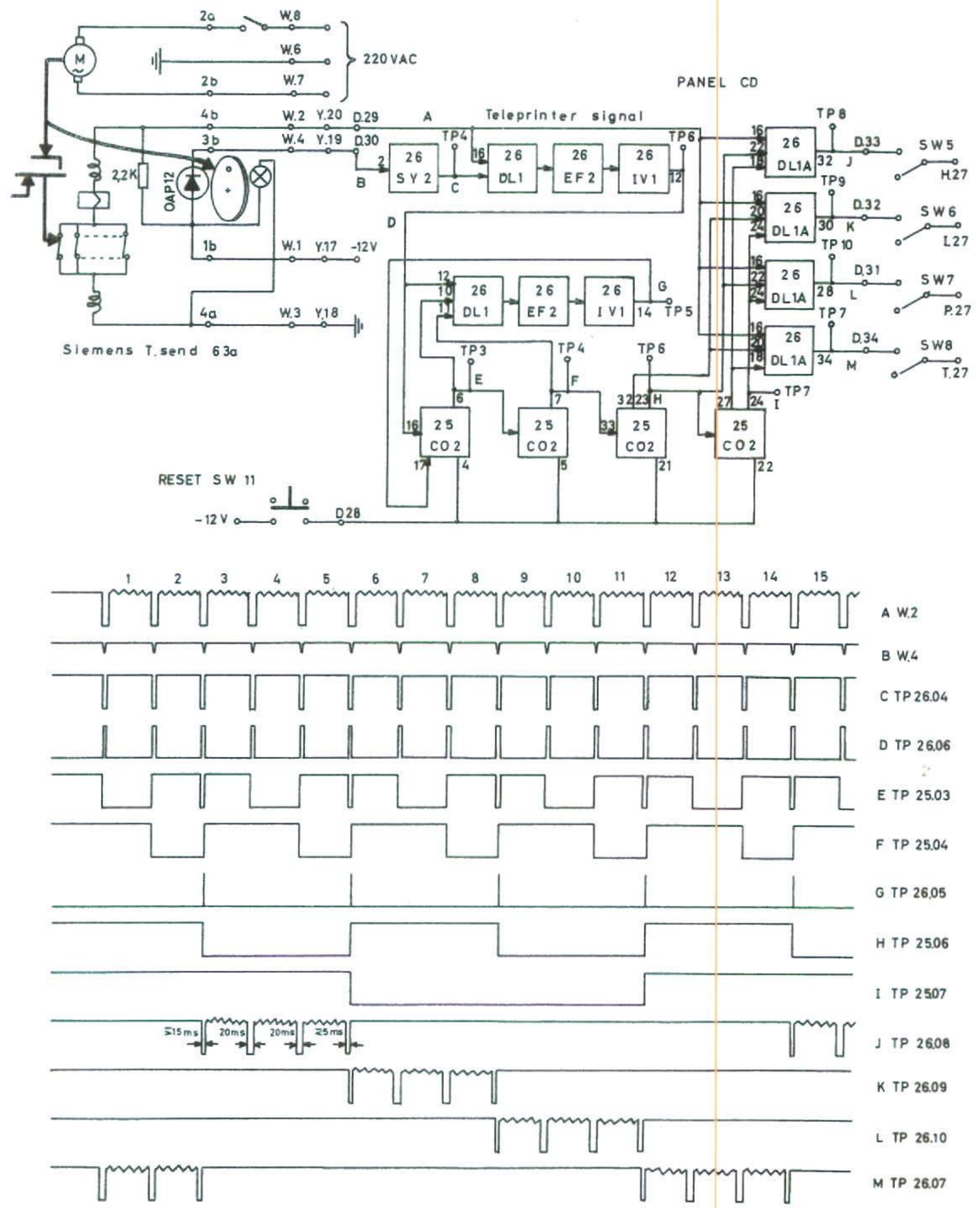


Figure 4.110 Teleprinter tape simulator

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THE DEVELOPMENT OF PASSIVE TRACKING SYSTEM

D A F

Final Project Report Mutual Weapons Development Program

Agreement No N-14-MWP-AF-62

NDRE REPORT No S8

Part III

FORSVARETS FORSKNINGSINSTITUTT
Norwegian Defence Research Establishment
PO Box 25 - Kjeller - Norway

May 1964

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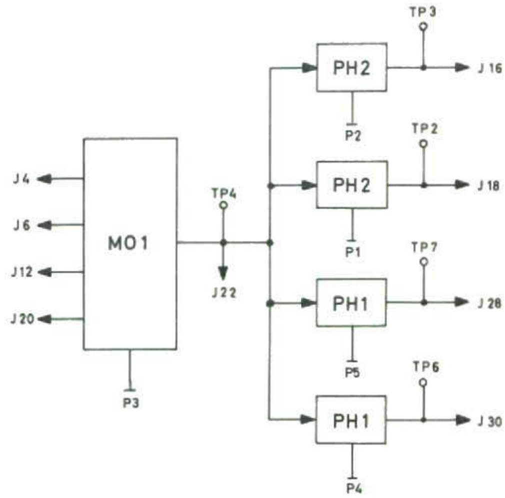
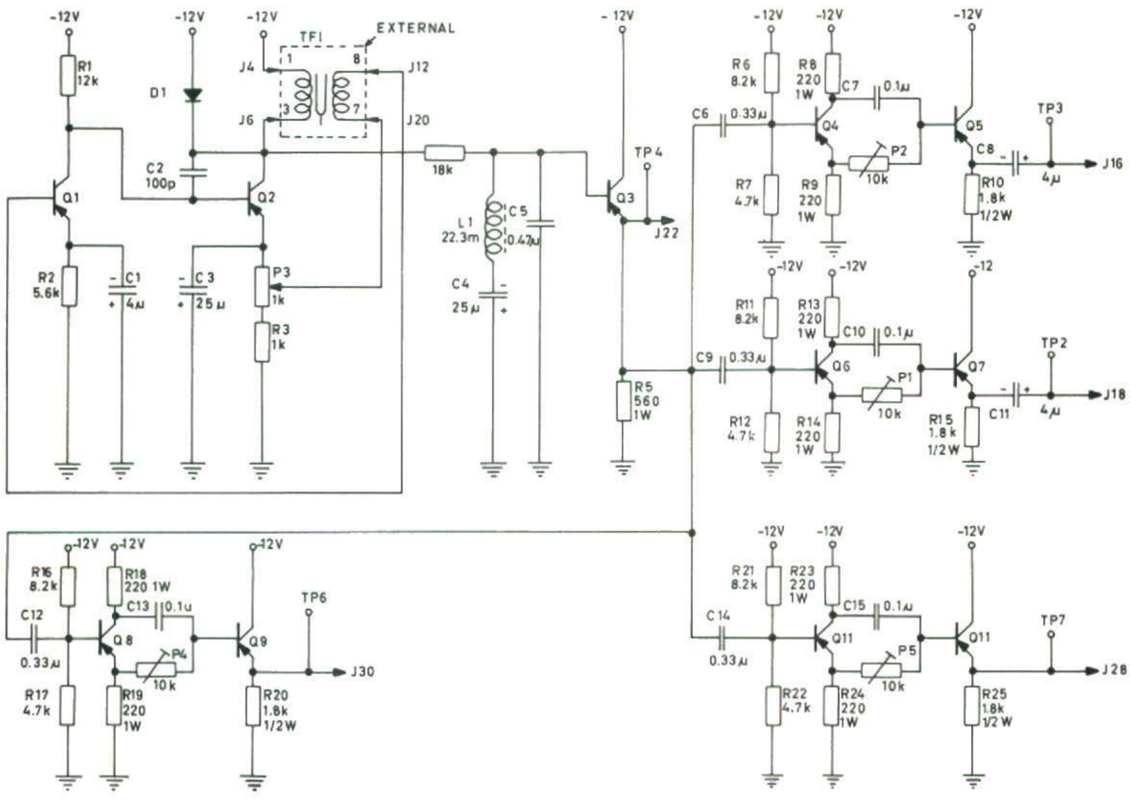
APPENDIX A

PRINTED CIRCUIT CARDS





-12 V: TP1, J2, J4

0 V: TP5, J24, J34

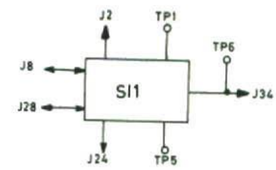
All resistors 1/4 W unless otherwise stated

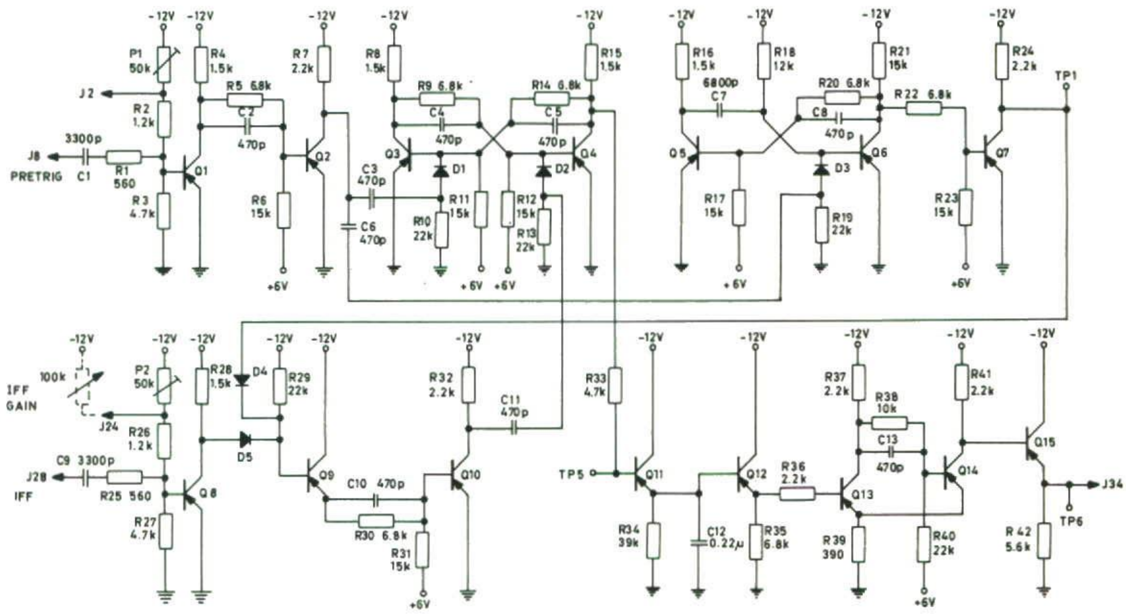
D1 : 0A202

Q1 - Q11: 2N525

Card type DAF 1/2

Date: 1.1.1964





-12 V: TP2, J4, J6

0 V: TP3, J10, J12, J14

J16, J22, J26, J30

+ 6 V: TP4, J18, J20

All resistors 1/4 W unless otherwise stated

D1 - D5 : 0A95

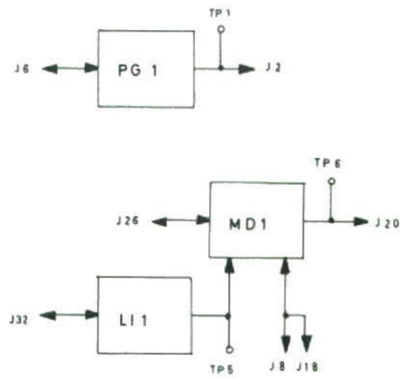
Q1 - Q6, Q8 - Q10: 2N395

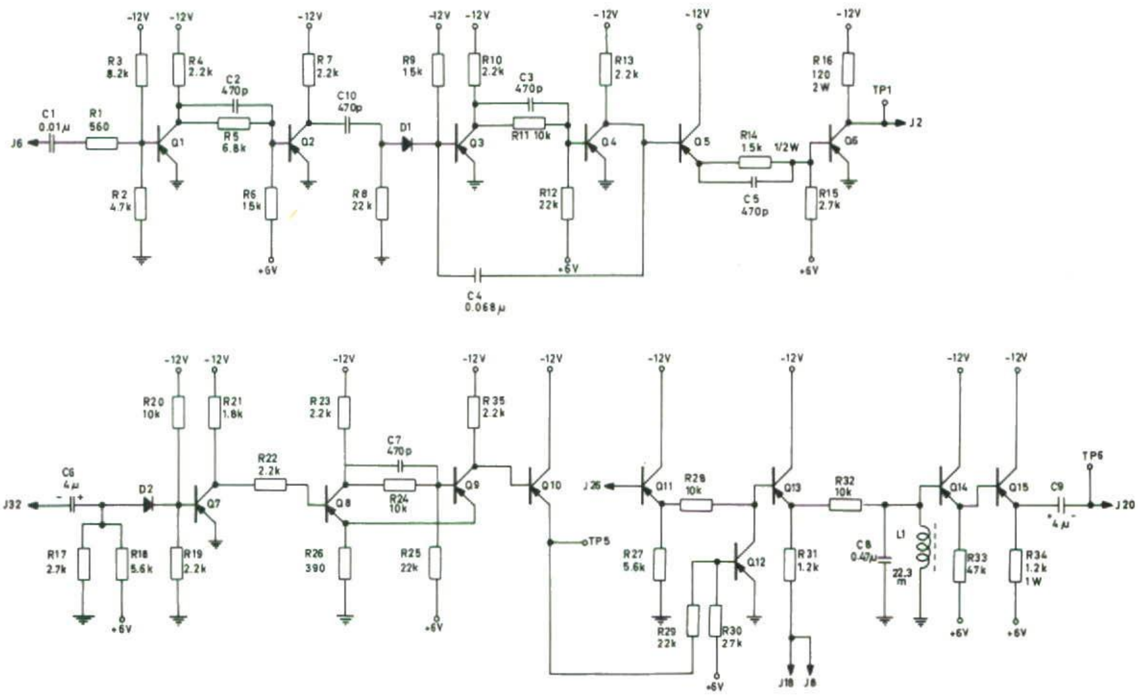
Q7, Q13 - Q15: 2N525

Q11 - Q12: 2S 302

Card type DAF 1/3

Date: 1.1.1964

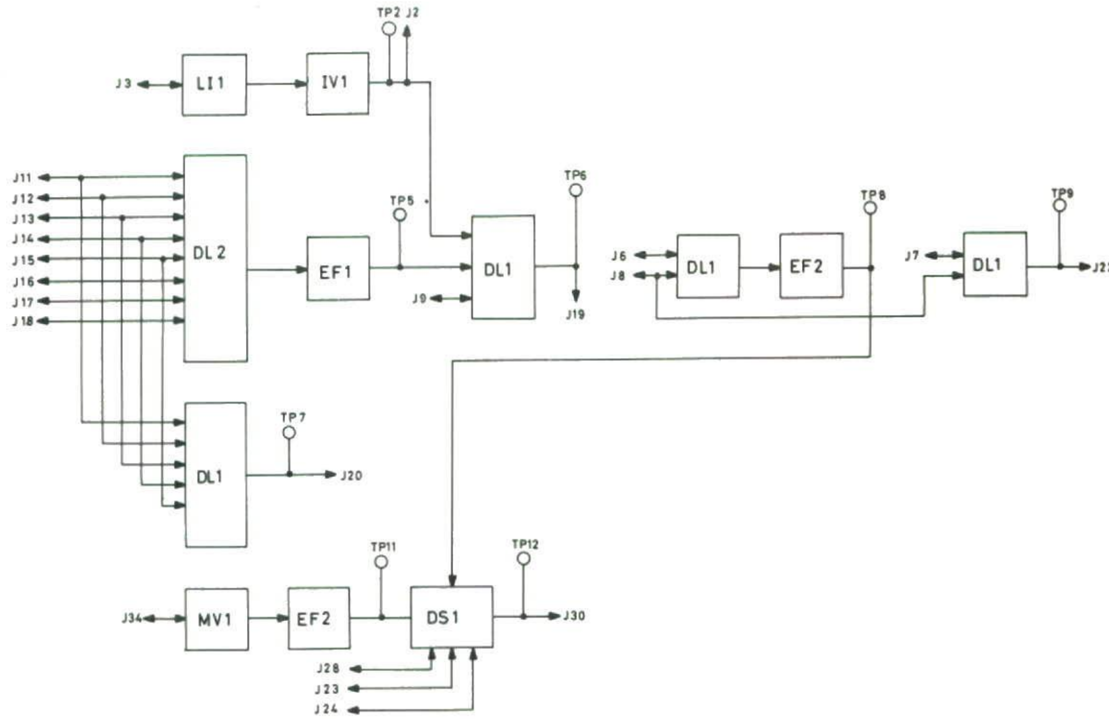


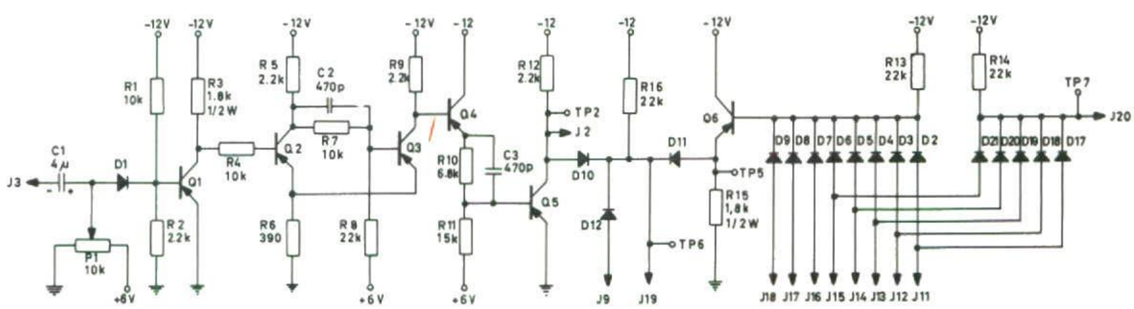


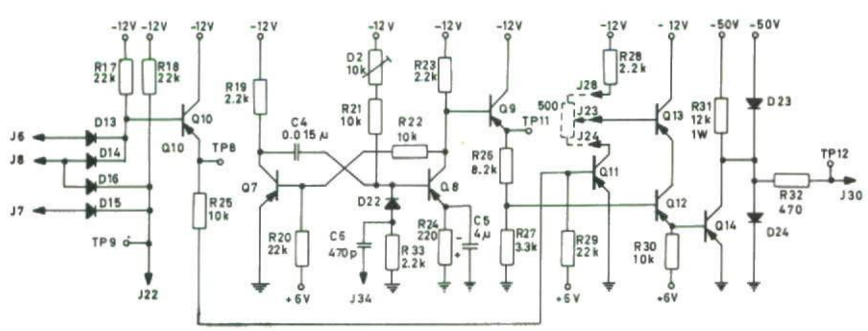
-12 V:	TP2, J24, J28	D1 :	0A95
0 V:	TP3, J16	D2 :	0A202
+ 6 V:	TP4, J34	Q1 - Q15:	2N525

All resistors 1/4 W unless otherwise stated

<u>Card type DAF 1/4A</u> Date: 1.1.1964





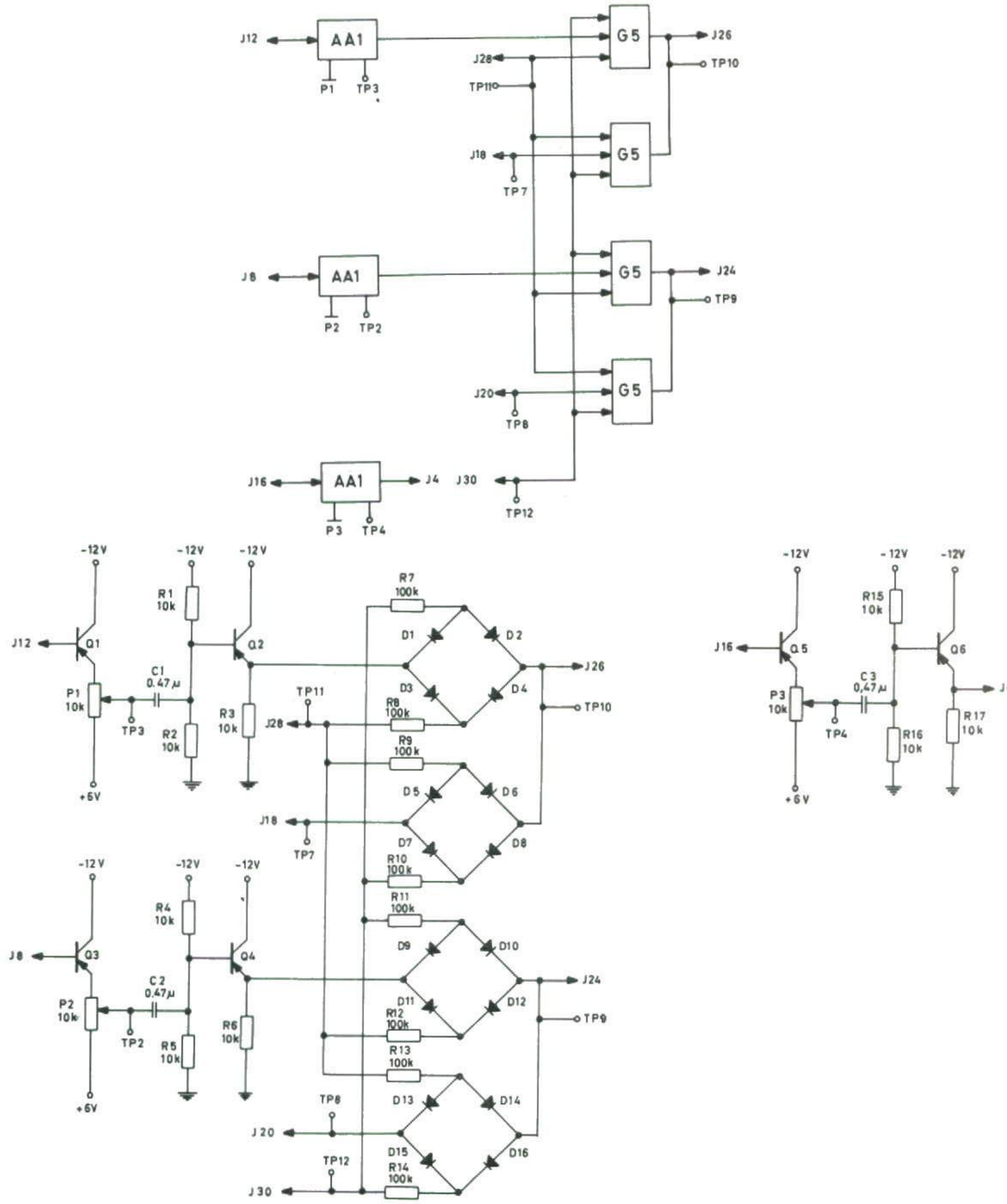


-50 V:	TP10, J26	D1 - D9, D22 - D24:	0A202
-12 V:	TP1, J10	D10 - D21:	0A95
0 V:	TP3, J4	Q1 - Q10:	2N525
+ 6 V:	TP4, J5, J32	Q11 - Q13:	2S 302
		Q14:	2S 301

All resistors 1/4 W unless otherwise stated

Card type DAF 1/5

Date: 1.1.1964



-12 V: TP1, J2, J6, J10, J14

0 V: TP5, J34

+ 6 V: TP6, J32

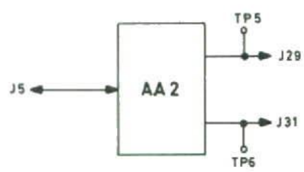
All resistors 1/4 W unless otherwise stated

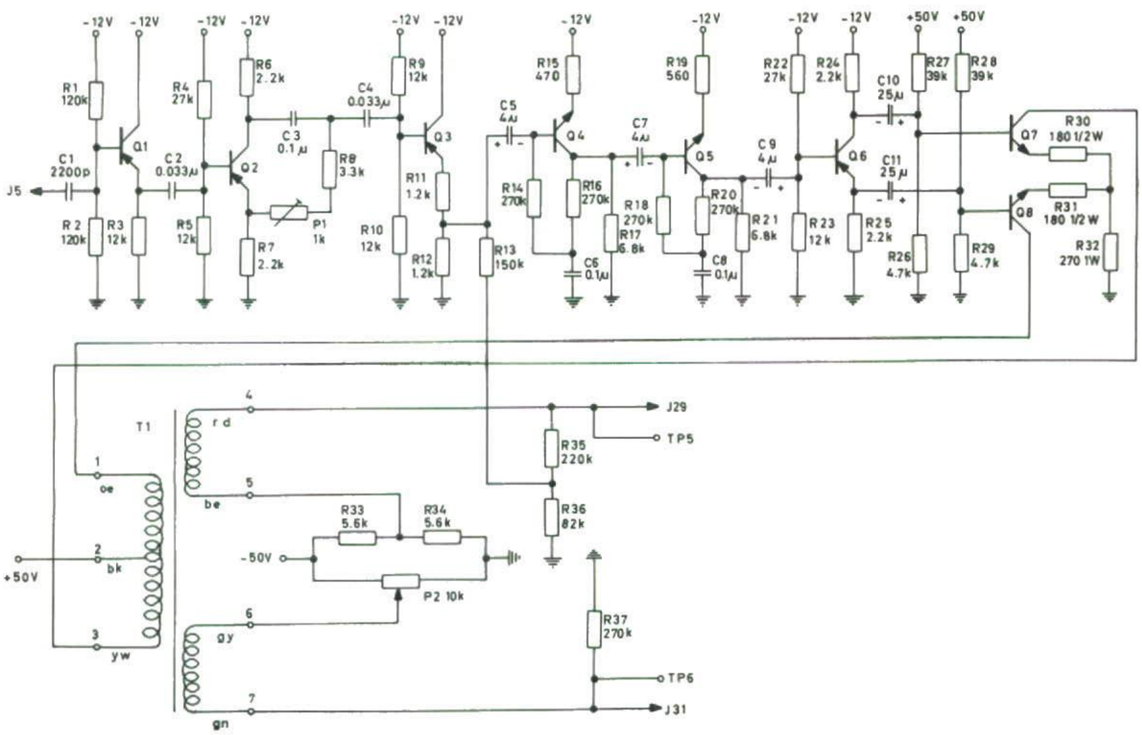
D1 - D16: 0A202

Q1 - Q6 : 2N525

Card type DAF 1/8

Date: 1.1.1964





-50 V: TP2, J3

-12 V: TP1, J9

0 V: TP3, J19

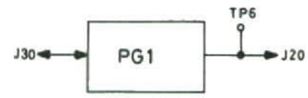
+50 V: TP4, J33

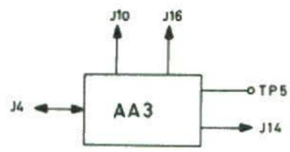
All resistors 1/4 W unless otherwise stated

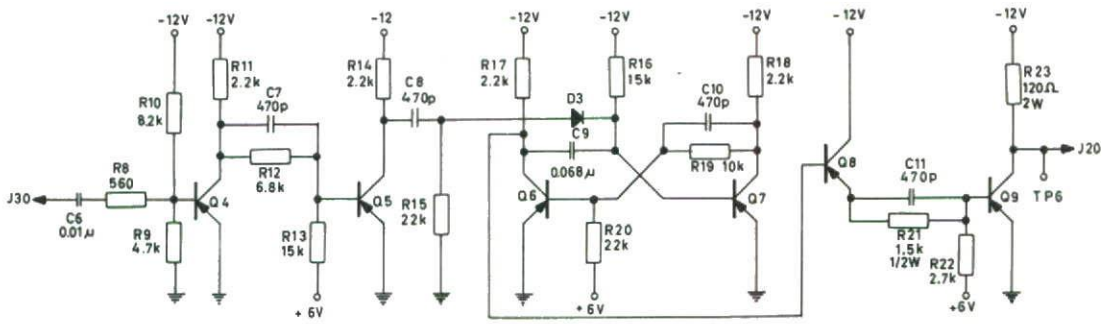
Q1 - Q3, Q6:	2S303
Q4 - Q5:	2N1711
Q7 - Q8:	2N699

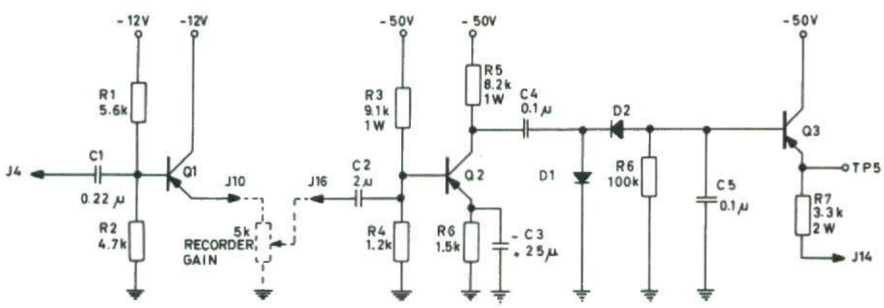
Card type DAF 1/9

Date: 1.1.1964









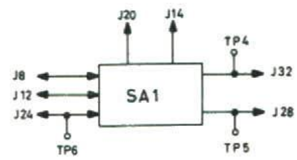
-50 V: TP2, J12
-12 V: TP1, J8
0 V: TP3, J2, J6, J18, J22, J28, J32
+ 6 V: TP4, J34

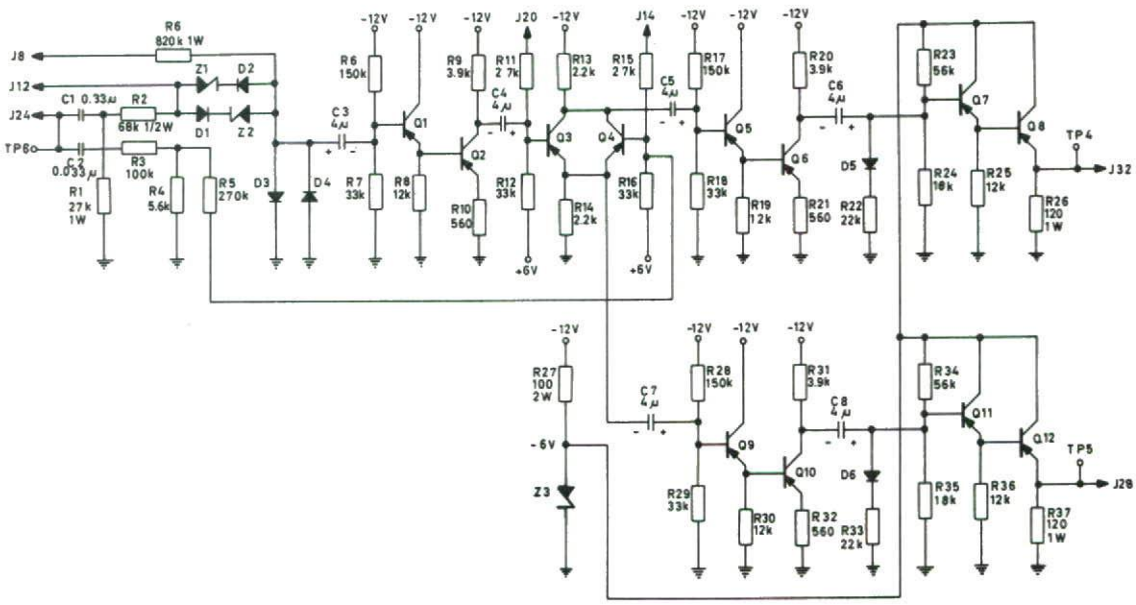
All resistors 1/4 W unless otherwise stated

D1 - D2 : 0A202
D3 : 0A95
Z1 : 104Z4
Q1, Q4 - Q9 : 2N525
Q2 - Q3 : 2S 301 (Q3 w/heat sink)

Card type DAF 1/10

Date: 1.1.1964



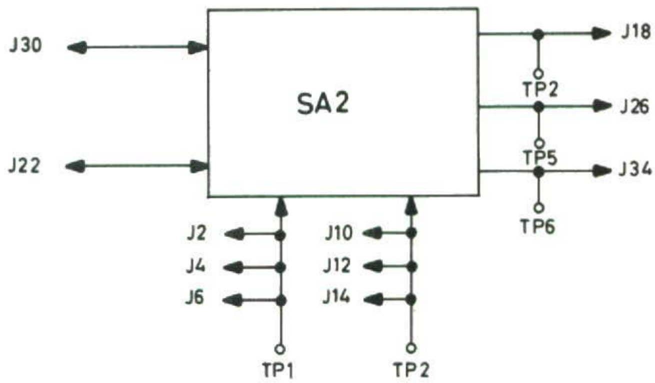


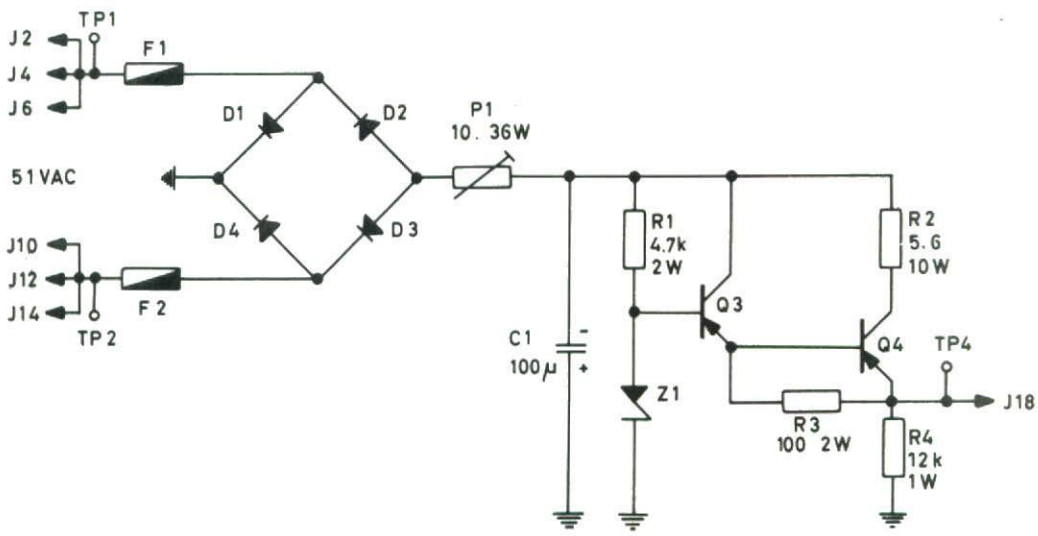
-12 V:	TP1, J2, J4	D1 - D6 :	0A202
0 V:	TP2, J6, J10, J18, J22,	Z1 - Z2 :	104Z4
	J26, J30, J34	Z3 :	ZL6
+ 6 V:	TP3, J16	Q1 - Q12:	2S 302

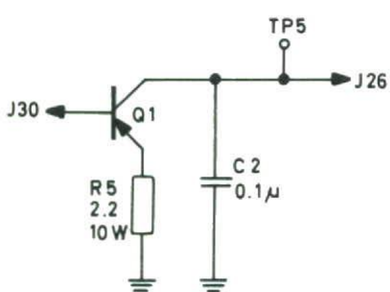
All resistors 1/4 W unless otherwise stated

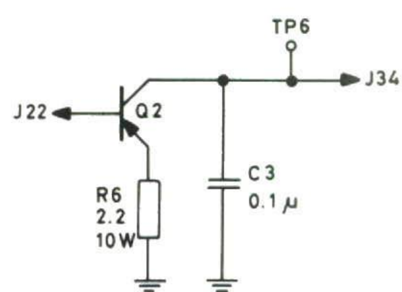
Card type DAF 1/11

Date: 1.1.1964







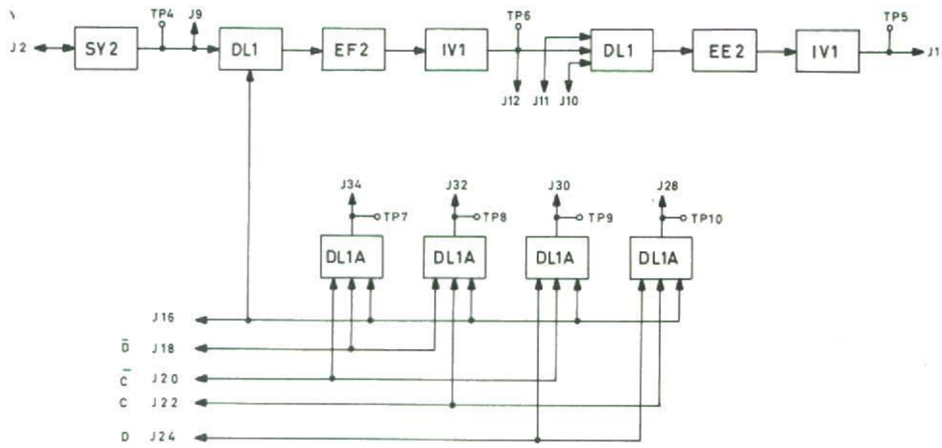


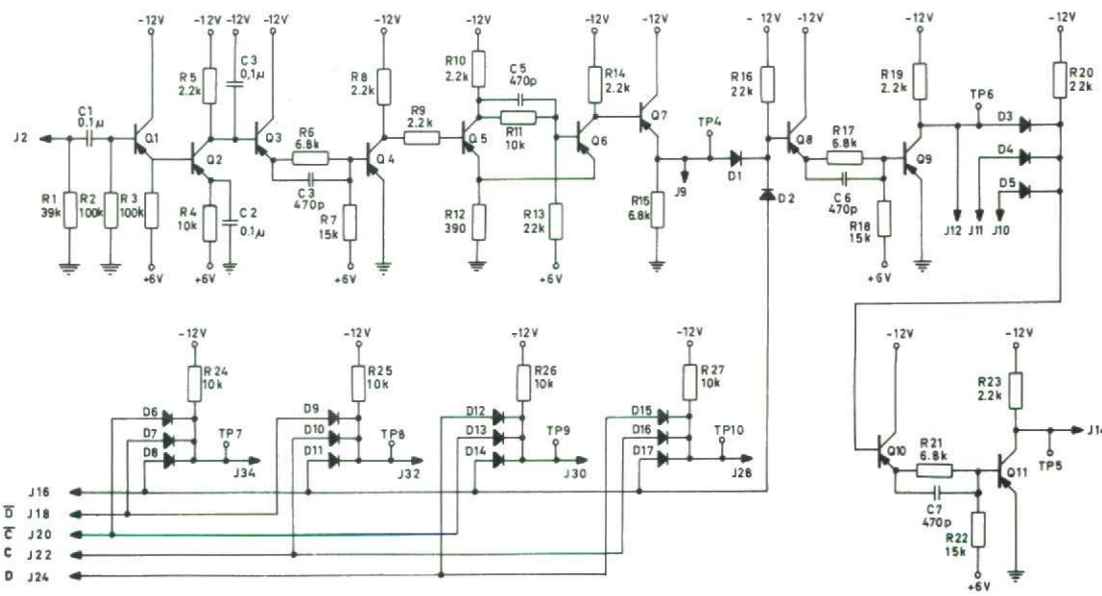
0 V: TP3, J8, J16, J20,
J24, J28, J32

D1 - D4	:	0Y5061
Z1	:	ZL33
Q1, Q2, Q4	:	147T1 (w/heat sink)
Q3	:	147T1

Card type DAF 1/12

Date: 1.1.1964





-12 V: TP1, J4

0 V: TP2, J6

+ 6 V: TP3, J8

All resistors 1/4 W unless otherwise stated

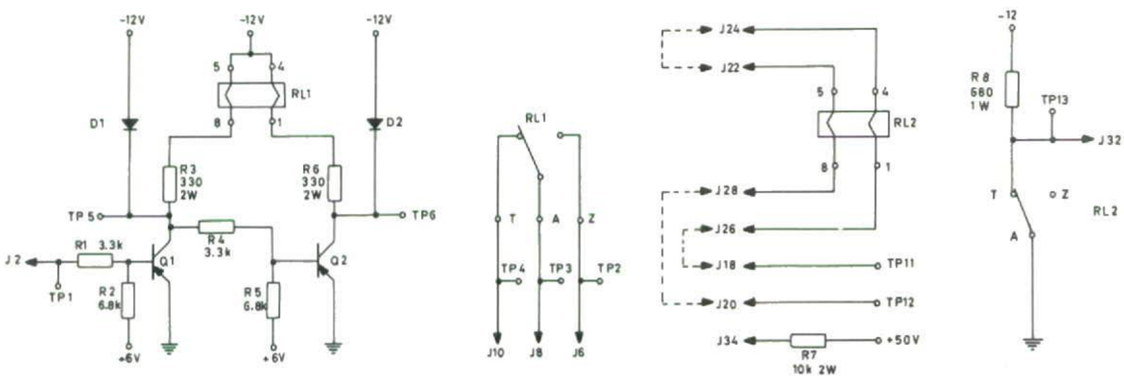
D1 - D17: 0A95

Q1 : 2S 302

Q2 - Q11: 2N525

<u>Card type DAF 1/13</u>

Date: 1.1.1964



-12 V: TP9, J4

0 V: TP8, J12, J30

+ 6 V: TP7, J14

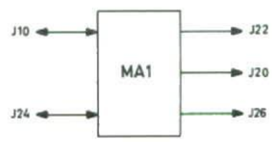
+50 V: TP10, J16

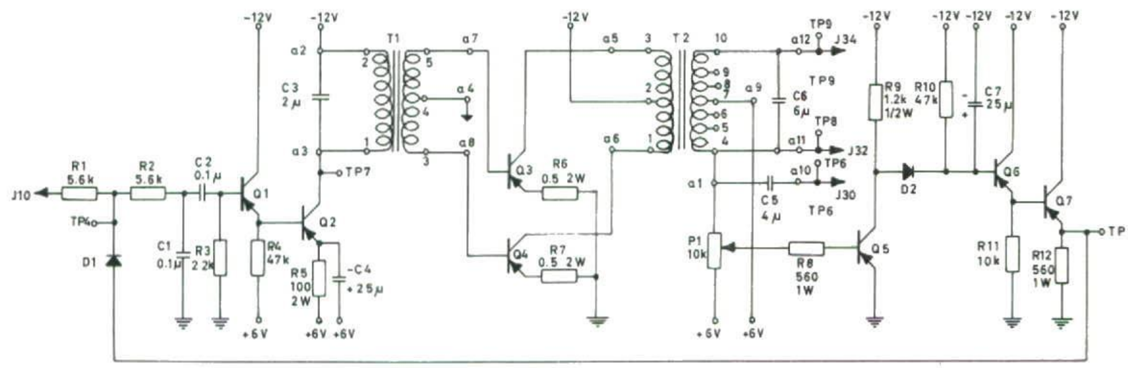
All resistors 1/4 W unless otherwise stated

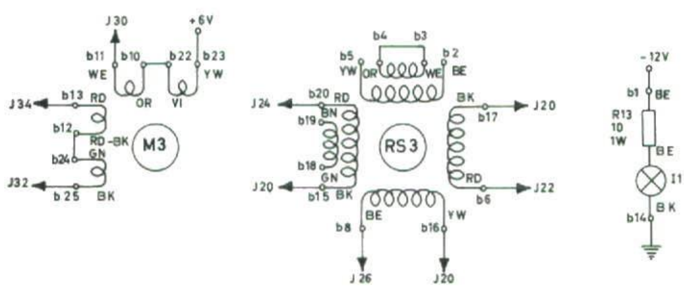
Card type DAF 1/14

D1 - D2	:	0A95
Q1 - Q2	:	2N525
RL1 - RL2	:	Siemens T rls 63 w
		T Bv 3302/36

Date: 1.1.1964







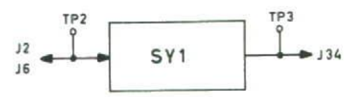
-12 V:	TP1, J4
0 V:	TP3, J2, J6
+ 6 V:	TP2, J8

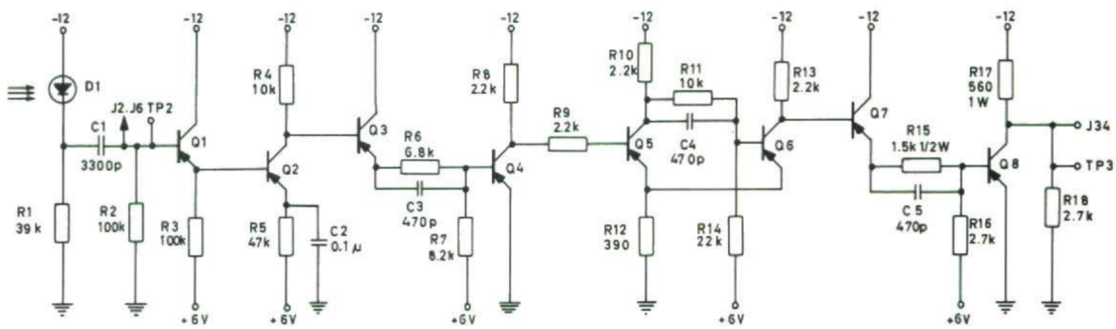
D1 - D2	:	0A202
Q1, Q5, Q7	:	2N525
Q2 - Q4	:	147T1 (w/heat sink)
Q6	:	2S 302
I1	:	Philips 8089N
M3	:	Kearfott R172-002
RS3	:	Kearfott R980-41A

All resistors 1/4 W unless otherwise stated

Card type DAF 1/15

Date: 1.1.1964





-12 V: TP1, J4

0 V: TP4, J30

+ 6 V: TP5, J32

All resistors 1/4 W unless otherwise stated

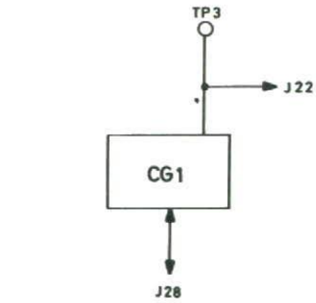
D1 : 0AP12

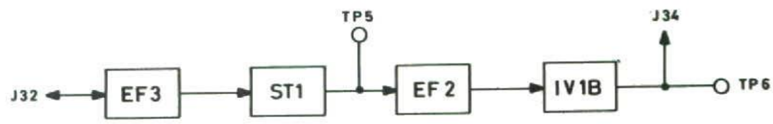
Q1 : 2S 302

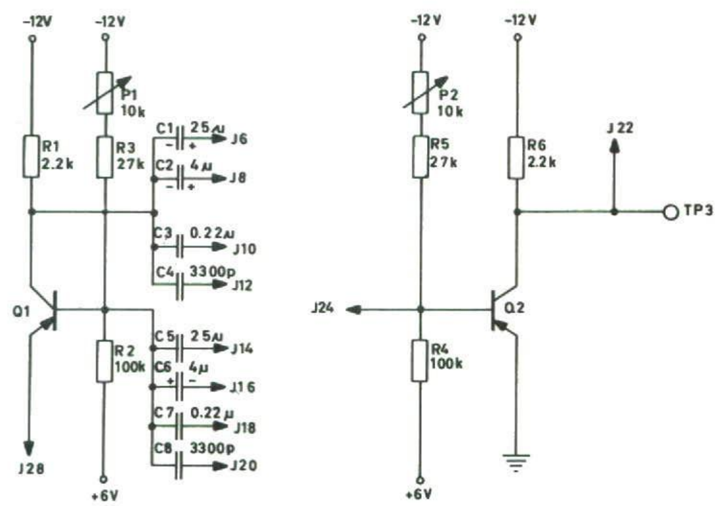
Q2 - Q8 : 2N525

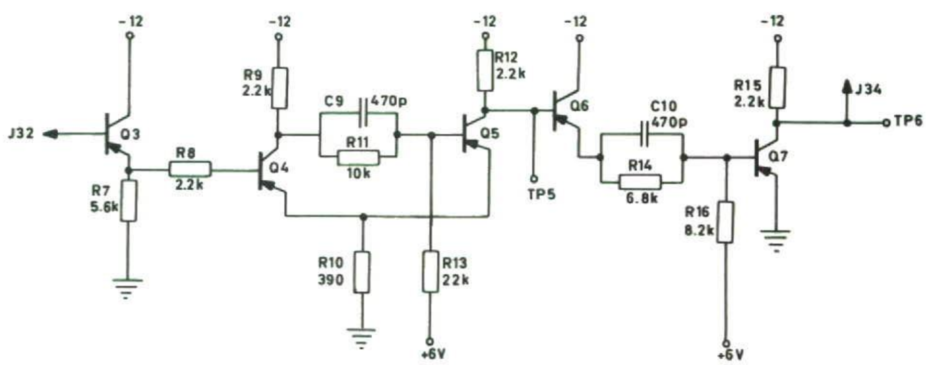
<u>Card type DAF 1/16</u>

Date: 1. 1. 1964









-12 V: TP2, J4

0 V: TP4, J30

+ 6 V: TP1, J2

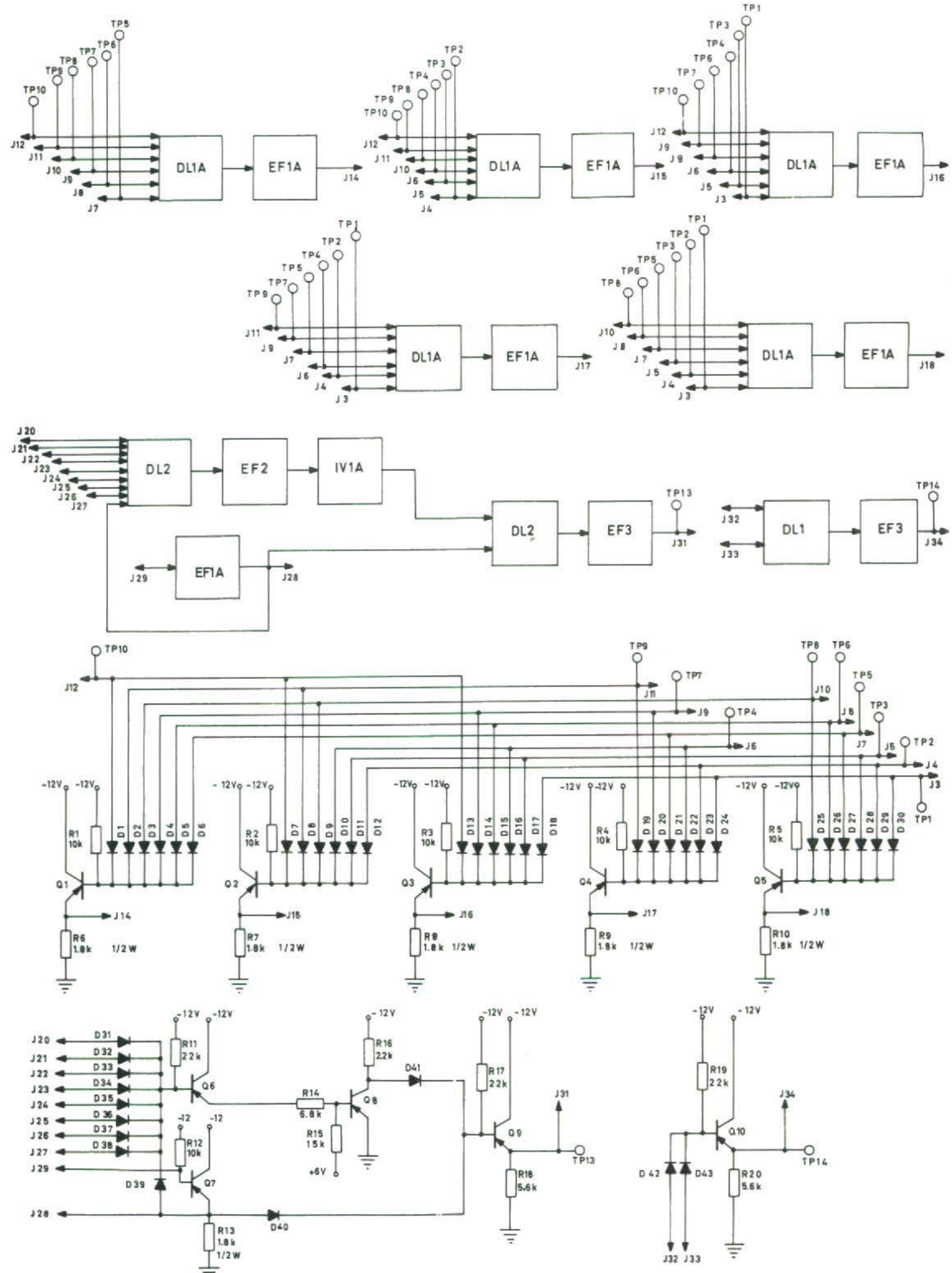
All resistors 1/4 W unless otherwise stated

Q1 - Q2 : 2S 303

Q3 - Q7 : 2N525

<u>Card type DAF 2/3</u>

Date: 1.1.1964



-12 V: TP11, J13

0 V: TP12, J19, J30

+ 6 V: TP15, J35

All resistors 1/4 W unless otherwise stated

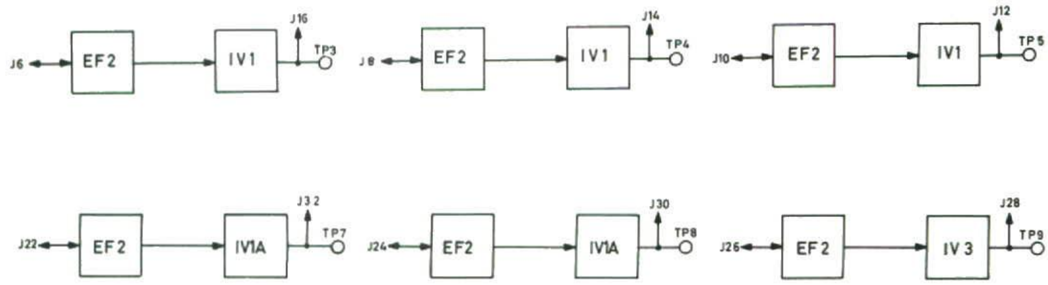
D1 - D30, D42 - D43: 0A95

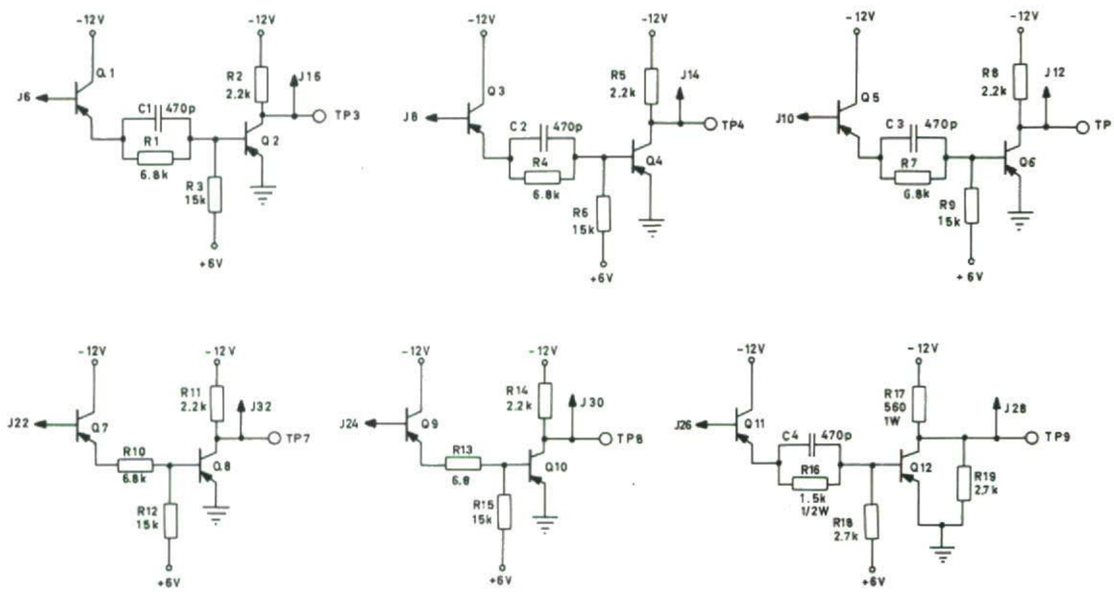
D31 - D41: 0A202

Q1 - Q10: 2N525

Card type DAF 2/6

Date: 1.1.1964





-12 V: TP2, J4

0 V: TP6, J18, J34

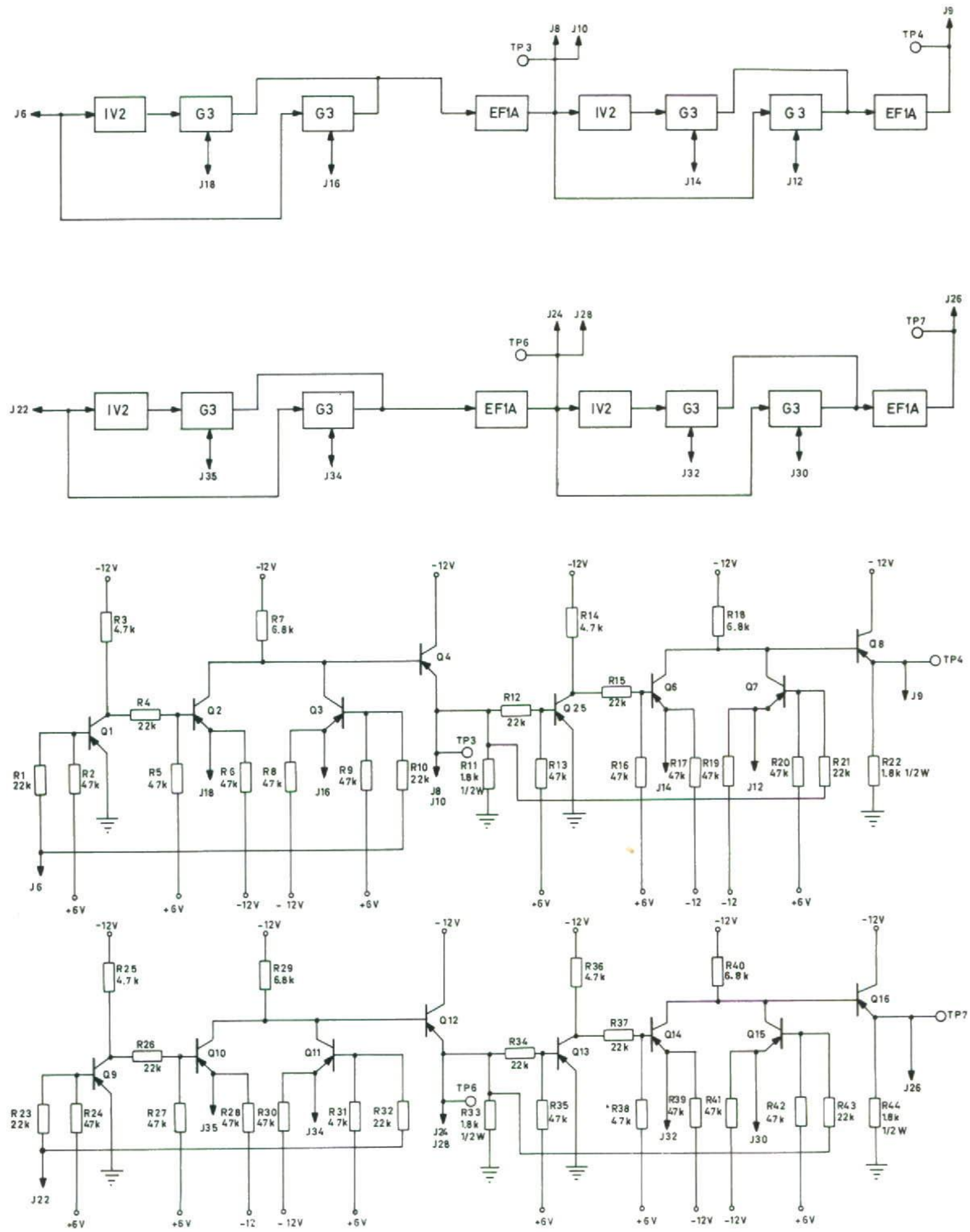
+ 6 V: TP1, J2

All resistors 1/4 W unless otherwise stated

Q1 - Q12: 2N525

Card type DAF 2/7

Date: 1.1.1964



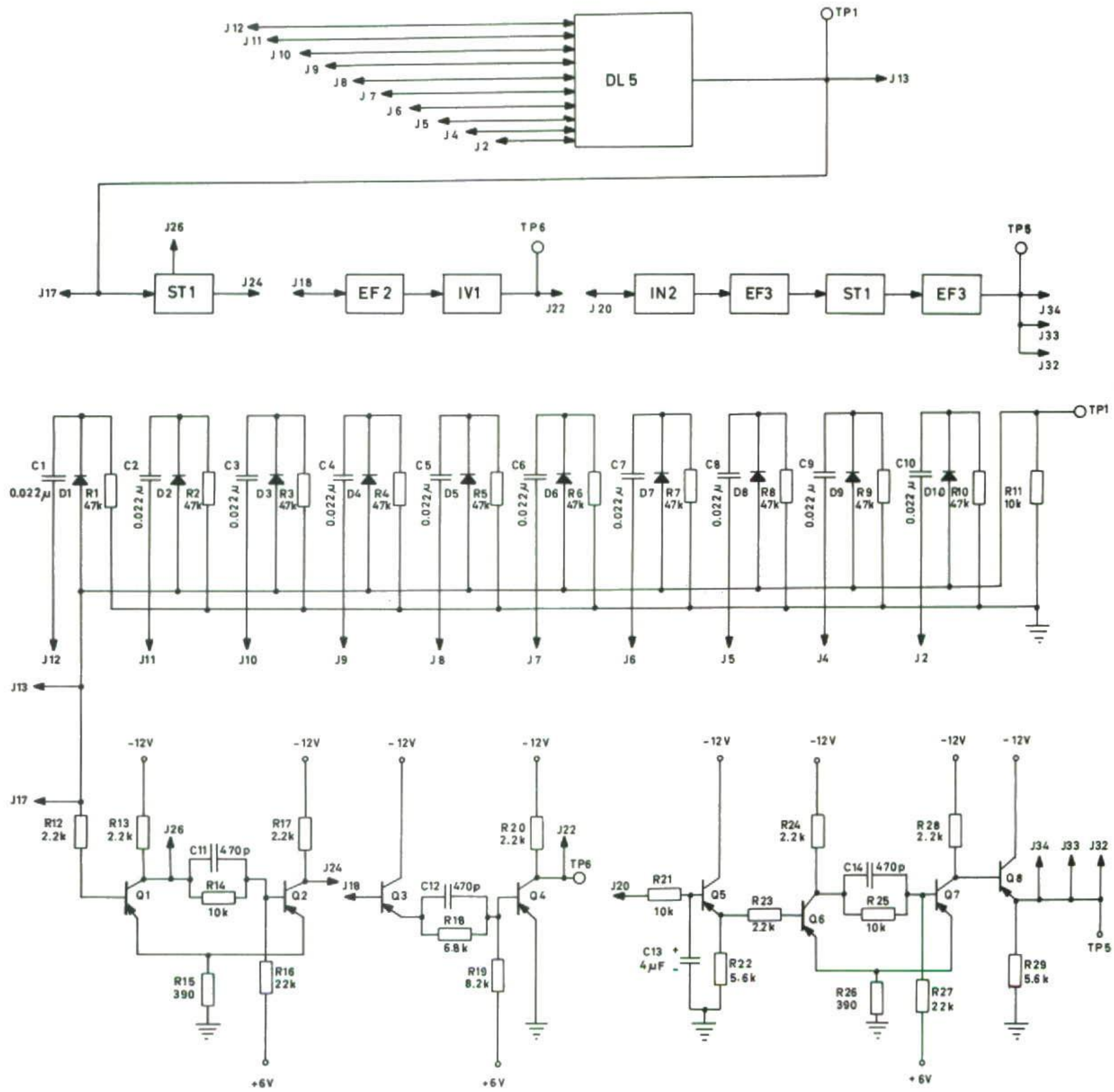
-12 V: TP2, J4 Q1 - Q3, Q5 - Q7, Q9 - Q11, Q13 - Q15: 2N395

0 V: TP5, J20 Q4, Q8, Q12, Q16: 2N525

+ 6 V: TP1, J2

All resistors 1/4 W unless otherwise stated

<u>Card type DAF 2/8</u> Date: 1.1.1964



-12 V: TP4, J16

0 V: TP2, J14

+ 6 V: TP3, J15

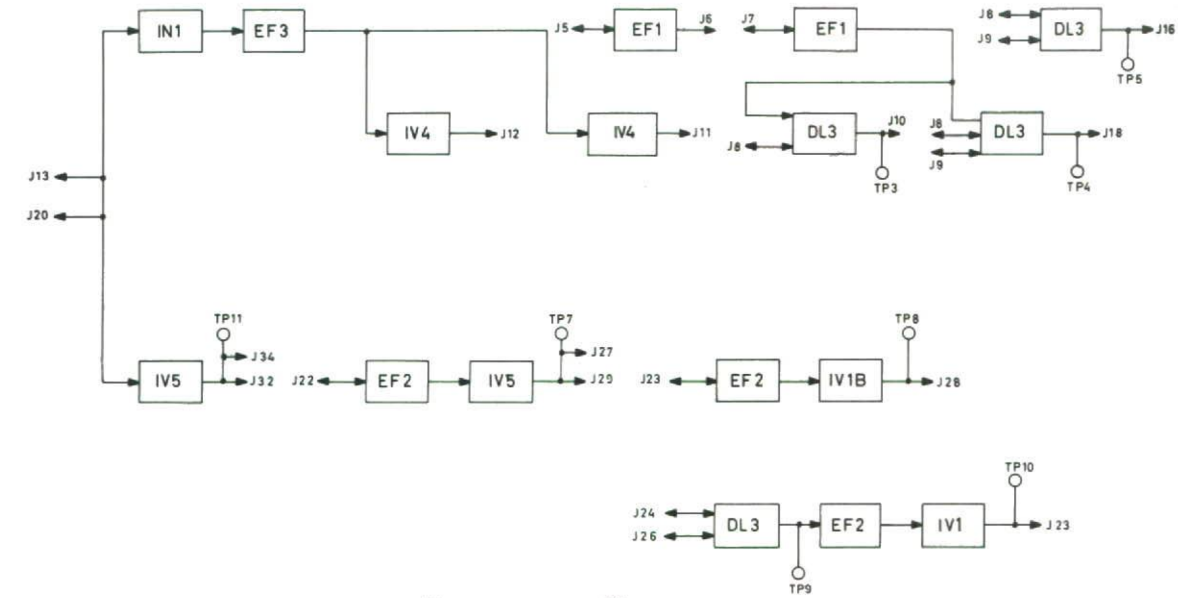
All resistors 1/4 W unless otherwise stated

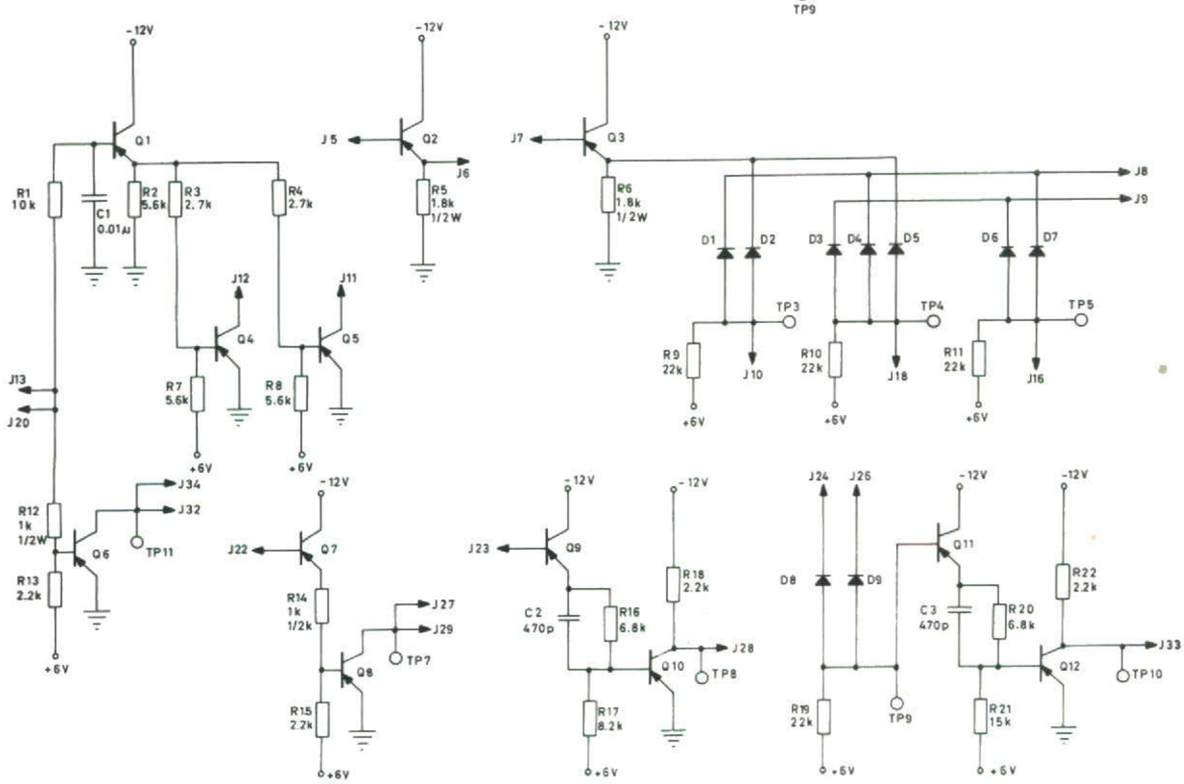
D1 - D10: 0A95

Q1 - Q8 : 2N525

Card type DAF 2/9

Date: 1.1.1964





-12 V: TP2, J4

0 V: TP6, J14

\+ 6 V: TP1, J2

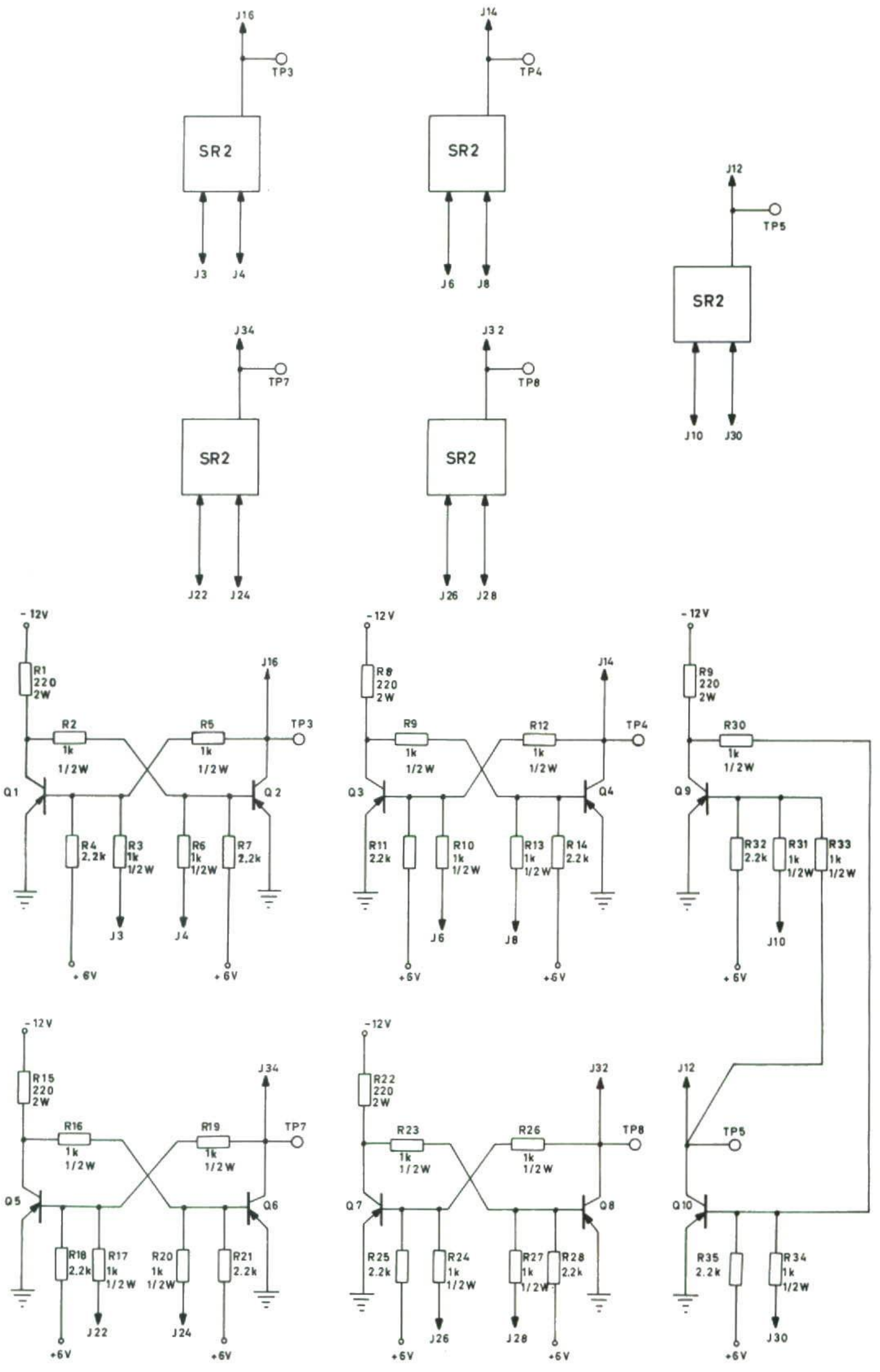
All resistors 1/4 W unless otherwise stated

D1 - D9 : 0A202

Q1 - Q12: 2N525

<u>Card type DAF 2/10</u>

Date: 1.1.1964



-12 V: TP1, J2

0 V: TP6, J18

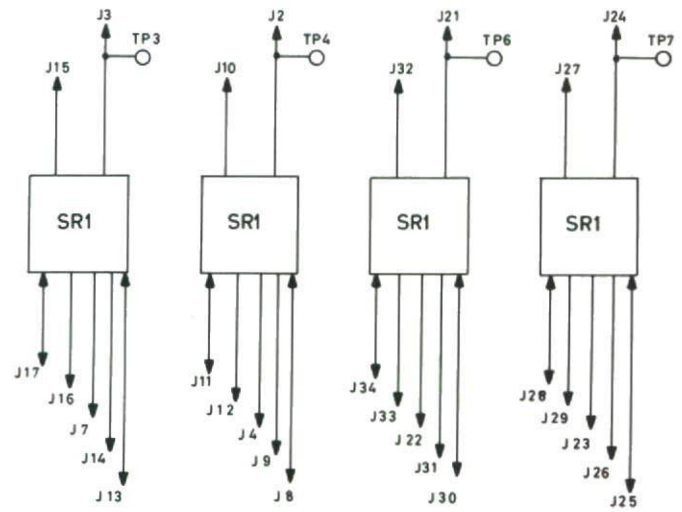
+ 6 V: TP2, J20

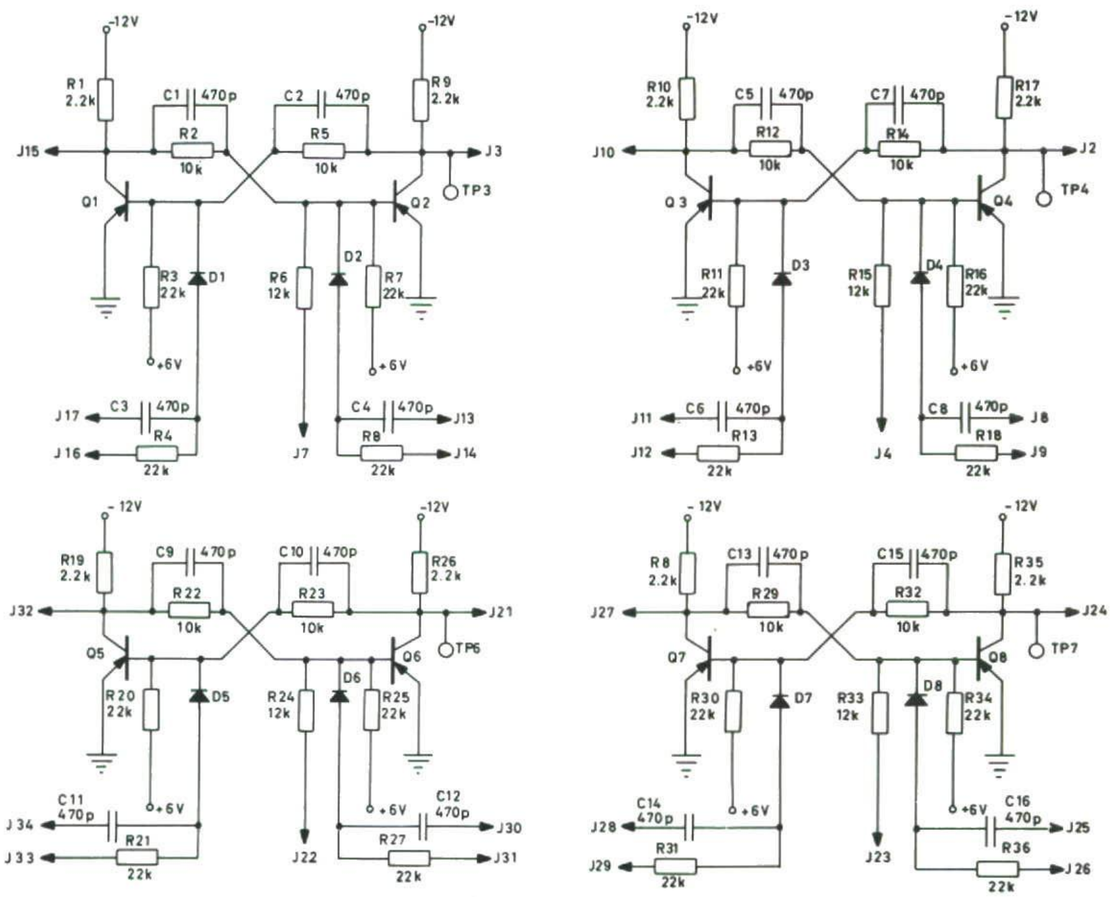
All resistors 1/4 W unless otherwise stated

Q1 - Q10: 2N525

<u>Card type DAF 2/11</u>

Date: 1.1.1964





-12 V: TP1, J5, J20

0 V: TP5, J18, J19, J35

+ 6 V: TP2, J6

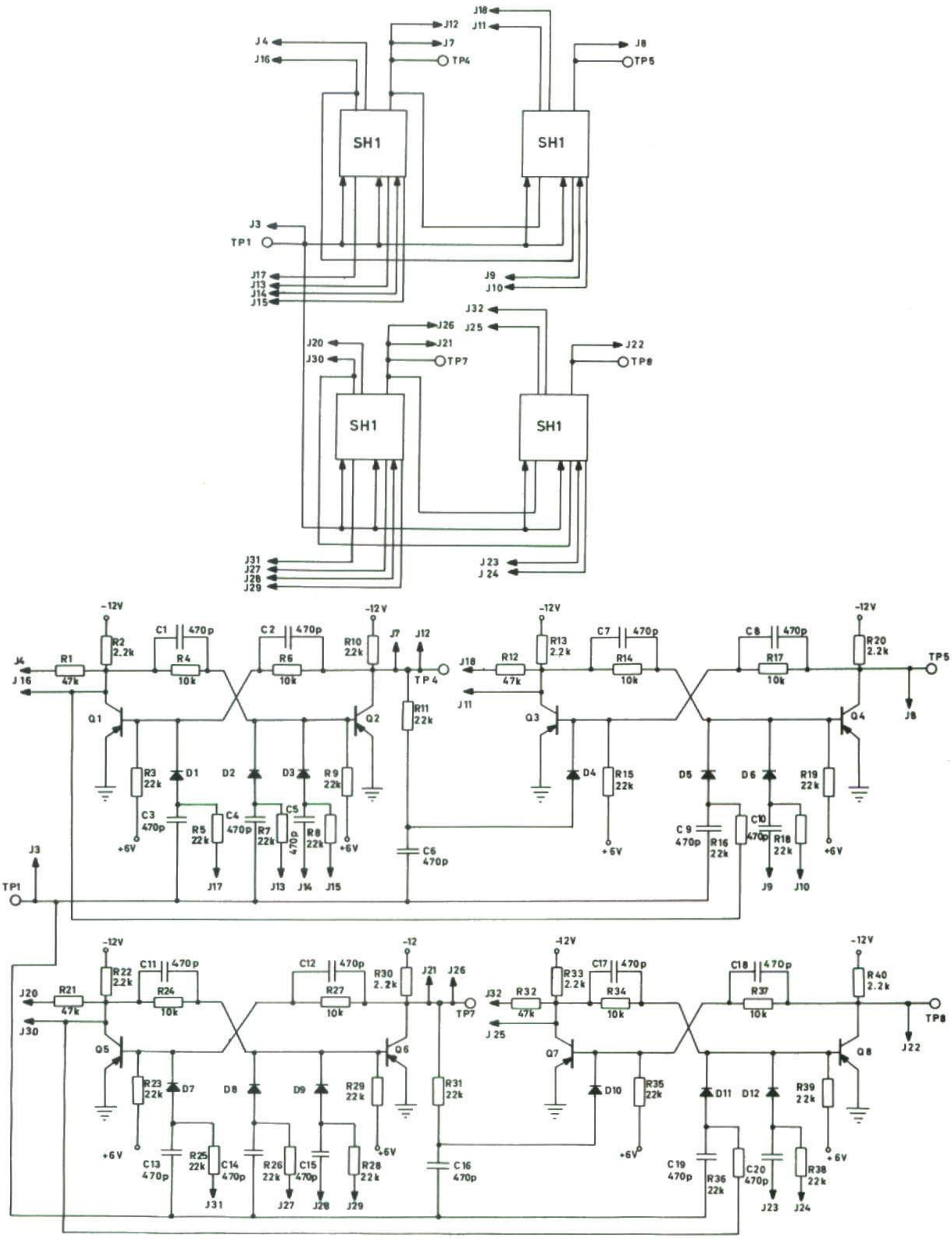
All resistors 1/4 W unless otherwise stated

D1 - D8 : 0A95

Q1 - Q8 : 2N525

<u>Card type DAF 2/12</u>

Date: 1.1.1964



-12 V: TP2, J2, J5

0 V: TP6, J19, J33, J34, J35

+ 6 V: TP3, J6

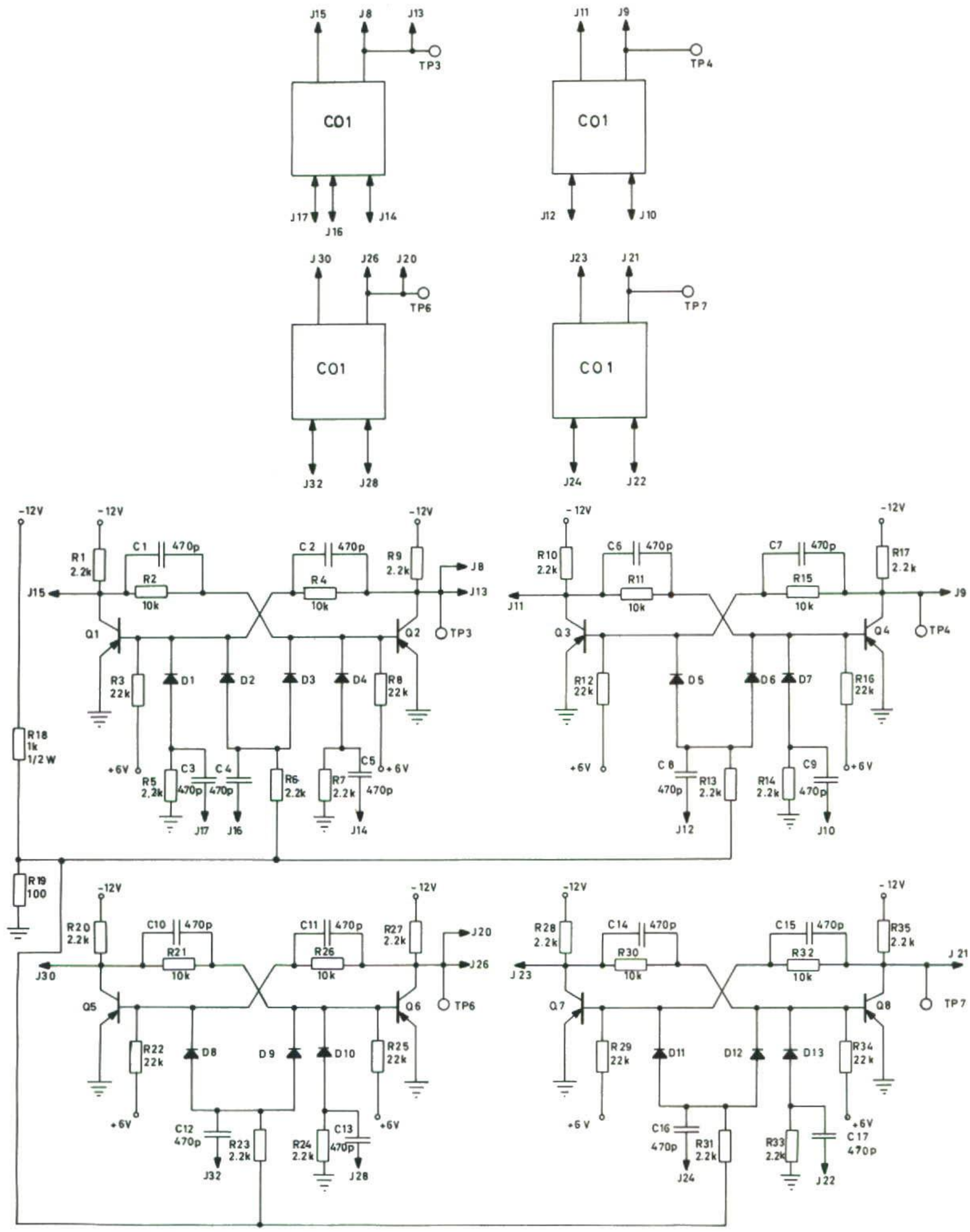
All resistors 1/4 W unless otherwise stated

D1 - D12: 0A95

Q1 - Q8 : 2N525

<u>Card type DAF 2/13</u>

Date: 1.1.1964



-12 V: TP1, J2, J3, J4

0 V: TP5, J18, J19, J33, J34

+ 6 V: TP2, J6

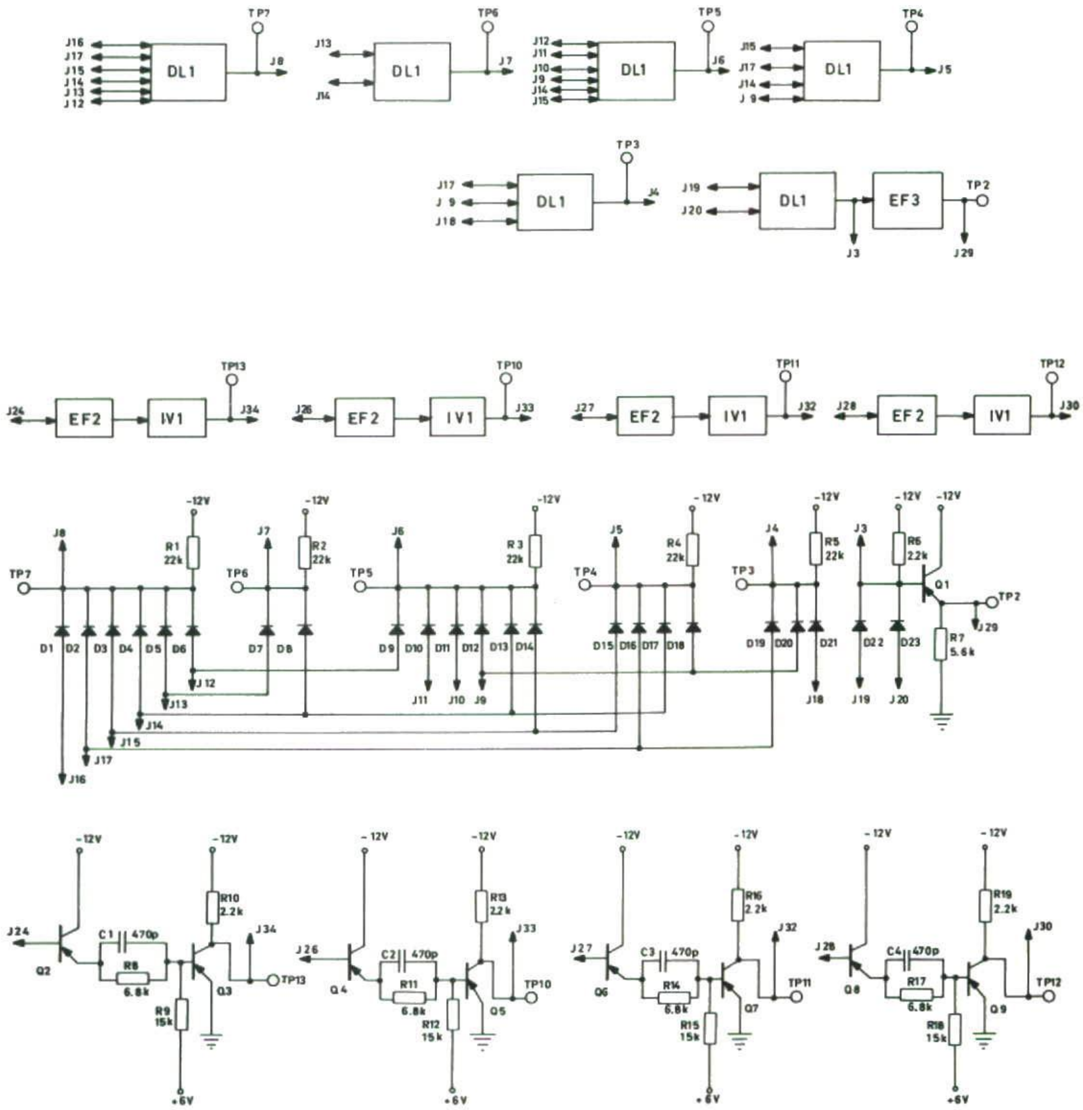
All resistors 1/4 W unless otherwise stated

D1 - D13: 0A95

Q1 - Q8 : 2N525

<u>Card type DAF 2/14</u>

Date: 1.1.1964



-12 V: TP1, J2

0 V: TP9, J21

+ 6 V: TP8, J22

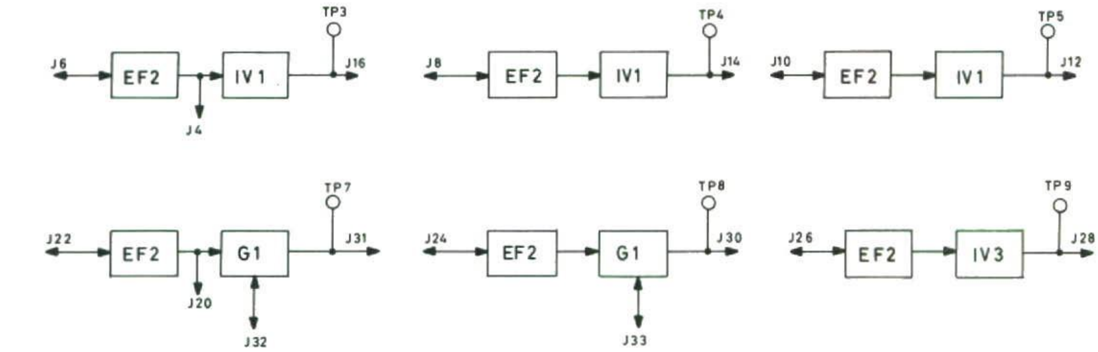
All resistors 1/4 W unless otherwise stated

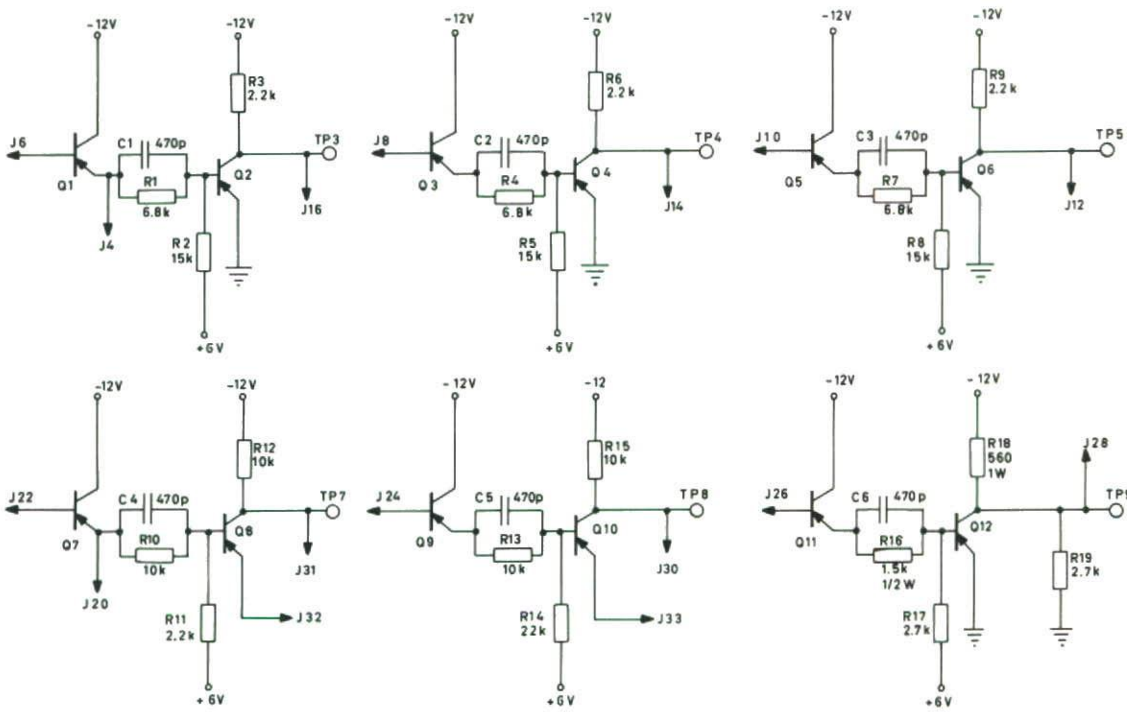
D1 - D23: 0A95

Q1 - Q9 : 2N525

Card type DAF 2/15

Date: 1.1.1964





-12 V: TP2, J3

0 V: TP6, J18, J34, J35

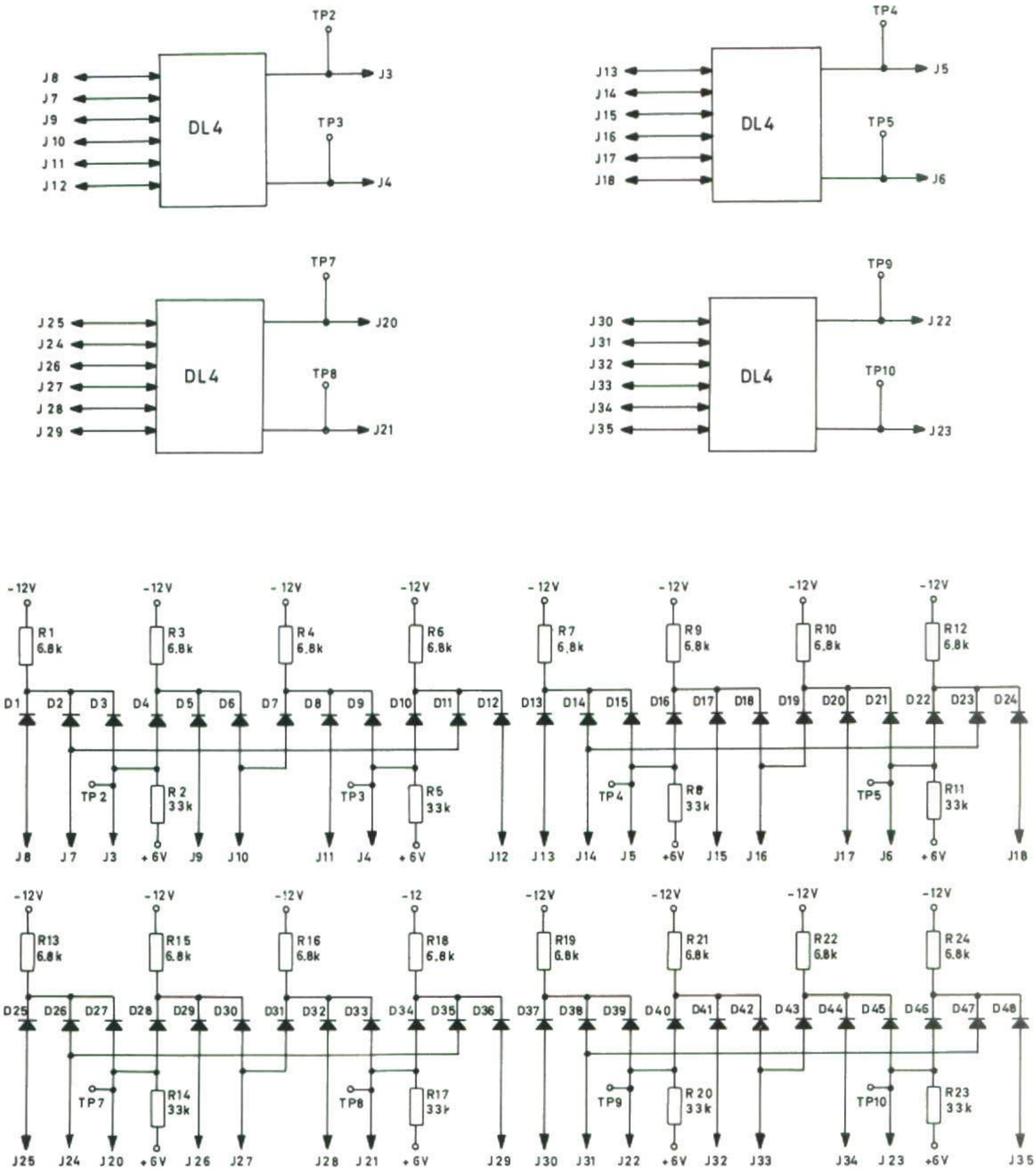
+ 6 V: TP1, J2

All resistors 1/4 W unless otherwise stated

Q1 - Q12: 2N525

Card type DAF 2/16

Date: 1.1.1964



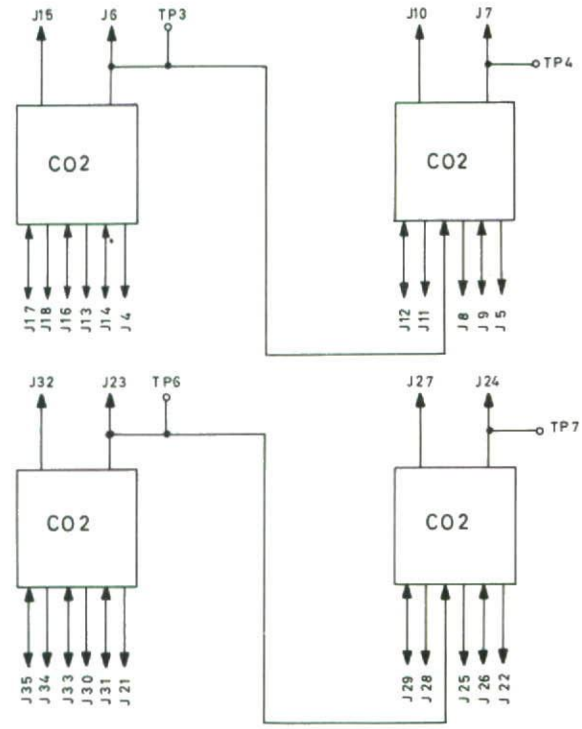
-12 V: TP1, J2 D1 - D48: 0A95

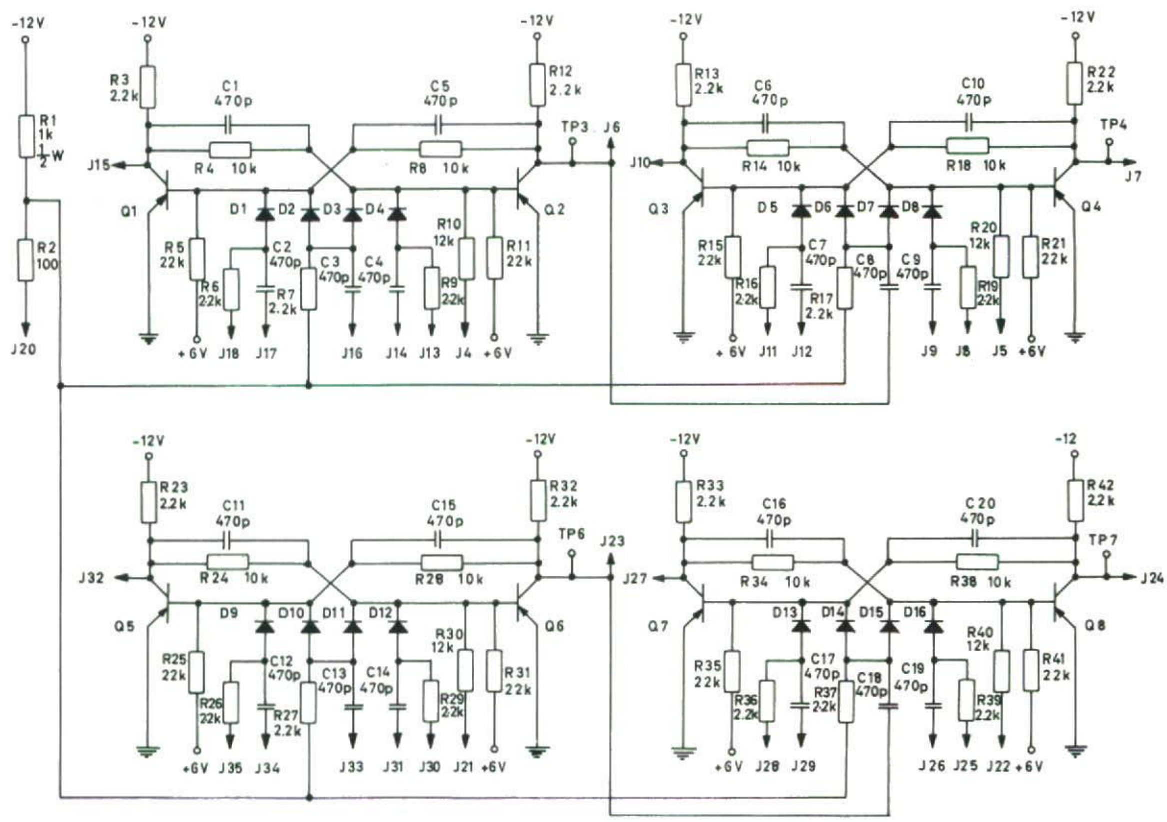
+ 6 V: TP6, J19

All resistors 1/4 W unless otherwise stated

Card type DAF 3/4

Date: 1.1.1964





-12 V: TP1, J2

0 V: TP5, J19

+ 6 V: TP2, J3

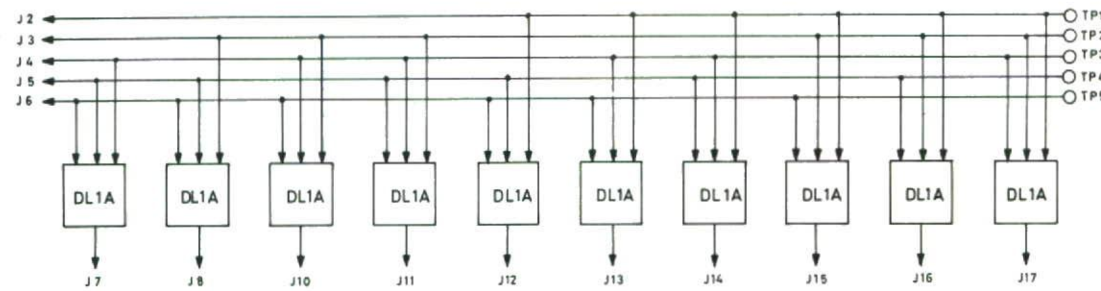
All resistors 1/4 W unless otherwise stated

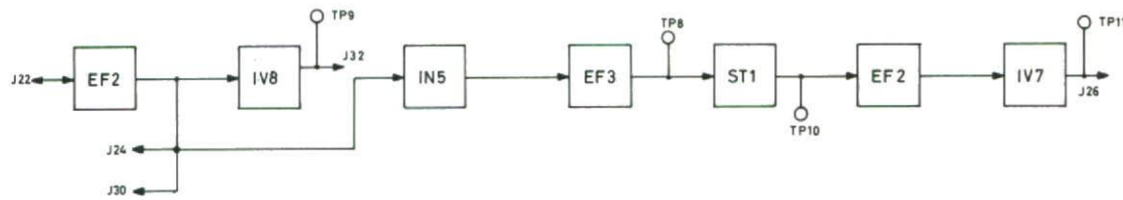
D1 - D16: 0A95

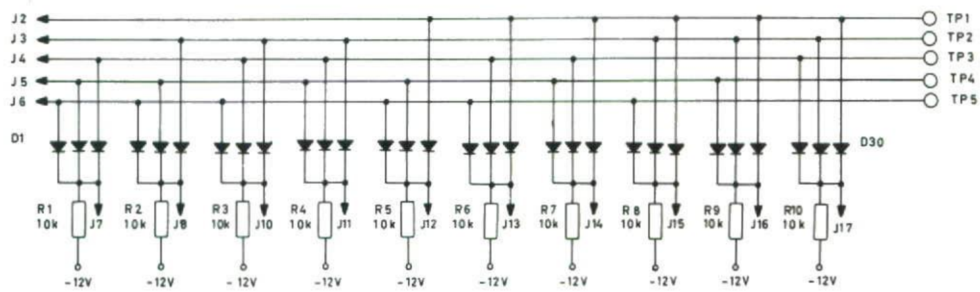
Q1 - Q8 : 2N525

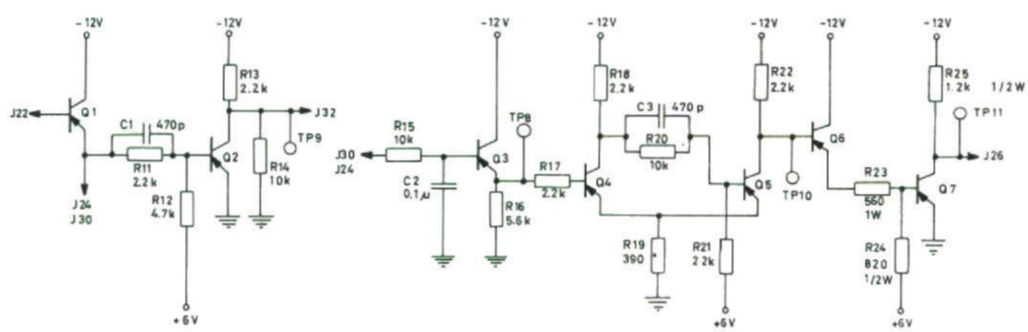
Card type DAF 3/5

Date: 1.1.1964









-12 V: TP6, J18

0 V: TP12, J34

+ 6 V: TP7, J20

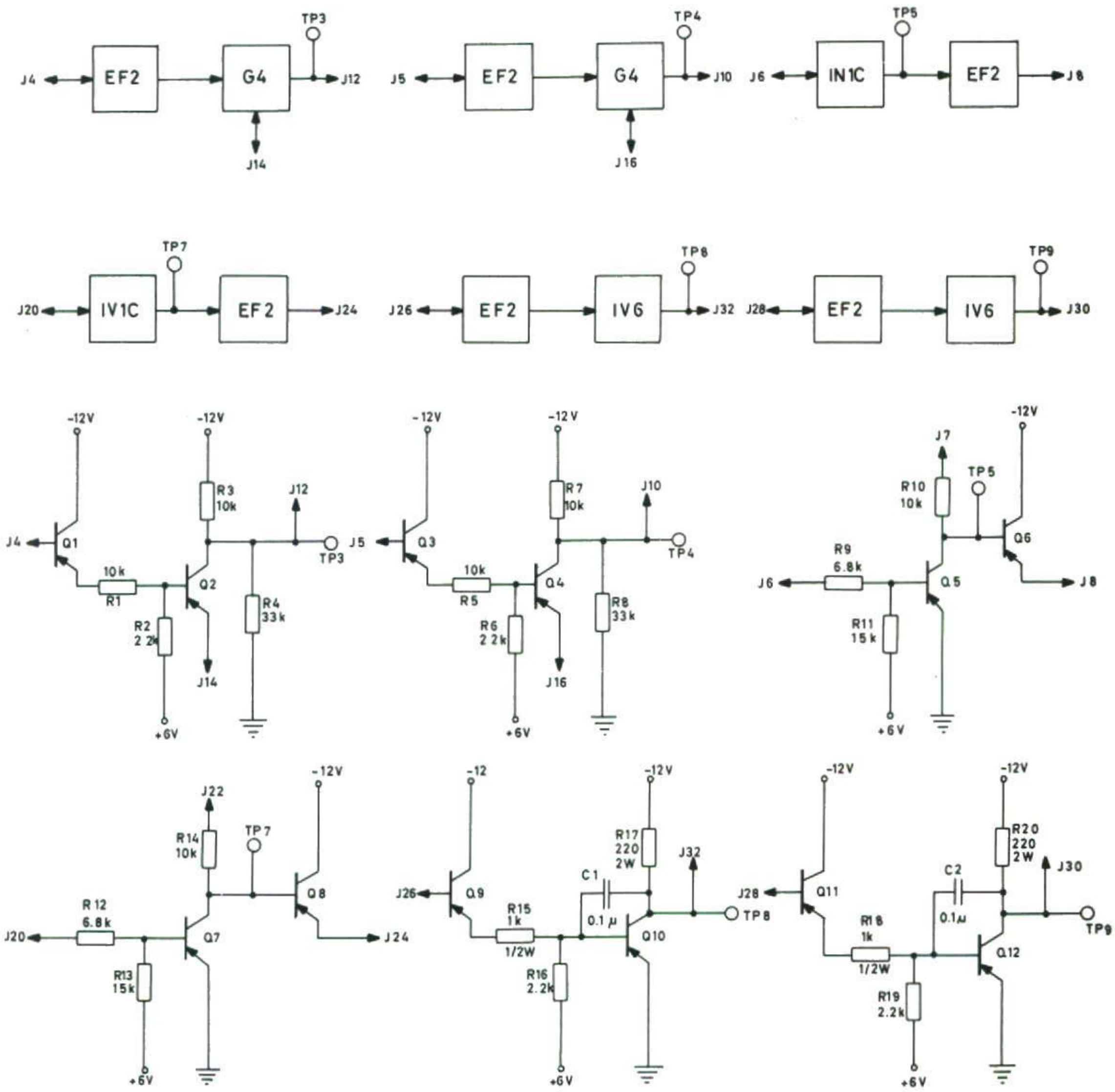
All resistors 1/4 W unless otherwise stated

D1 - D30: 0A95

Q1 - Q7 : 2N525

<u>Card type DAF 3/6</u>

Date: 1.1.1964



-12 V: TP2, J3

0 V: TP6, J18

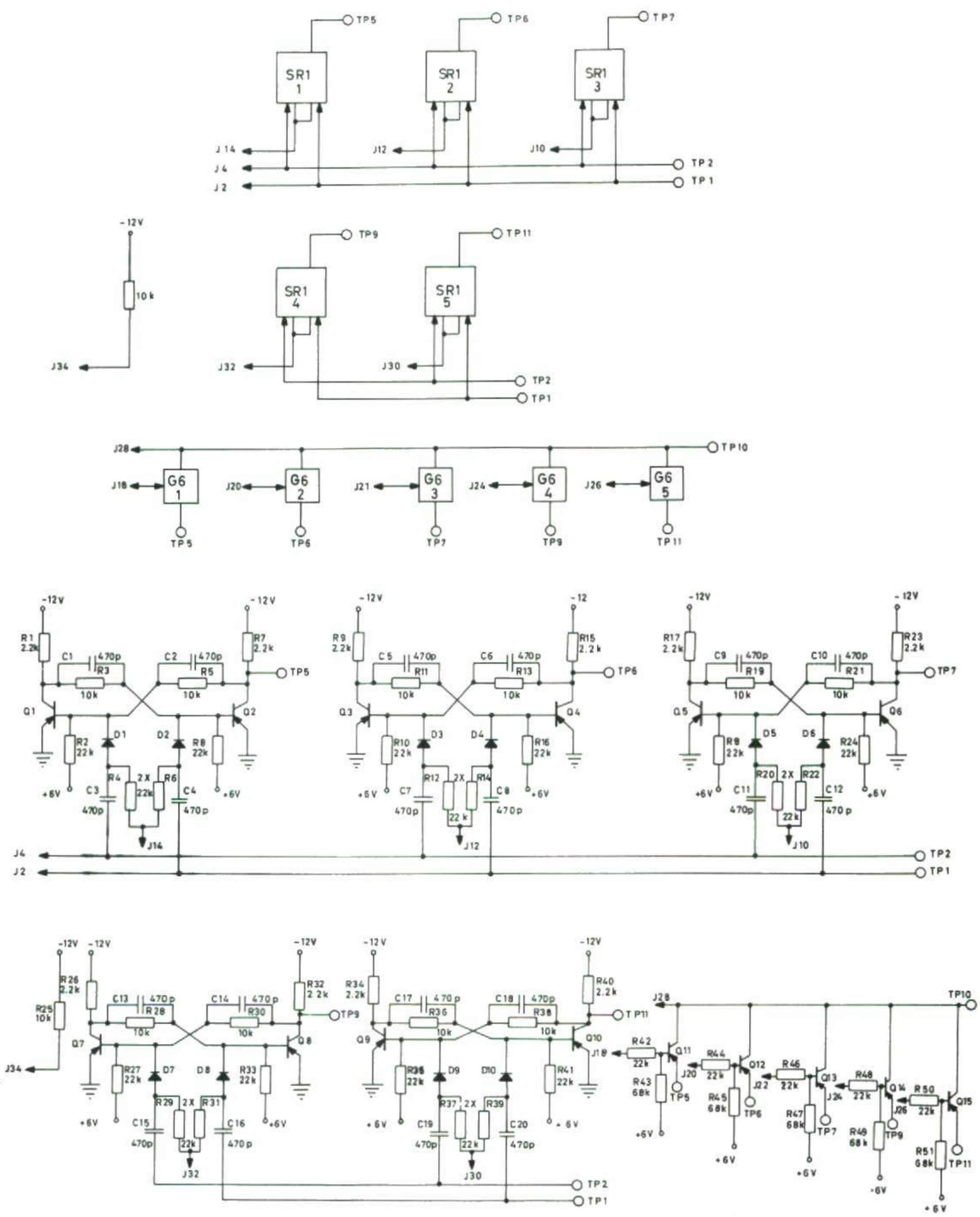
+ 6 V: TP1, J2

All resistors 1/4 W unless otherwise stated

Q1 - Q12: 2N525

<u>Card type DAF 3/7</u>

Date: 1.1.1964



-12 V: TP3, J6

0 V: TP8, J16

+ 6 V: TP4, J8

All resistors 1/4 W unless otherwise stated

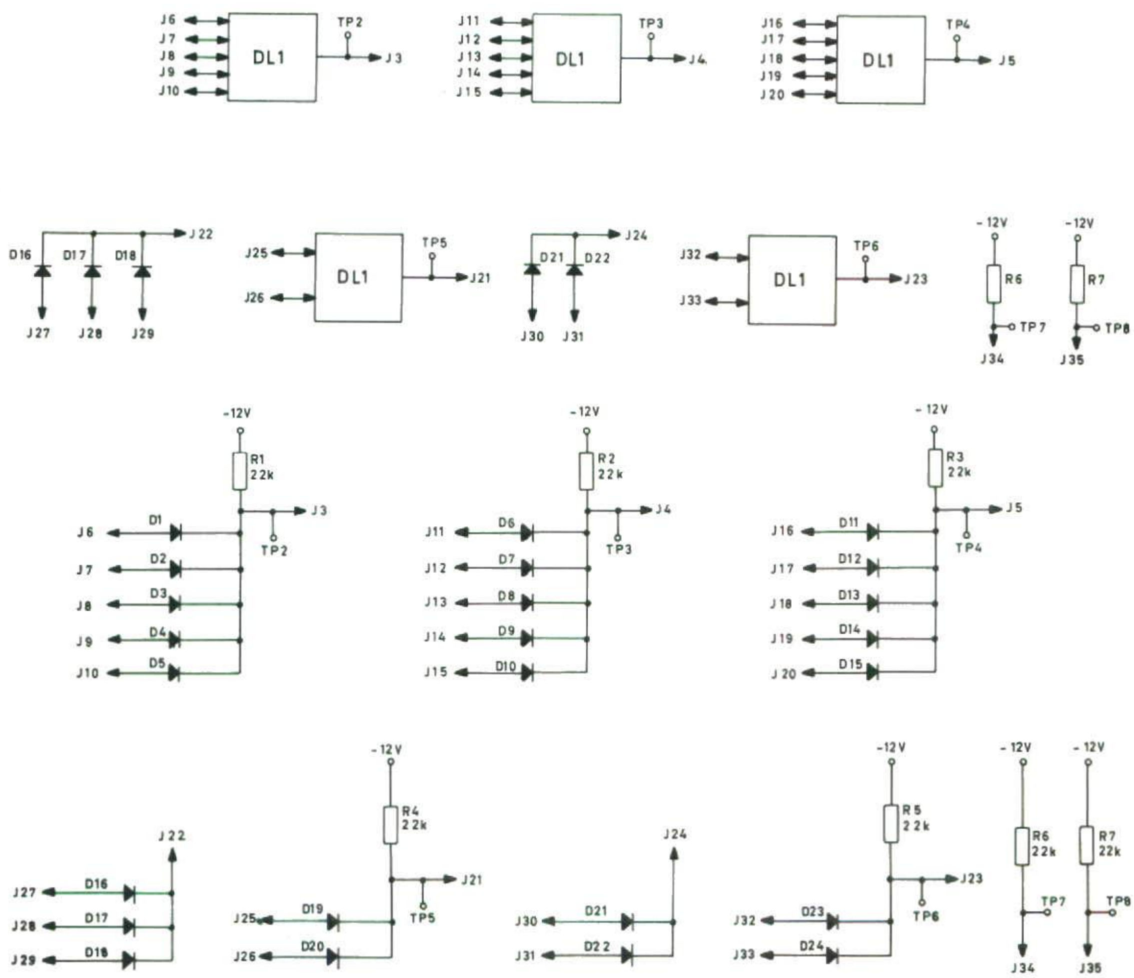
D1 - D10: 0A95

Q1 - Q10: 2N525

Q11- Q15: 2S 302

<u>Card type DAF 3/8</u>

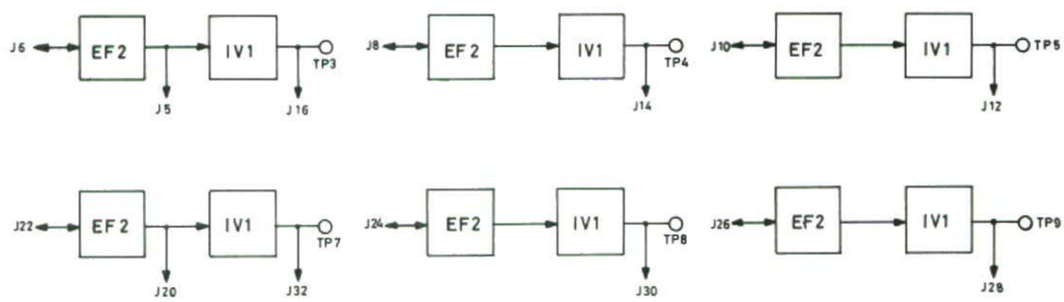
Date: 1.1.1964

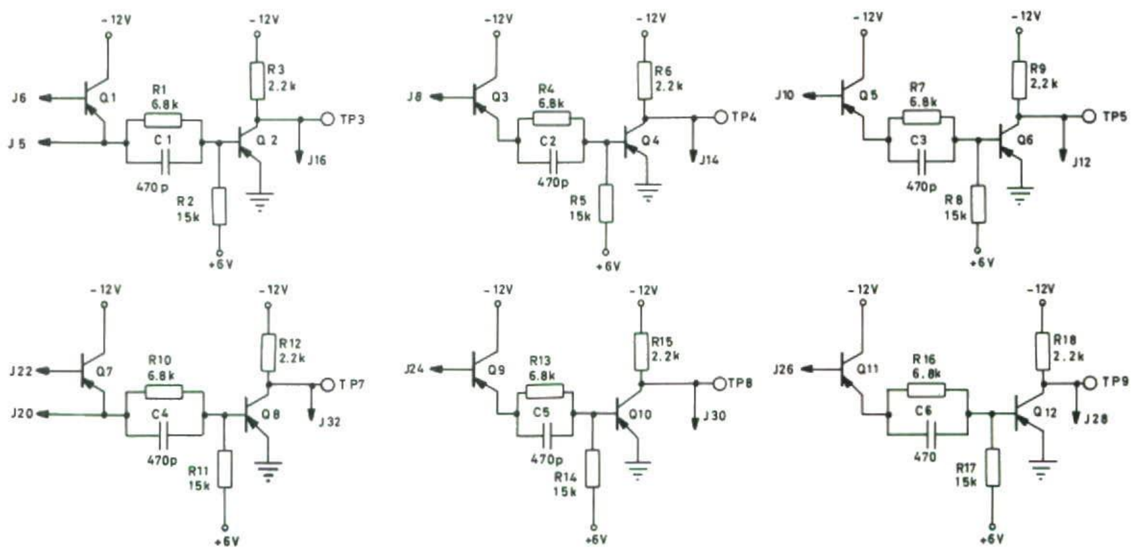


-12 V: TP1, J2 D1 - D24: 0A95

All resistors 1/4 W unless otherwise stated

Card type DAF 3/9 Date: 1.1.1964





-12 V: TP2, J4

0 V: TP6, J18, J34

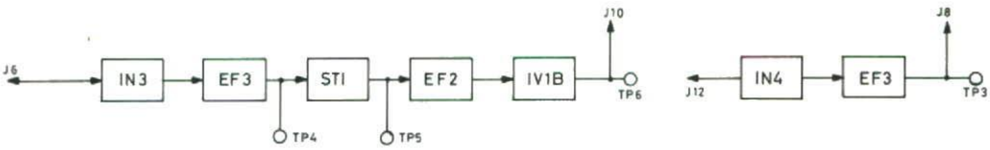
+ 6 V: TP1, J2

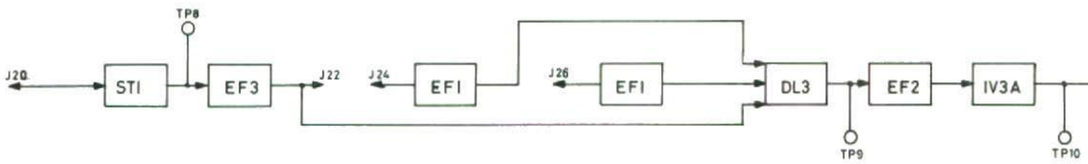
All resistors 1/4 W unless otherwise stated

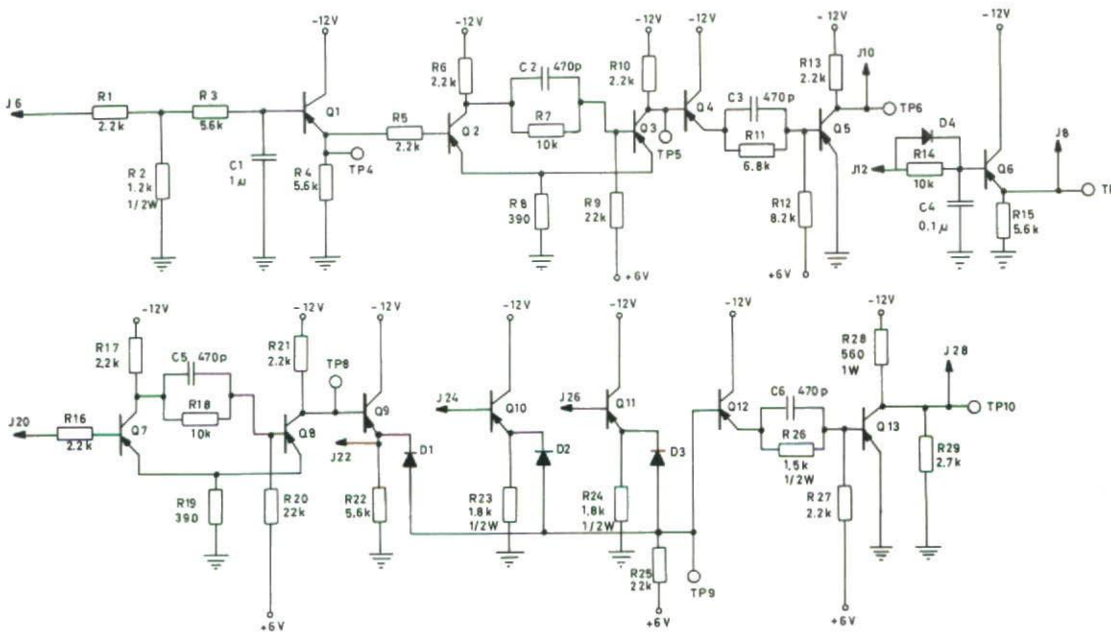
Q1 - Q12: 2N525

<u>Card type DAF 3/10</u>

Date: 1.1.1964







-12 V: TP2, J4

0 V: TP7, J18

+ 6 V: TP1, J2

All resistors 1/4 W unless otherwise stated

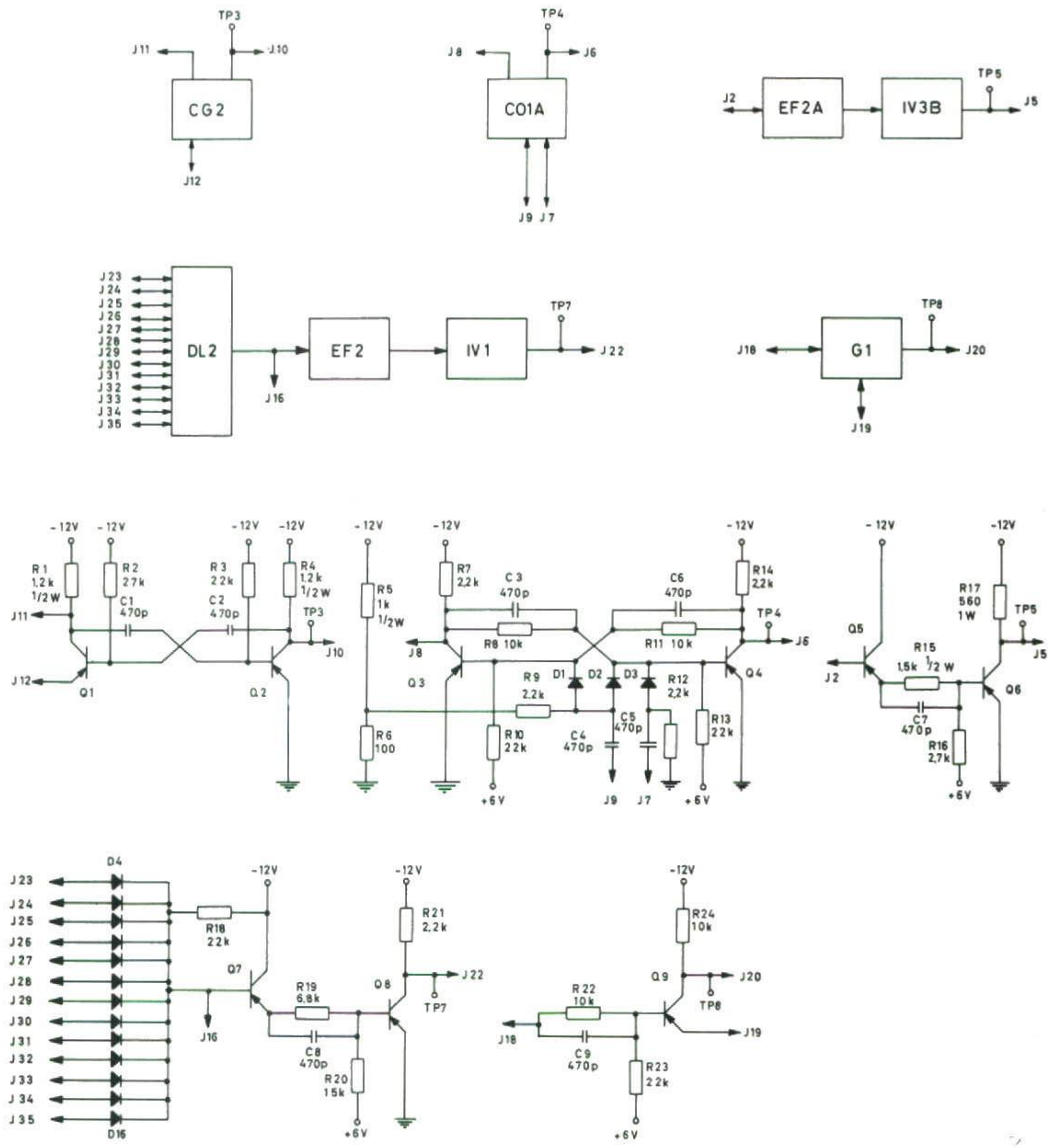
D1 - D3 : 0A202

D4 : 0A95

Q1 - Q13: 2N525

<u>Card type DAF 3/11</u>

Date: 1.1.1964



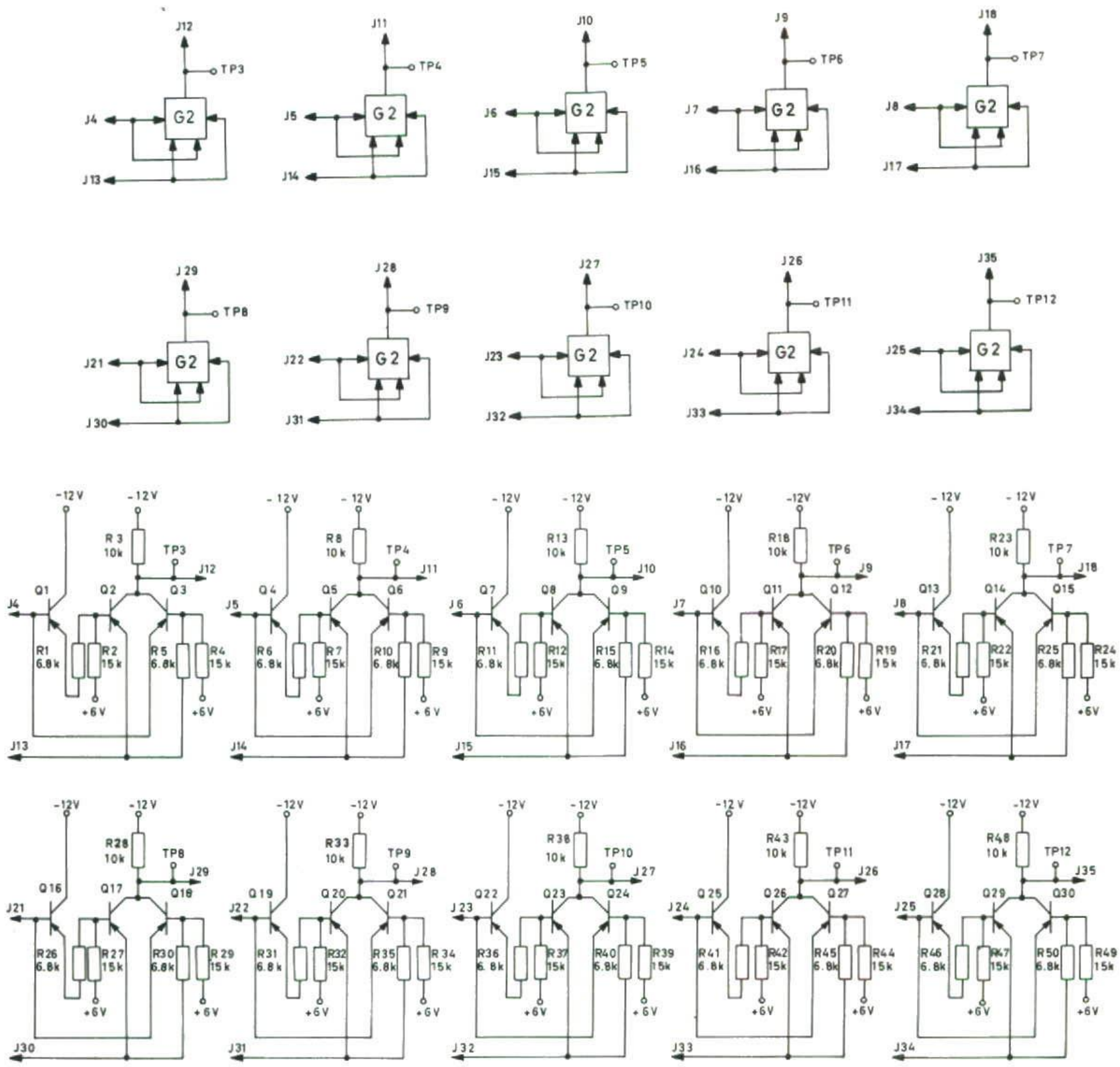
-12 V: TP1, J3
0 V: TP6, J14
+ 6 V: TP2, J4

D1 - D3 : 0A95
D4 - D16: 0A202
Q1 - Q6 : 2N395
Q7 - Q9 : 2N525

All resistors 1/4 W unless otherwise stated

Card type DAF 3/12

Date: 1.1.1964



-12 V: TP2, J3

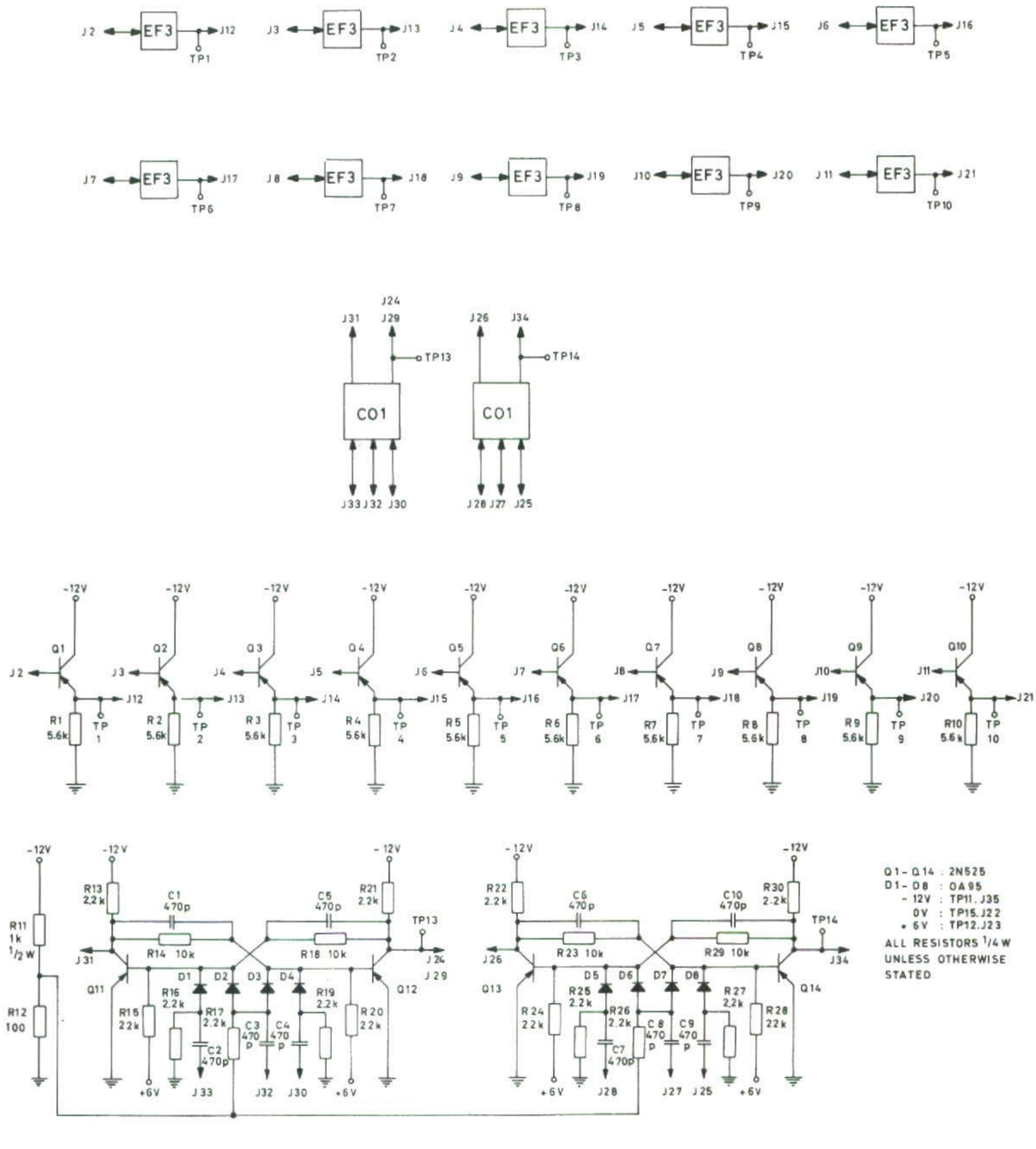
Q1 - Q30: 2N525

+ 6 V: TP1, J2

All resistors 1/4 W unless otherwise stated

Card type DAF 3/13

Date: 1. 1. 1964



-12 V: TP11, J35

0 V: TP15, J22

+ 6 V: TP12, J23

All resistors 1/4 W unless otherwise stated

D1 - D8 : 0A95

Q1 - Q14: 2N525

<u>Card type DAF 3/14</u>

Date: 1.1.1964

Matrix core location		n		255/256 · sin
Col no	Row no	Decimal	Binary	Binary
0	0	0	000 0000	0000 0000
0	1	1	000 0001	0000 0011
0	3	2	000 0010	0000 0110
0	2	3	000 0011	0000 1001
0	7	4	000 0100	0000 1101
0	6	5	000 0101	0001 0000
0	4	6	000 0110	0001 0011
0	5	7	000 0111	0001 0110
0	15	8	000 1000	0001 1001
0	14	9	000 1001	0001 1100
0	12	10	000 1010	0001 1111
0	13	11	000 1011	0010 0010
0	8	12	000 1100	0010 0101
0	9	13	000 1101	0010 1001
0	11	14	000 1110	0010 1100
0	10	15	000 1111	0010 1111
0	X	0-15	000	Ø0ØØ ØØØØ
1	0	16	001 0000	0011 0010
1	1	17	001 0001	0011 0101
1	3	18	001 0010	0011 1000
1	2	19	001 0011	0011 1011
1	7	20	001 0100	0011 1110
1	6	21	001 0101	0100 0001
1	4	22	001 0110	0100 0100
1	5	23	001 0111	0100 0111
1	15	24	001 1000	0100 1010
1	14	25	001 1001	0100 1101
1	12	26	001 1010	0101 0000
1	13	27	001 1011	0101 0011
1	8	28	001 1100	0101 0110
1	9	29	001 1101	0101 1001
1	11	30	001 1110	0101 1100
1	10	31	001 1111	0101 1111
1	X	0-31	00	0ØØØ ØØØØ
2	0	32	010 0000	0110 0010
2	1	33	010 0001	0110 0100
2	3	34	010 0010	0110 0111
2	2	35	010 0011	0110 1010
2	7	36	010 0100	0110 1101
2	6	37	010 0101	0111 0000
2	4	38	010 0110	0111 0011
2	5	39	010 0111	0111 0101
2	15	40	010 1000	0111 1000
2	14	41	010 1001	0111 1011
2	12	42	010 1010	0111 1110
2	13	43	010 1011	1000 0000
2	8	44	010 1100	1000 0011
2	9	45	010 1101	1000 0110
2	11	46	010 1110	1000 1000
2	10	47	010 1111	1000 1011
2	X	32-39	010 0	0ØØØ ØØØØ
3	0	48	011 0000	1000 1110
3	1	49	011 0001	1001 0000
3	3	50	011 0010	1001 0011
3	2	51	011 0011	1001 0101
3	7	52	011 0100	1001 1000
3	6	53	011 0101	1001 1010
3	4	54	011 0110	1001 1101
3	5	55	011 0111	1001 1111
3	15	56	011 1000	1010 0010
3	14	57	011 1001	1010 0100
3	12	58	011 1010	1010 0111
3	13	59	011 1011	1010 1001
3	8	60	011 1100	1010 1011
3	9	61	011 1101	1010 1110
3	11	62	011 1110	1011 0000
3	10	63	011 1111	1011 0010
3	X	48-63	011	Ø0ØØ ØØØØ

Card type DAF 4/5 Ferrite matrix FM1

Binary sine table and core locations

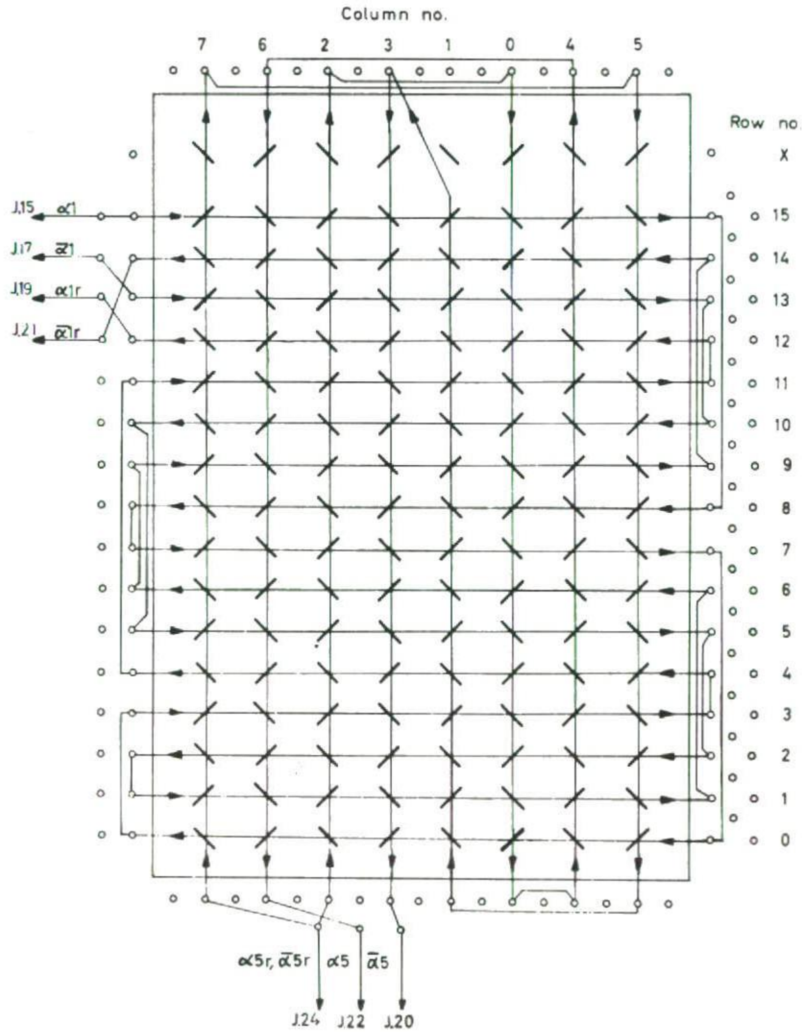
Input angle = $\pi \cdot \frac{n}{256}$ (n = 0 - 63)

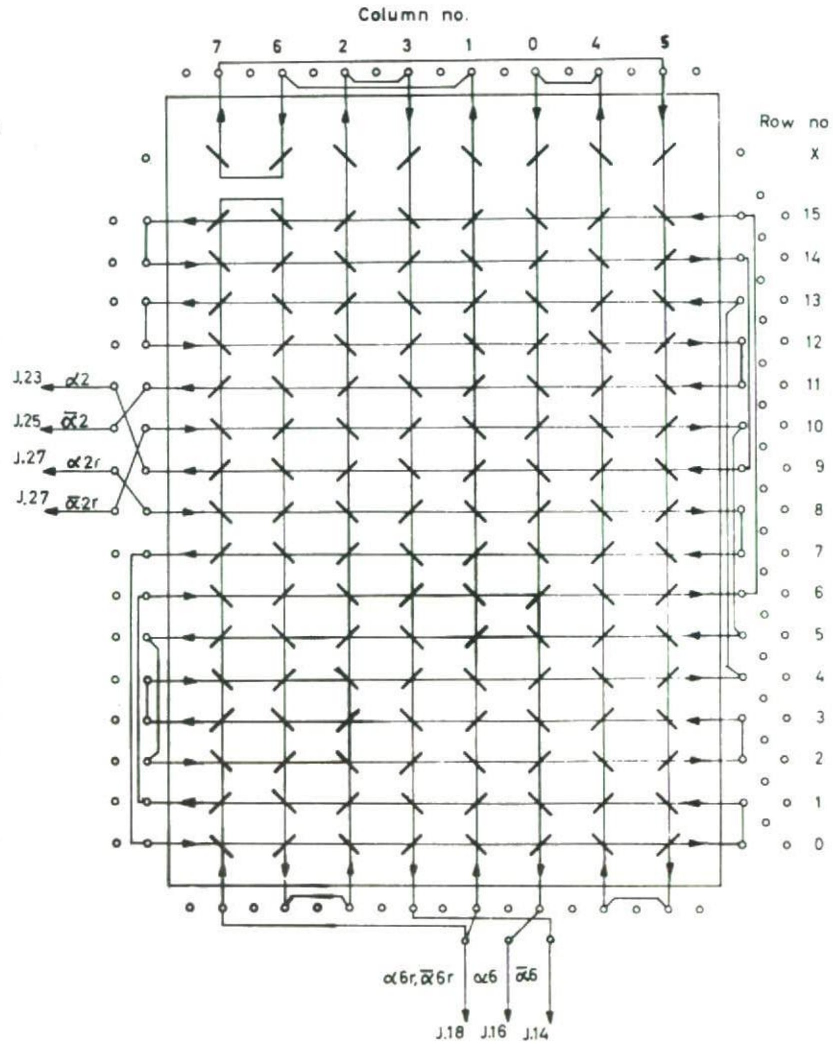
Matrix core location		n		255/256 · sin
Col no	Row no	Decimal	Binary	Binary
4	0	64	100 0000	1011 0100
4	1	65	100 0001	1011 0111
4	3	66	100 0010	1011 1001
4	2	67	100 0011	1011 1011
4	7	68	100 0100	1011 1101
4	6	69	100 0101	1011 1111
4	4	70	100 0110	1100 0001
4	5	71	100 0111	1100 0011
4	15	72	100 1000	1100 0101
4	14	73	100 1001	1100 0111
4	12	74	100 1010	1100 1001
4	13	75	100 1011	1100 1011
4	8	76	100 1100	1100 1101
4	9	77	100 1101	1100 1111
4	11	78	100 1110	1101 0000
4	10	79	100 1111	1101 0010
4	X	72-79	100 1	ØØ0Ø ØØØØ
5	0	80	101 0000	1101 0100
5	1	81	101 0001	1101 0110
5	3	82	101 0010	1101 0111
5	2	83	101 0011	1101 1001
5	7	84	101 0100	1101 1011
5	6	85	101 0101	1101 1100
5	4	86	101 0110	1101 1110
5	5	87	101 0111	1101 1111
5	15	88	101 1000	1110 0001
5	14	89	101 1001	1110 0010
5	12	90	101 1010	1110 0100
5	13	91	101 1011	1110 0101
5	8	92	101 1100	1110 0111
5	9	93	101 1101	1110 1000
5	11	94	101 1110	1110 1001
5	10	95	101 1111	1110 1010
5	X	24-31	001 1	ØØ00 0000
6	0	96	110 0000	1110 1100
6	1	97	110 0001	1110 1101
6	3	98	110 0010	1110 1110
6	2	99	110 0011	1110 1111
6	7	100	110 0100	1111 0000
6	6	101	110 0101	1111 0001
6	4	102	110 0110	1111 0010
6	5	103	110 0111	1111 0011
6	15	104	110 1000	1111 0100
6	14	105	110 1001	1111 0101
6	12	106	110 1010	1111 0110
6	13	107	110 1011	1111 0111
6	8	108	110 1100	1111 0111
6	9	109	110 1101	1111 1000
6	11	110	110 1110	1111 1001
6	10	111	110 1111	1111 1001
6	X	0-7	000 0	0Ø0Ø ØØØ0
7	0	112	111 0000	1111 1010
7	1	113	111 0001	1111 1011
7	3	114	111 0010	1111 1011
7	2	115	111 0011	1111 1100
7	7	116	111 0100	1111 1100
7	6	117	111 0101	1111 1101
7	4	118	111 0110	1111 1101
7	5	119	111 0111	1111 1101
7	15	120	111 1000	1111 1110
7	14	121	111 1001	1111 1110
7	12	122	111 1010	1111 1110
7	13	123	111 1011	1111 1111
7	8	124	111 1100	1111 1111
7	9	125	111 1101	1111 1111
7	11	126	111 1110	1111 1111
7	10	127	111 1111	1111 1111
7	X	80-87	101 0	0000 0000

Card type DAF 4/5 — Ferrite matrix FM1

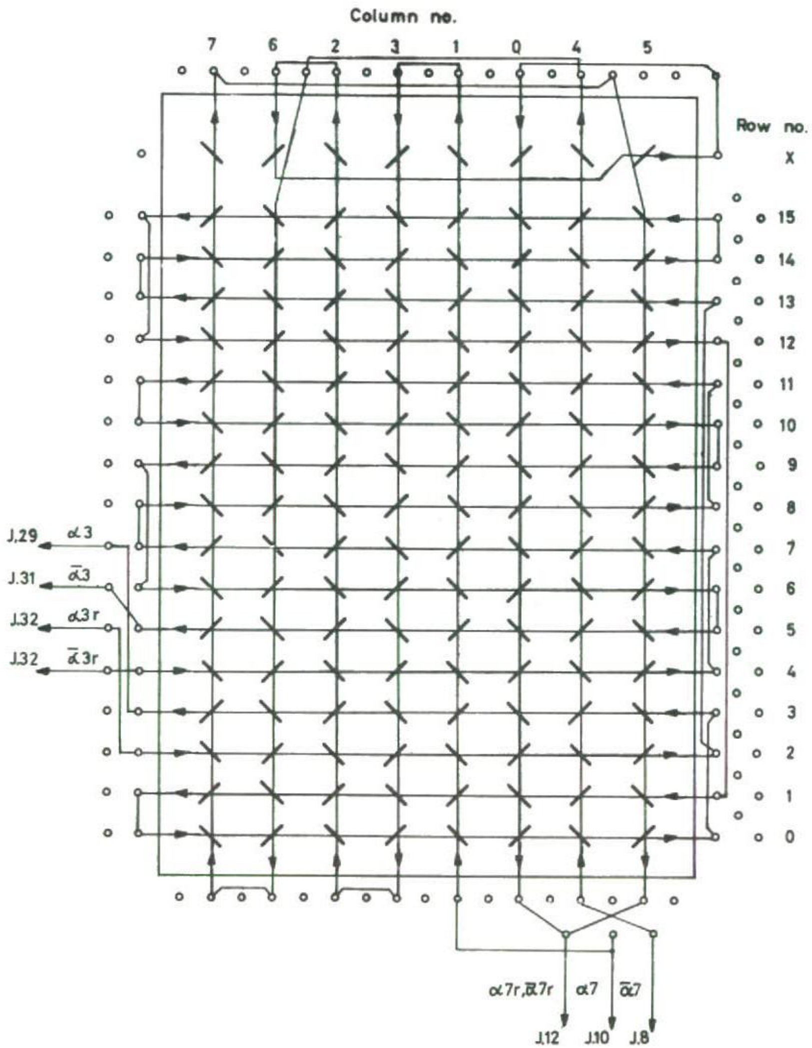
Binary sine table and core locations

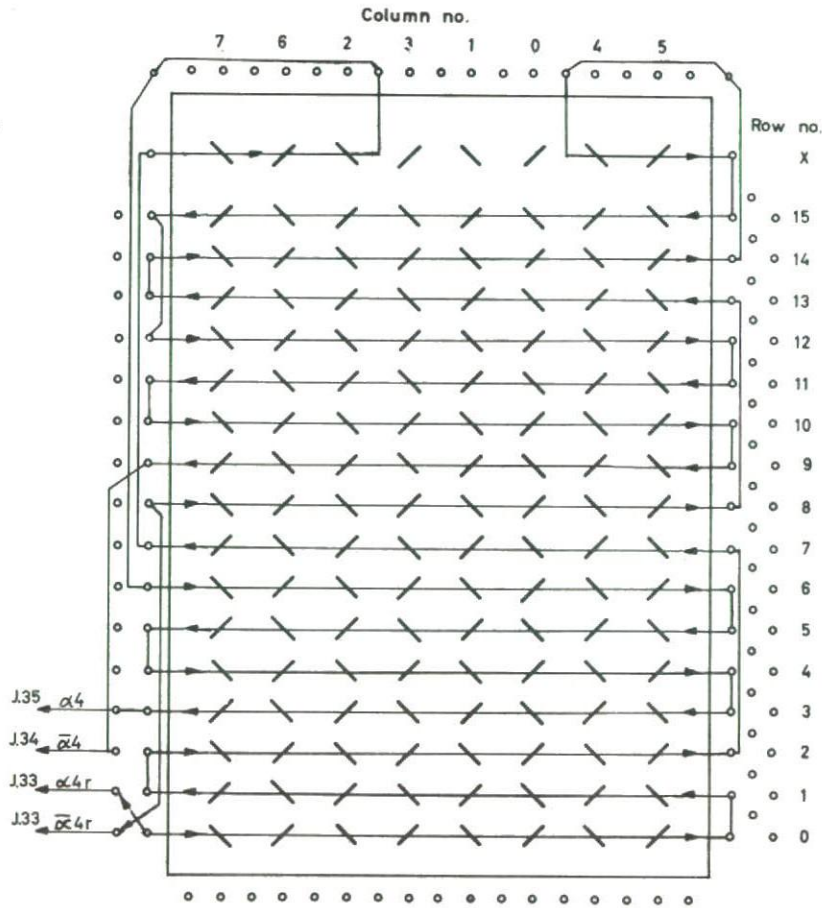
Input angle = $\pi \cdot \frac{n}{256}$ (n = 64 - 127)



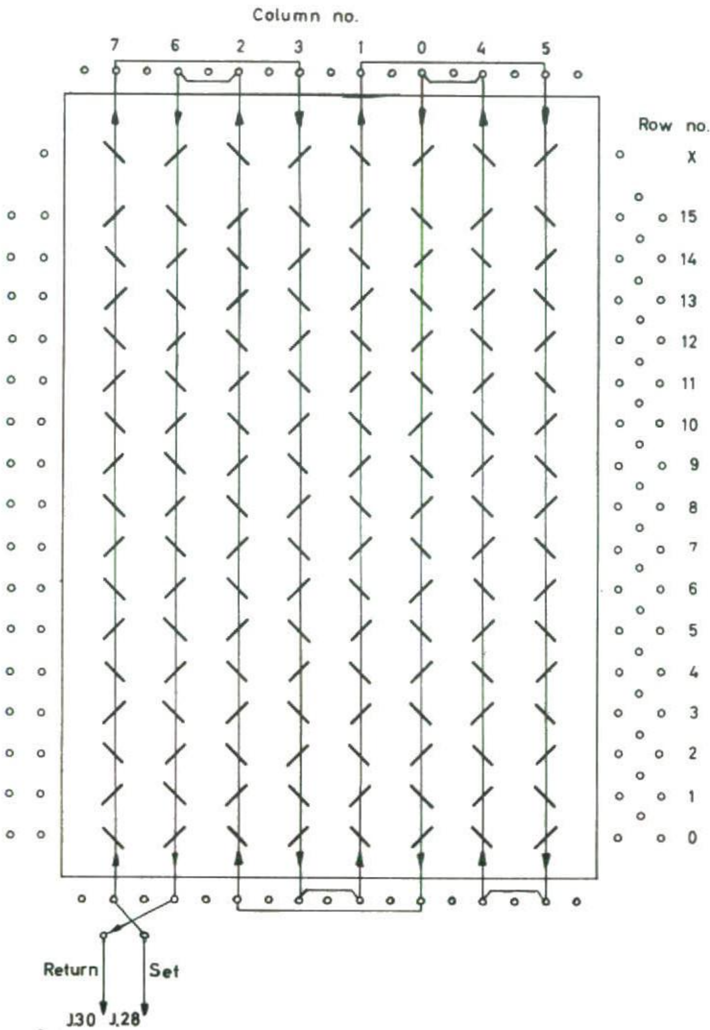


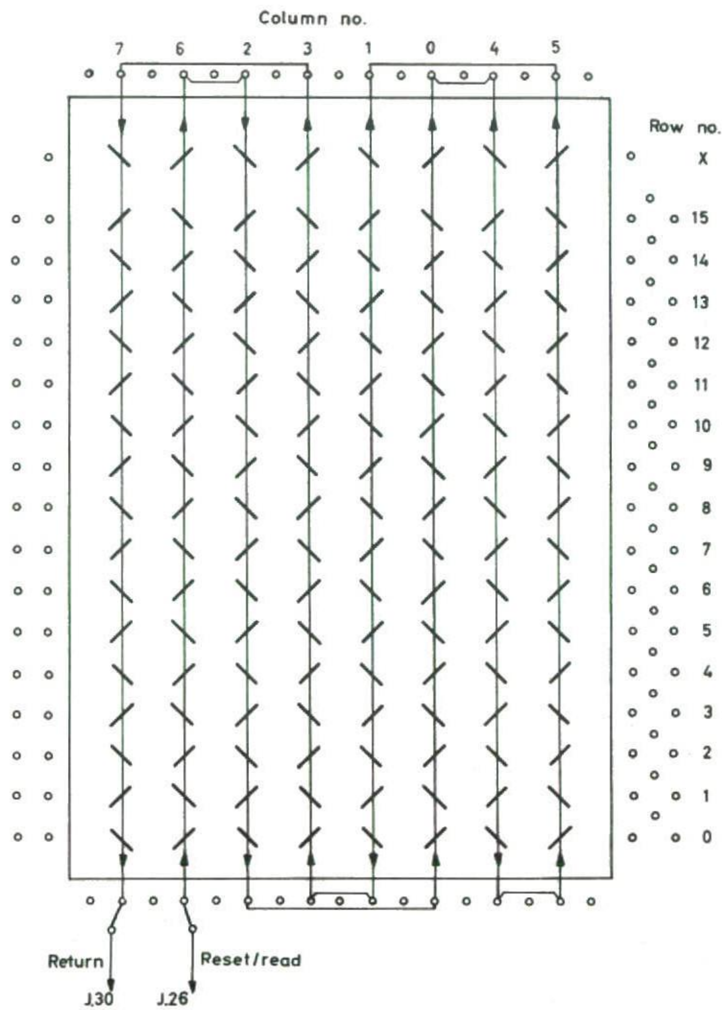
Card type DAF 4/5 Ferrite matrix FM1. Wiring diagram for $\alpha1$, $\bar{\alpha}1$, $\alpha2$, $\bar{\alpha}2$, $\alpha5$, $\bar{\alpha}5$, $\alpha6$ and $\bar{\alpha}6$. Date: 1.1.1964



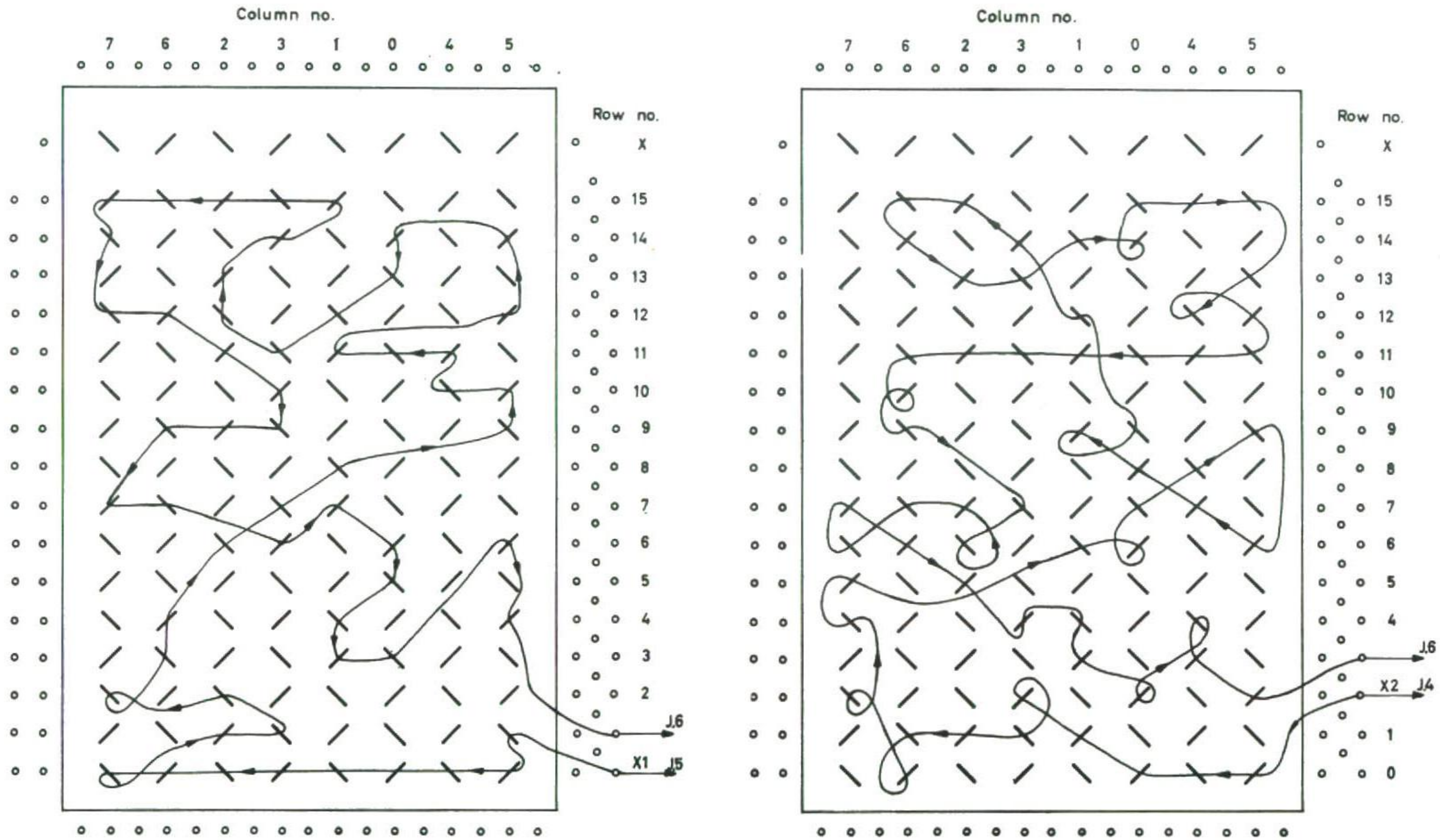


Card type DAF 4/5 Ferrite matrix FM1. Wiring diagram for $\alpha 3$, $\overline{\alpha}3$, $\alpha 4$, $\overline{\alpha}4$, $\alpha 7$ and $\overline{\alpha}7$. Date: 1.1.1964

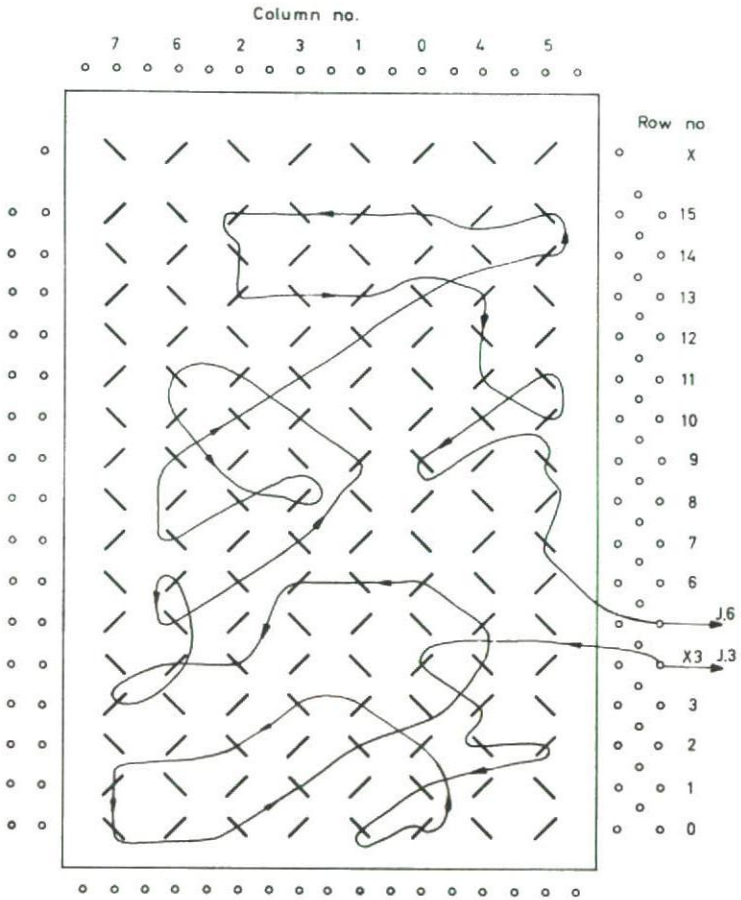


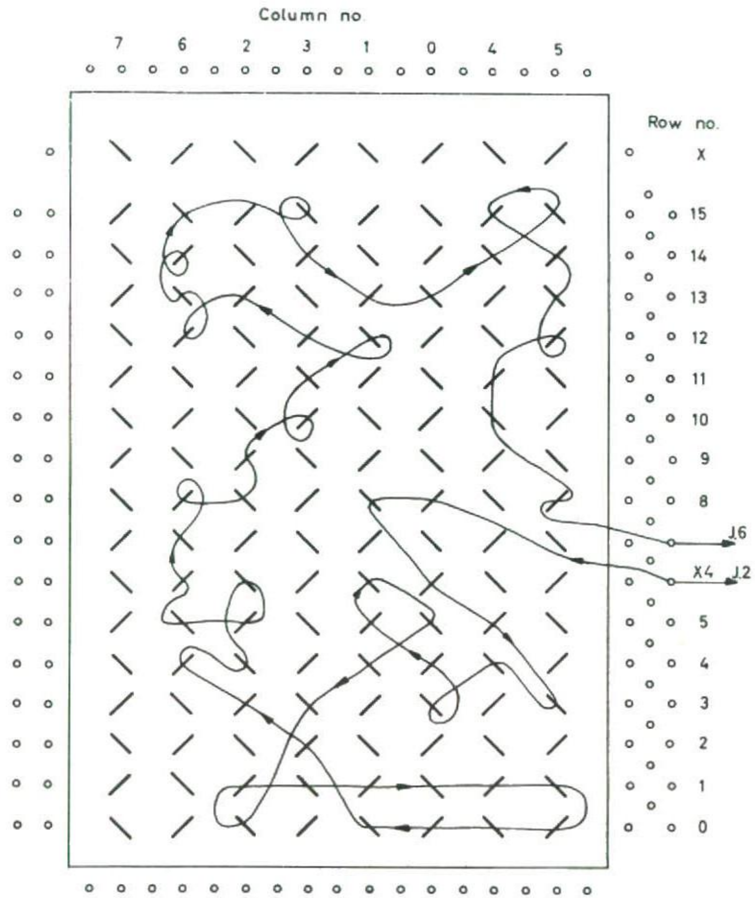


Card type DAF 4/5 Ferrite matrix FM1. Wiring diagram for SET and RESET/READ. Date: 1.1.1964

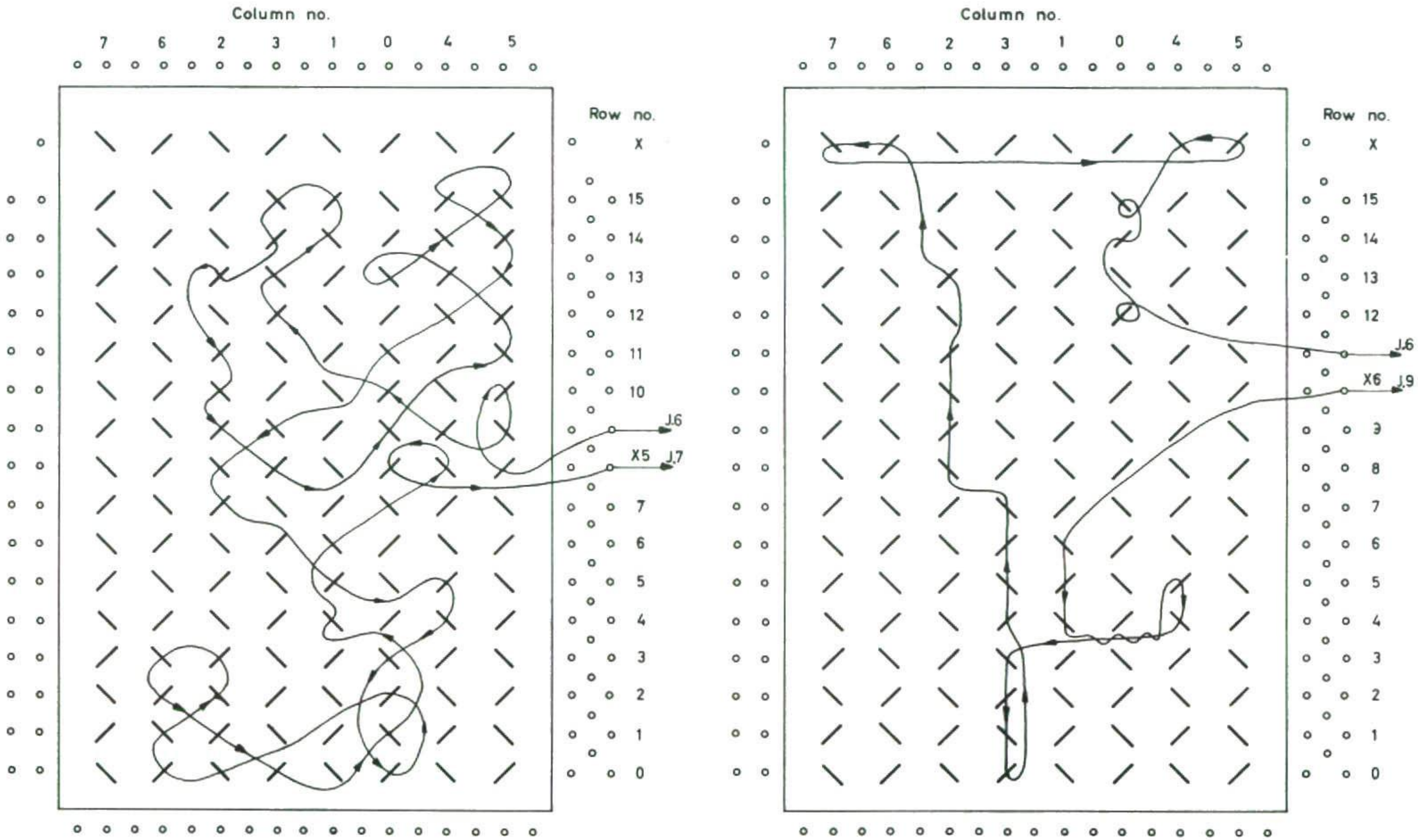


Card type DAF 4/5 Ferrite matrix FM1. Wiring diagram for X1 and X2. Date: 1.1.1964

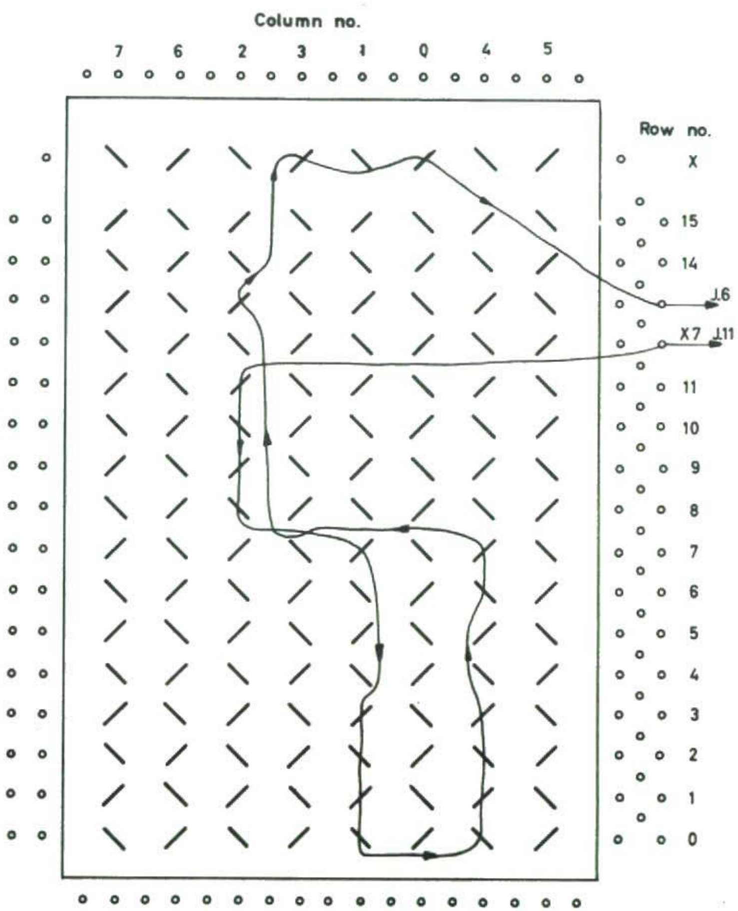


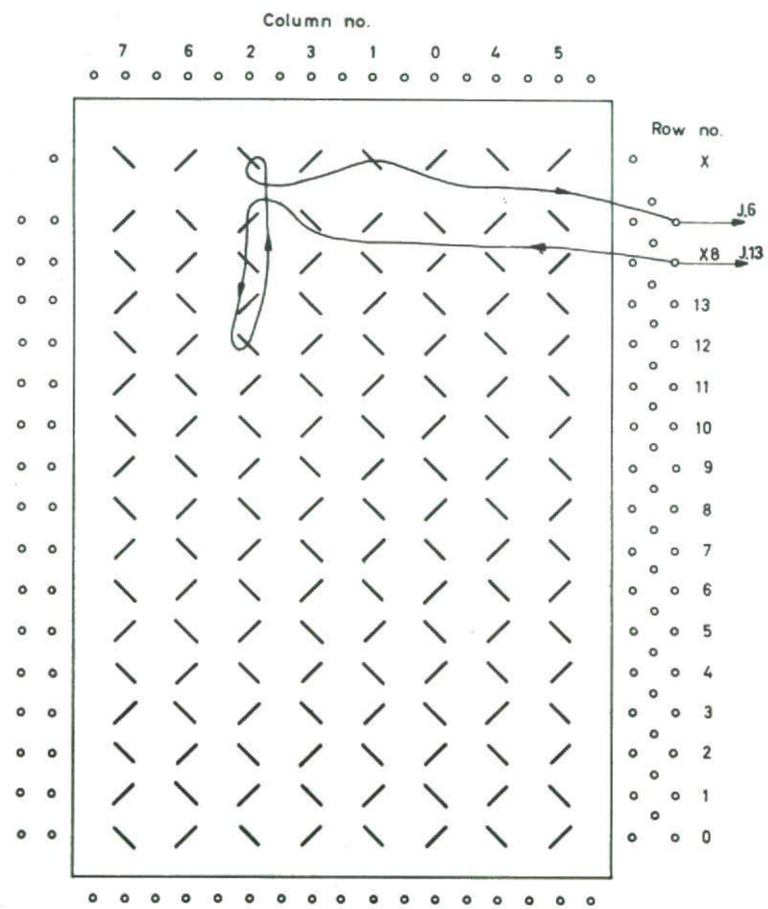


Card type DAF 4/5 Ferrite matrix FM1. Wiring diagram for X3 and X4. Date: 1.1.1964

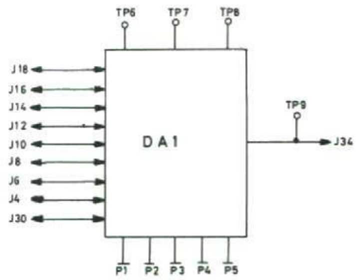


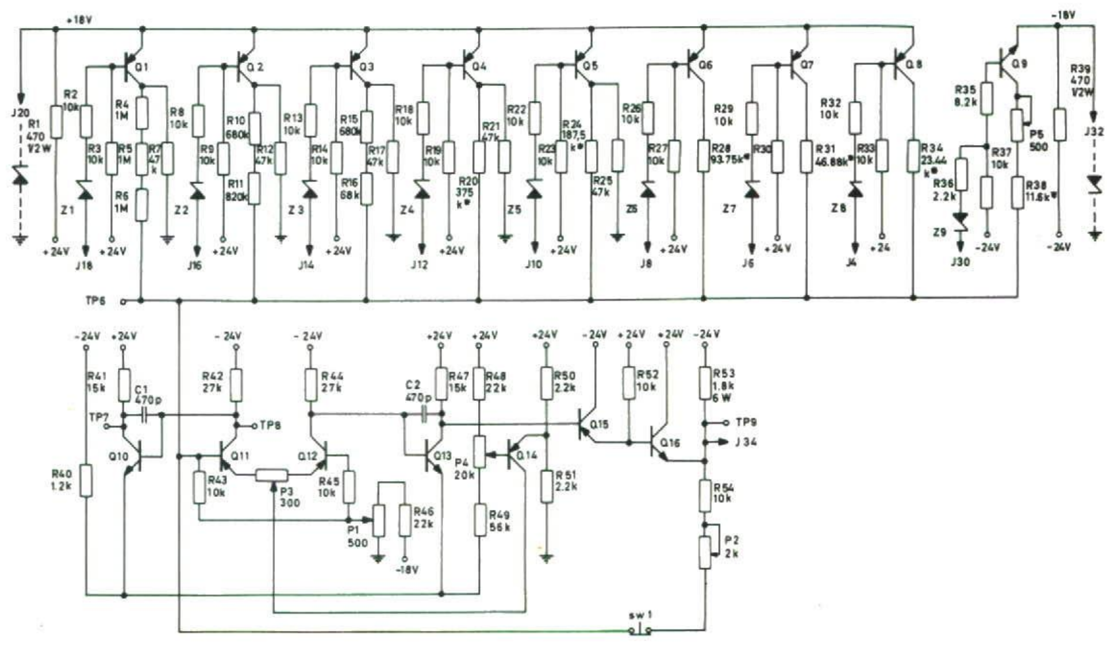
Card type DAF 4/5 Ferrite matrix FM1. Wiring diagram for X5 and X6. Date: 1.1.1964





Card type DAF 4/5 Ferrite matrix FM1. Wiring diagram for X7 and X8. Date: 1.1.1964





-24 V: TP4, J28
-18 V: TP5, J32
0 V: TP3, J22
+18 V: TP2, J20
+24 V: TP1, J2

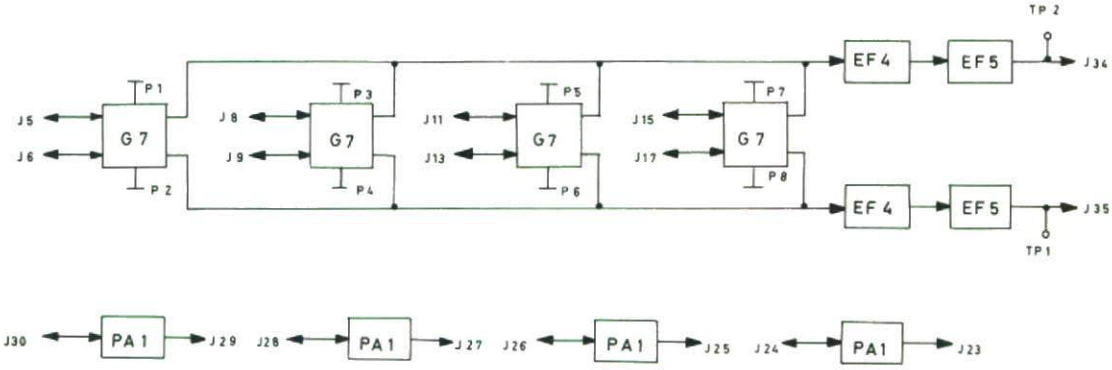
Z1 - Z8 : 115Z4
Z9 : 112Z4
Q1 - Q8, Q14: 2S 303
Q9, Q10, Q13, Q16: 2N1711
Q11, Q12, Q15: 2S 301

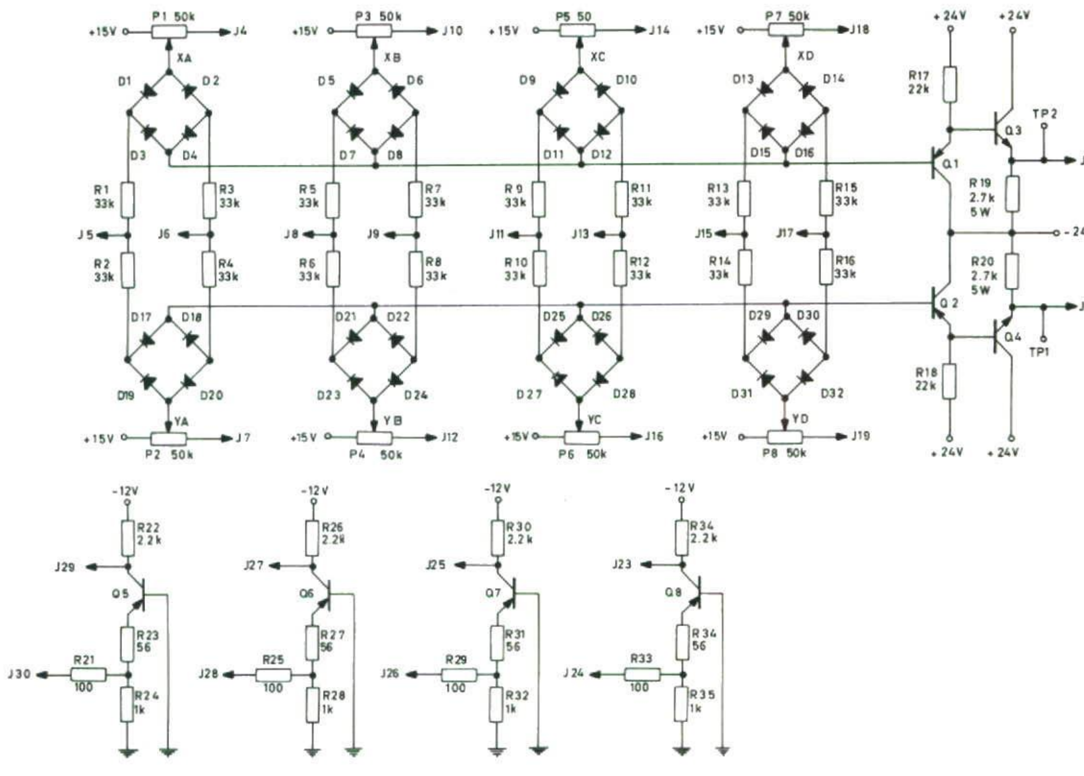
Note*) Special purpose resistors

All resistors 1/4 W unless otherwise stated

<u>Card type DAF 4/6</u>

Date: 1.1.1964



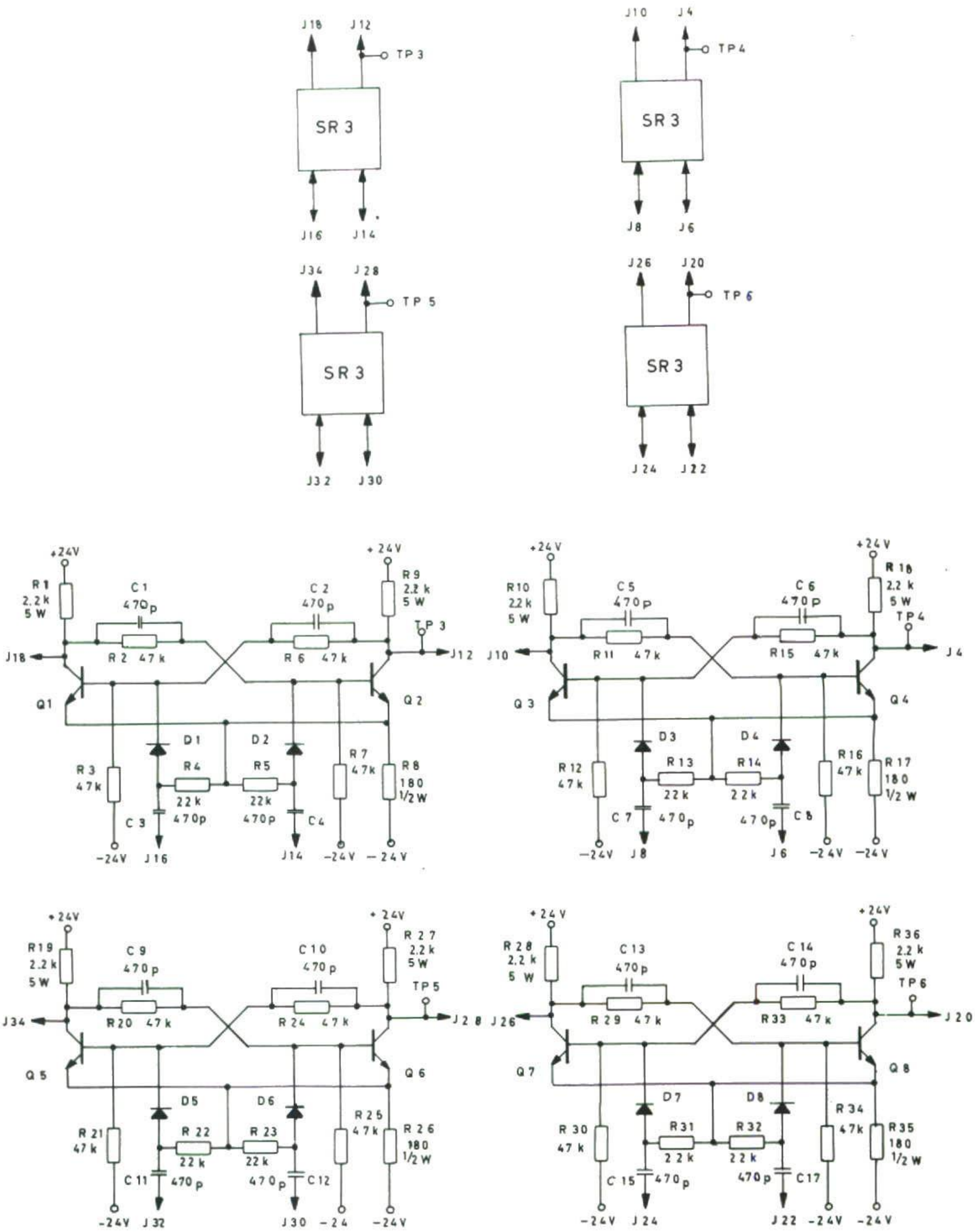


-24 V:	TP5, J32	D1 - D32:	0A202
-12 V:	J21	Q1 - Q2 :	2S 301
0 V:	J31	Q3 - Q4 :	2N1711
+15 V:	TP3, J2	Q5 - Q8 :	2N525
+24 V:	TP4, J33		

All resistors 1/4 W unless otherwise stated

Card type DAF 4/7

Date: 1.1.1964

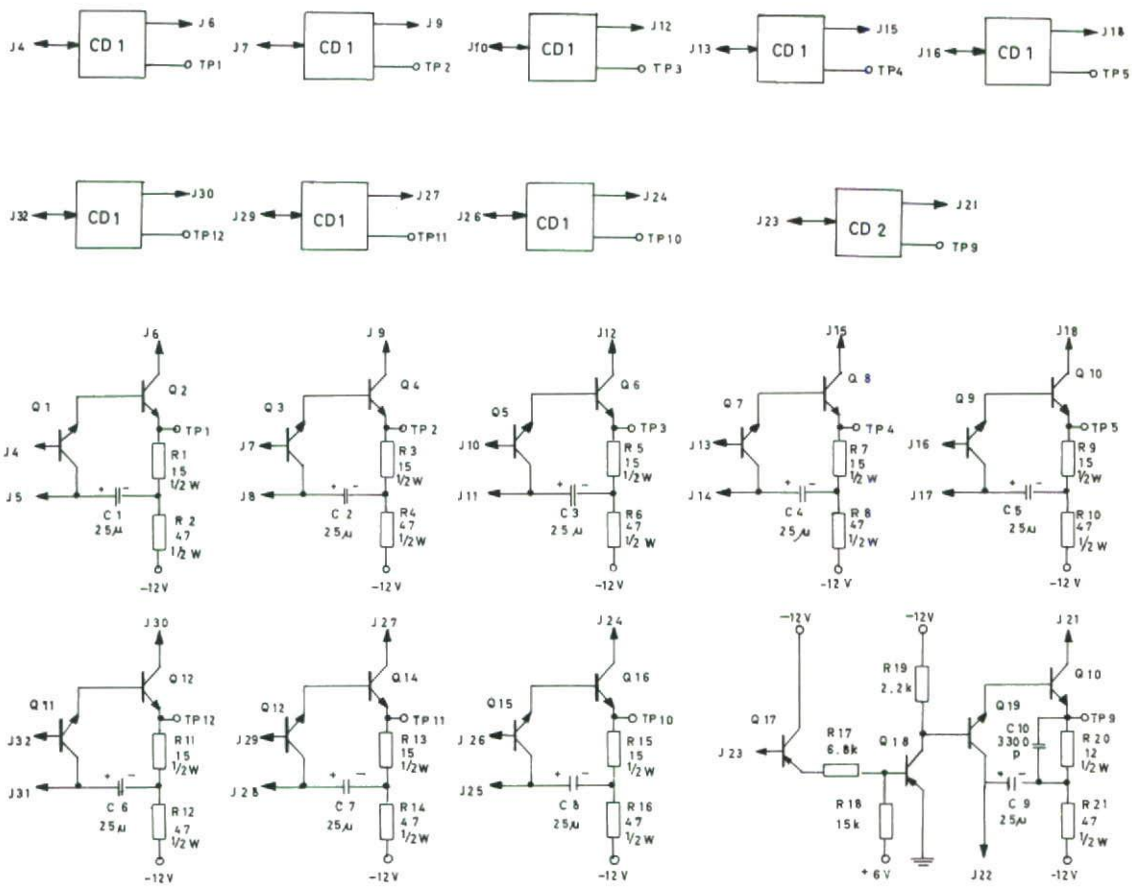


-24 V: TP2, J3	D1 - D8 : 0A95
+24 V: TP1, J2	Q1 - Q8 : 2N1711

All resistors 1/4 W unless otherwise stated

Card type DAF 4/8

Date: 1.1.1964



-12 V: J2, J3

0 V: J33, J34, J35

+ 6 V: J19

Q1, Q3, Q5, Q7, Q9, Q11, Q13, Q15, Q19 : 2N1711

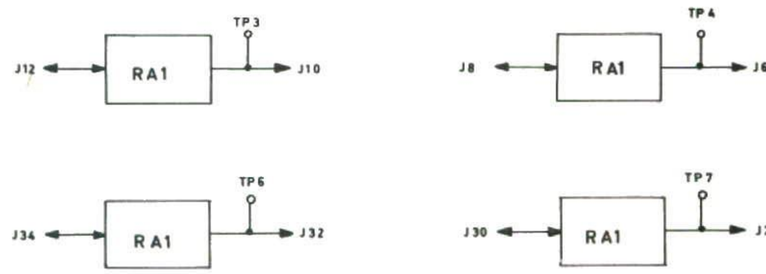
Q2, Q4, Q6, Q8, Q10, Q12, Q14, Q16, Q20 : 2N2195

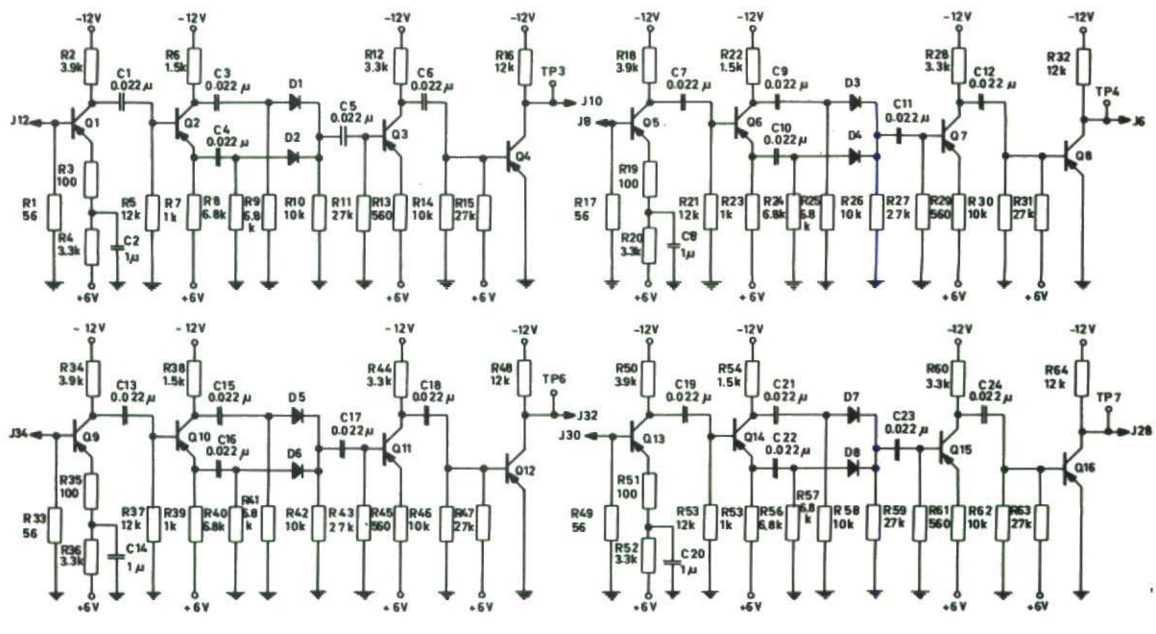
Q17, Q18 : 2N525

All resistors 1/4 W unless otherwise stated

<u>Card type DAF 4/9</u>

Date: 1.1.1964





-12 V: TP1, J2

0 V: TP5, J18

+ 6 V: TP2, J4

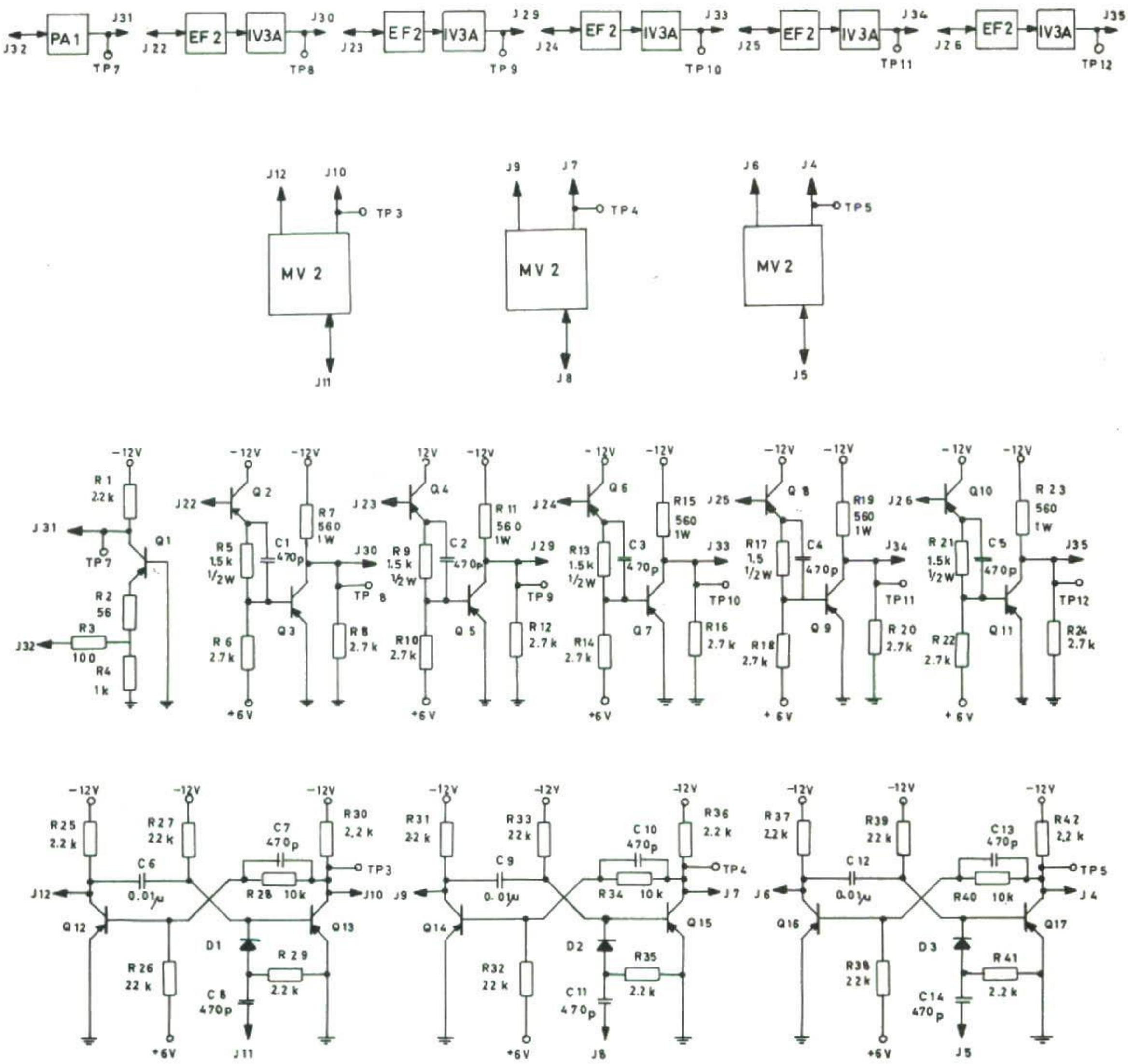
All resistors 1/4 W unless otherwise stated

D1 - D8 : 1N252

Q1 - Q16: 2N395

Card type DAF 4/10

Date: 1.1.1964



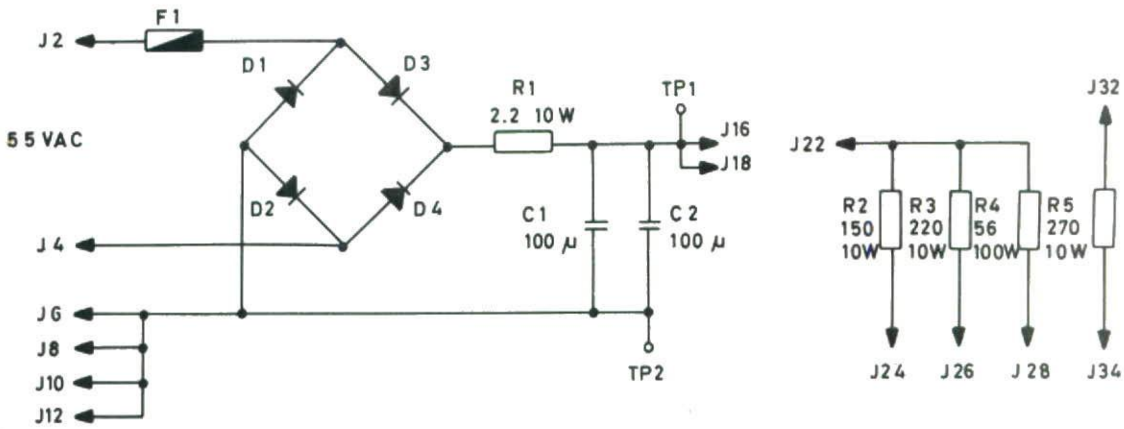
-24 V: TP1, J2 D1 - D3 : 0A95

0 V: TP6, J13 Q1 - Q17: 2N525

\+ 6 V: TP2, J3

All resistors 1/4 W unless otherwise stated

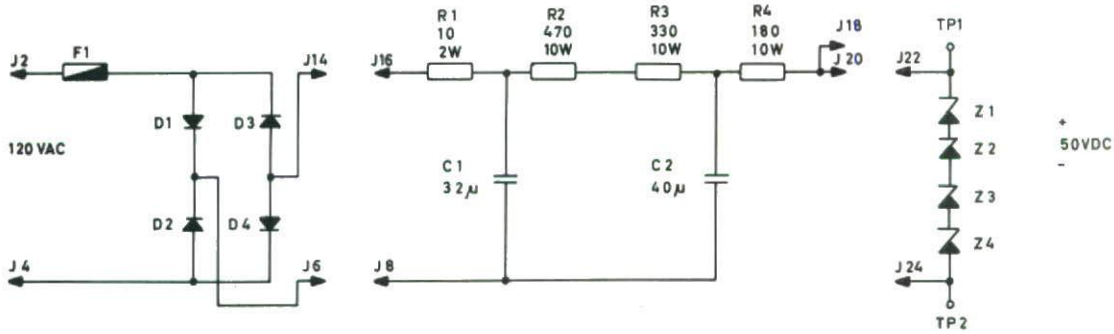
<u>Card type DAF 4/11</u> Date: 1.1.1964



D1 - D4 : 1N1117
F1 : 2A

Card type DAF 11/12

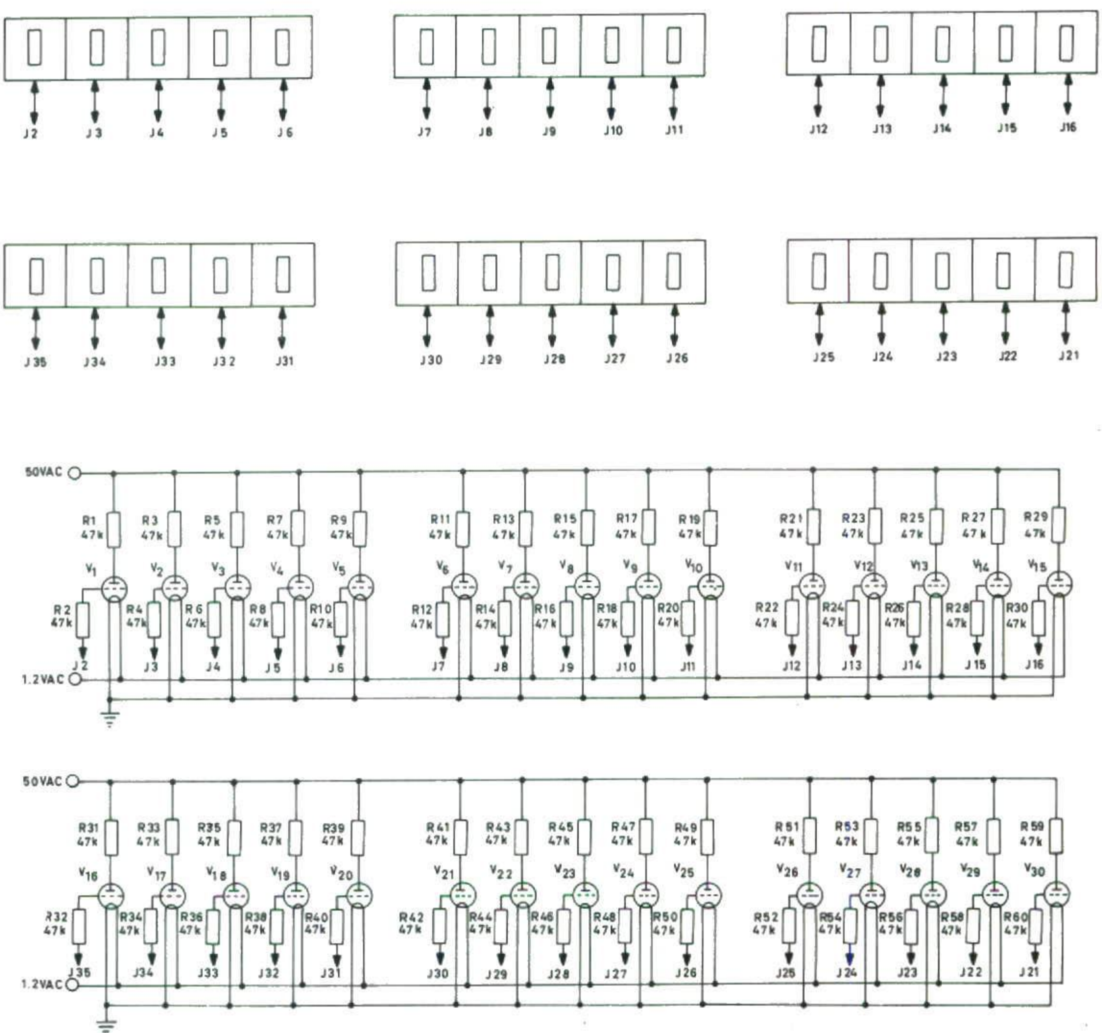
Date: 1.1.1964



D1 - D4 : 1N539
Z1 - Z4 : 212Z4
F1 : 2A

Card type DAF 11/13

Date: 1.1.1964



+50 V : J19

1.2 VAC : J18

0 V : J17, J20

All resistors 1/4 W unless otherwise stated

V1 - V30: DM160

Card type DAF 15/16

Date 1.1.1964

APPENDIX B

STROBE REPORTING STATION SRS-1

CABLING TABLES

From	Colour	Terminal	To	Colour	Note
13.10		TA.01	Fuse 1	we spec.	220 VAC mains
13.10		TA.02	Fuse 2	we spec.	
T1.02	spec.	TA.03	TA.05		
		TA.03	PS1.01	spec.	
		TA.03	SW1.2a	spec.	
T1.04	spec.	TA.04	TA.06		
		TA.04	PS1.02	spec.	
		TA.04	SW1.2b		
VM1.AC1	spec.	TA.05			
VM1.AC2	spec.	TA.06			
PH.06	spec.	TA.07	T1.02	spec.	220 VAC PS5
PH.16	spec.	TA.08	T1.04	spec.	
1309	bn	TA.10	P.04	we/gn	synchro C.S1
1309	gy	TA.12	P.05	we/gn	synchro C.S2
1309	we	TA.14	P.10	we/gn	synchro C.S3
1309	yw	TA.16	P.24	rd/gn	synchro F.S1
1309	bn	TA.18	P.20	rd/gn	synchro F.S2
1309	rd	TA.20	P.02	rd/gn	synchro F.S3
1309	gn	TA.22	J.24	rd/be	115 VAC from
1309	bk	TA.24	J.25	rd/be	Tx synchros
1313	gn	TA.17	PH.07	vt/we	IFF challenge
1313	bn	TA.21	PH.19	vt/we	
1303.8	gy	TA.25	T1.06	rd/be	115 VAC int.
1303.8	be	TA.26			
1303.7	bn	TA.27	T1.07	rd/be	115 VAC int.
1303.7	bk	TA.28			
1303.6	gn	TA.30			
1303.2	oe	TA.31	3.9kohm[1]		Tx relay
1303.4	bk	TA.32			
1305.5	bk	TA.34			
1303.2	be	TA.35	K.35	bk	Tx relay 0 V
1303.1	bn	TA.36	A.31	gn	Rx relay
1303.1	be	TA.37	A.32	gy	Rx relay
1303.3	be	TA.38	A.33	vt/we	Tx relay (Z)
		TA.38	K.20	vt/we	+ 50 V No 1
1303.5	oe	TA.39	A.34	rd/be	Tx relay (A)
		TA.39	3.9kohm[1]		
1303.3	bk	TA.40	A.35	oe	Tx relay (T)
		TA.40	K.31	vt/we	- 50 V No 2

[1] 3.9 kohm connected between TA.31 - TA.39

Table 1.3 SRS terminal board TA connections

From	Colour	Terminal	To	Colour	Note
SW3.17b	rd/be	A.02	15.34	rd/be	
SW3.08b	gy	A.03	16.07	gy	
SW3.12b	rd/be	A.04	18.28	rd/be	
Repeat	vt/we	A.06	16.29	vt/we	Repeat
Wait	rd/be	A.07	16.32	rd/be	Wait
SW3.08a	oe	A.08	19.29	oe	
SW2.26a	we	A.09	21.24	we	
SW2.20a	vt/we	A.10	21.10	vt/we	
SW2.16a	rd/be	A.11	21.06	rd/be	
SW2.18a	oe	A.12	21.08	oe	
SW2.22a	gn	A.13	21.12	gn	
SW2.13a	we	A.14	21.22	we	
SW2.07a	vt/we	A.15	21.18	vt/we	
SW2.03a	rd/be	A.16	21.14	rd/be	
SW2.05a	we	A.17	21.16	we	
SW2.09a	gy	A.18	21.20	gy	
		A.19	22.04	be	- 12 V
C.32	be	A.20	A.19	be	- 12 V
SW4.26b	be	A.20			- 12 V
C.34	rd	A.21	22.14	rd	+ 6 V
C.33	bk	A.22	22.30	bk	0 V
		A.23	22.16	vt/we	
SW3.23a	gn	A.24	21.34	gn	
SW3.26a	gy	A.25	12.22	gy	
SW3.01b	bk	A.26	A.22	bk	
SW3.01a	oe	A.29	22.02	oe	
SW3.10a	rd/be	A.30	22.32	rd/be	
TA.36	gn	A.31	22.24	gn	
TA.37	gy	A.32	22.26	gy	
TA.38	vt/we	A.33	22.10	oe	+ 50 V
TA.39	rd/be	A.34	22.08	rd/be	
TA.40	oe	A.35	22.06	vt/we	- 50 V

Table 2.1 SRS panel AB. Plug A connections
(Plug card type DAF 1/2/10)

From	Colour	Terminal	To	Colour	Note
L.02	gy	B.02	11.18	gy	
L.03	oe	B.03	11.04	oe	
L.04	gn	B.04	10.32	gn	
L.05	gy	B.05	10.20	gy	
L.06	oe	B.06	10.18	oe	
L.07	rd/be	B.07	10.04	rd/be	
L.08	we	B.08	09.32	we	
L.09	gn	B.09	09.20	gn	
L.10	gy	B.10	09.18	gy	
L.11	oe	B.11	09.04	oe	
L.12	we	B.12	08.32	we	
L.13	gn	B.13	08.20	gn	
L.14	oe	B.14	08.18	oe	
L.15	gy	B.15	08.04	gy	
L.16	gn	B.16	11.20	gn	
L.21	gn	B.21	03.31	gn	
L.22	gy	B.22	03.28	gy	
L.23	we	B.23	04.08	we	
L.24	vt/we	B.24	04.22	vt/we	
L.25	rd/be	B.25	04.24	rd/be	
L.26	oe	B.26	03.24	oe	
L.27	we	B.27	05.08	we	
L.28	rd/be	B.28	05.22	rd/be	
L.29	oe	B.29	05.24	oe	
L.30	gy	B.30	05.26	gy	
L.31	gn	B.31	03.18	gn	
L.32	vt/we	B.32	03.17	vt/we	
L.33	oe	B.33	03.16	oe	
L.34	rd/be	B.34	03.15	rd/be	
L.35	gy	B.35	03.33	gy	

Table 2.2 SRS panel AB. Plug B connections
(Plug card type DAF 1/2/11)

From	Colour	Terminal	To	Colour	Note
		01.02	02.02	be	- 12 V
O.16	oe	01.03	06.02	we	
N.11	gy	01.04	07.02	gn	
O.17	gn	01.06	06.04	vt/we	
N.12	we	01.08	07.04	we	
O.20	gn	01.10	06.07	gy	
N.06	gn	01.12			
N.03	rd/be	01.14			
N.02	vt/we	01.16			
		01.18	02.18	bk	0 V
O.13	rd	01.20	02.20	rd	+ 6 V
O.18	vt/we	01.22	06.05	rd/be	
N.13	rd/be	01.24	07.05	vt/we	
O.19	oe	01.26	06.06	oe	
N.14	gy	01.28	07.06	rd/be	
N.15	we	01.30	07.07	oe	

Table 2.3 SRS panel AB. Card No 1 connections
(Card type DAF 3/9)

From	Colour	Terminal	To	Colour	Note
01.02	be	02.02	03.13	be	- 12 V
O.21	gy	02.03	06.08	we	
N.16	gn	02.04	07.08	vt/we	
O.22	we	02.06	06.09	vt/we	
N.17	vt/we	02.08	07.09	rd/be	
O.25	we	02.10	06.12	gy	
N.35	we	02.12			
N.32	oe	02.14			
N.31	rd/be	02.16			
01.18	bk	02.18	03.19	bk	0 V
01.20	rd	02.20	03.35	rd	+ 6 V
O.23	rd/be	02.22	06.10	rd/be	
N.18	oe	02.24	07.10	oe	
O.24	gy	02.26	06.11	oe	
N.19	gn	02.28	07.11	gy	
N.20	vt/we	02.30	07.12	gn	
N.34	gn	02.32			
N.33	gy	02.34			

Table 2.4 SRS panel AB. Card No 2 connections
(Card type DAF 2/11)

From	Colour	Terminal	To	Colour	Note
O.26	gn	03.03			
O.27	we	03.04			
O.28	vt/we	03.05			
O.29	rd/be	03.06			
O.30	oe	03.07			
O.31	gy	03.08			
O.32	gn	03.09			
O.33	we	03.10			
O.34	vt/we	03.11			
O.35	rd/be	03.12			
02.02	be	03.13	04.04	be	- 12 V
		03.14	03.33	oe	A5
B.34	rd/be	03.15	11.15	oe	A4
B.33	oe	03.16	10.24	rd/be	A3
B.32	vt/we	03.17	10.29	gn	A2
B.31	gn	03.18	10.10	vt/we	A1
02.18	bk	03.19	04.20	bk	0 V
		03.20	05.26	vt/we	
		03.20	10.15	rd/be	
		03.21	05.24	we	
		03.21	09.24	vt/we	
		03.22	05.09	gn	
		03.22	09.29	gn	
		03.23	05.08	gy	
B.26	oe	03.24	04.26	oe	
		03.25	04.24	rd/be	
		03.26	04.09	vt/we	
		03.26	08.29	gy	
		03.27	04.08	we	
B.22	gy	03.28	04.06	gy	φ1
PA.0	oe	03.29			bo
B.14	bk	03.30			0 V
PA.c	gn	03.30			
B 21	gn	03.31	08.15	rd/be	X
		03.32	20.21	gy	
B.35	gy	03.33			
		03.34	11.10	we	
02.20	rd	03.35	04.02	rd	+ 6 V

Table 2.5 SRS panel AB. Card No 3 connections
(Card type DAF 2/6)

From	Colour	Terminal	To	Colour	Note
03.35	rd	04.02	05.02	rd	+ 6 V
03.13	be	04.04	05.04	be	- 12 V
03.28	gy	04.06			
03.27	we	04.08			
B.23	we	04.08			
03.26	vt/we	04.09	04.22	gy	
		04.10	08.10	vt/we	
PA.2b	rd/be	04.12			
PA.2a	vt/we	04.14			
PA.1b	we	04.16			
PA.1a	gn	04.18			
03.19	bk	04.20	05.20	bk	0 V
B.24	vt/we	04.22			
B.25	rd/be	04.24			
03.25	rd/be	04.24			
03.24	oe	04.26	09.15	oe	
		04.28	08.24	rd/be	
PA.4b	we	04.30			
PA.4a	gn	04.32			
PA.3b	gy	04.34			
PA.3a	oe	04.35			

Table 2.6 SRS panel AB. Card No 4 connections
(Card type 2/8)

From	Colour	Terminal	To	Colour	Note
04.02	rd	05.02	06.15	rd	+ 6 V
04.04	be	05.04	06.16	be	- 12 V
B.27	we	05.08			
03.23	gy	05.08			
03.22	gn	05.09	05.22	vt/we	
		05.10	09.10	oe	
PA.6b	vt/we	05.12			
PA.6a	we	05.14			
PA.5b	gn	05.16			
PA.5a	gy	05.18			
04.20	bk	05.20	06.14	bk	0 V
B.28	rd/be	05.22			
B.29	oe	05.24			
03.21	we	05.24			
B.30	gy	05.26			
03.20	vt/we	05.26			
PA.8b	gn	05.30			
PA.8a	gy	05.32			
PA.7b	oe	05.34			
PA.7a	rd/be	05.35			

Table 2.7 SRS panel AB. Card No 5 connections (Card type DAF 2/8)

From	Colour	Terminal	To	Colour	Note
01.03	we	06.02			
01.06	vt/we	06.04			
01.22	rd/be	06.05			
01.26	oe	06.06			
01.10	gy	06.07			
02.03	we	06.08			
02.06	vt/we	06.09			
02.22	rd/be	06.10			
02.26	oe	06.11			
02.10	gy	06.12			
05.20	bk	06.14	07.14	bk	0 V
05.02	rd	06.15	07.15	rd	+ 6 V
05.04	be	06.16	07.16	be	- 12 V
		06.20	15.03	we	
		06.22	15.13	gn	
		06.24	06.18	rd/be	
		06.34	15.07	vt/we	

Table 2.8 SRS panel AB. Card No 6 connections (Card type DAF 2/9)

From	Colour	Terminal	To	Colour	Note
01.04	gn	07.02			
01.08	we	07.04			
01.24	vt/we	07.05			
01.28	rd/be	07.06			
01.30	oe	07.07			
02.04	vt/we	07.08			
02.08	rd/be	07.09			
02.24	oe	07.10			
02.28	gy	07.11			
02.30	gn	07.12			
06.14	bk	07.14	08.19	bk	0 V
06.15	rd	07.15	08.06	rd	+ 6 V
06.16	be	07.16	08.05	be	- 12 V
		07.20	15.02	gy	
		07.22	15.08	oe	
		07.24	07.18	we	
		07.34	15.04	gn	

Table 2.9 SRS panel AB. Card No 7 connections
(Card type DAF 2/9)

From	Colour	Terminal	To	Colour	Note
O.15	rd/be	08.02			
B.15	gy	08.04			
07.16	be	08.05	09.05	be	- 12 V
07.15	rd	08.06	09.06	rd	+ 6 V
		08.08	08.31	oe	
		08.09	14.28	we	Set INFO
04.10	vt/we	08.10			
		08.11	08.27	gy	
		08.13	08.02	be	
		08.14	08.09	rd/be	
		08.14	08.23	gy	
03.31	rd/be	08.15			
		08.17	08.33	rd/be	
B.14	oe	08.18			
07.14	bk	08.19	09.19	bk	0 V
B.13	gn	08.20			
		08.22	09.17	we	
		08.23	08.28	gn	
04.28	rd/be	08.24			
		08.25	09.13	vt/we	
		08.28	09.28	we	
03.26	gy	08.29			
B.12	we	08.32			

Table 2.10 SRS panel AB. Card No 8 connections
(Card type DAF 2/13)

From	Colour	Terminal	To	Colour	Note
		09.03	10.03	gn	Shift signal
B.11	oe	09.04			
08.05	be	09.05	10.05	be	- 12 V
08.06	rd	09.06	10.06	rd	+ 6 V
		09.08	09.31	gn	
		09.09	10.14	gy	
05.10	oe	09.10			
		09.11	09.27	we	
08.25	vt/we	09.13			
		09.14	09.09	oe	
04.26	oe	09.15			
08.22	we	09.17			
B.10	gy	09.18			
08.19	bk	09.19	10.19	bk	0 V
B.09	gn	09.20			
		09.22	10.17	vt/we	
		09.23	09.14	rd/be	
03.21	vt/we	09.24			
		09.25	10.13	rd/be	
08.28	we	09.28	09.23	vt/we	
03.22	gn	09.29			
B.08	we	09.32			

Table 2.11 SRS panel AB. Card No 9 connections (Card type DAF 2/13)

From	Colour	Terminal	To	Colour	Note
09.03	gn	10.03	11.03	gn	Shift signal
B.07	rd/be	10.04			
09.05	be	10.05	11.05	be	- 12 V
09.06	rd	10.06	11.06	rd	+ 6 V
		10.08	10.31	gy	
03.18	vt/we	10.10			
		10.11	10.27	gn	
09.25	rd/be	10.13			
09.09	gy	10.14			
03.20	rd/be	10.15			
09.22	vt/we	10.17			
B.06	oe	10.18			
09.19	bk	10.19	11.19	bk	0 V
B.05	gy	10.20			
		10.22	11.17	we	
		10.23	10.28	rd/be	
		10.23	10.09	vt/we	
03.16	rd/be	10.24			
		10.25	11.13	vt/we	
		10.28	11.14	oe	
03.17	gn	10.29			
B.04	gn	10.32			

Table 2.12 SRS panel AB. Card No 10 connections (Card type DAF 2/13)

From	Colour	Terminal	To	Colour	Note
10.03	gn	11.03	12.28	we	Shift signal
B.03	oe	11.04			
10.05	be	11.05	12.03	be	- 12 V
10.06	rd	11.06	12.02	rd	+ 6 V
		11.08	11.31	rd/be	
		11.09	16.33	vt/we	Set address A5+p
03.34	we	11.10			
		11.11	11.27	oe	
10.25	vt/we	11.13			
10.28	oe	11.14	13.28	rd/be	Set adress A1 - 4
03.15	oe	11.15			
10.22	we	11.17			
B.02	gy	11.18			
10.19	bk	11.19	12.18	bk	0 V
B.16	gn	11.20			
		11.21	13.22	gy	Output SH
		11.30	13.33	gn	Output SH

Table 2.13 SRS panel AB. Card No 11 connections
(Card type DAF 2/13)

From	Colour	Terminal	To	Colour	Note
11.06	rd	12.02	13.02	rd	+ 6 V
11.05	be	12.03	13.03	be	- 12 V
		12.04	15.26	gy	
		12.06	14.16	oe	
		12.10	12.31	oe	
		12.12	17.16	gy	
		12.14	12.26	rd/be	
		12.16	16.05	gn	
11.19	bk	12.18	13.18	bk	0 V
A.25	gy	12.22			
		12.24	17.15	gn	
11.03	we	12.28	13.24	we	
		12.30	12.08	vt/we	
		12.32	15.32	rd/be	
		12.33	20.03	we	

Table 2.14 SRS panel AB. Card No 12 connections
(Card type DAF 2/16)

From	Colour	Terminal	To	Colour	Note
12.02	rd	13.02	14.02	rd	+ 6 V
12.03	be	13.03	14.03	be	- 12 V
		13.08	14.31	we	
		13.10	19.07	rd/be	
		13.12	17.14	vt/we	
		13.14	16.26	vt/we	
12.18	bk	13.18	14.18	bk	0 V
11.21	gy	13.22			
12.28	we	13.24			
		13.26	16.18	rd/be	
11.14	rd/be	13.28	16.11	oe	
		13.30	18.32	gy	
		13.31	19.20	we	
		13.32	20.21	gn	
11.30	gn	13.33			

Table 2.15 SRS panel AB. Card No 13 connections
(Card type DAF 2/16)

From	Colour	Terminal	To	Colour	Note
13.02	rd	14.02	15.06	rd	+ 6 V
13.03	be	14.03	15.05	be	- 12 V
		14.06	19.08	gy	
		14.08	19.04	gn	
		14.10	19.05	we	
		14.12	20.13	oe	
		14.14	20.17	rd/be	
12.06	oe	14.16	18.28	oe	
13.18	bk	14.18	15.18	bk	0 V
		14.22	19.06	vt/we	
		14.26	16.10	gy	
08.09	we	14.28	16.12	gn	
13.08	we	14.31			
		14.32	18.30	we	

Table 2.16 SRS panel AB. Card No 14 connections (Card type DAF 2/16)

From	Colour	Terminal	To	Colour	Note
07.20	gy	15.02			
06.20	we	15.03			
07.34	gn	15.04	16.08	vt/we	
14.03	be	15.05	16.04	be	- 12 V
14.02	rd	15.06	16.02	rd	+ 6 V
06.34	vt/we	15.07	16.09	vt/we	
07.22	oe	15.08			
		15.09	15.12	rd/be	
		15.12	15.14	oe	
06.22	gn	15.13			
		15.14	15.16	gy	
		15.16	15.31	gn	
14.18	bk	15.18	16.14	bk	0 V
		15.25	15.28	gn	
12.04	gy	15.26	16.13	rd/be	
		15.27	16.22	gy	
		15.28	15.30	we	
		15.29	16.06	oe	
		15.30	16.28	vt/we	
		15.31	15.33	we	
12.32	rd/be	15.32			
		15.33	15.35	bk	
A.02	rd/be	15.34			

Table 2.17 SRS panel AB. Card No 15 connections (Card type DAF 2/12)

From	Colour	Terminal	To	Colour	Note
15.06	rd	16.02	17.06	rd	+ 6 V
15.05	be	16.04	17.02	be	- 12 V
12.16	gn	16.05	18.17	we	
15.29	oe	16.06			
A.03	gy	16.07			
15.04	vt/we	16.08			
15.07	vt/we	16.09			
14.26	gy	16.10			
13.28	oe	16.11	20.28	oe	
14.28	gn	16.12			
15.26	rd/be	16.13			
15.18	bk	16.14	17.18	bk	0 V
		16.16	16.23	oe	
13.26	rd/be	16.18			
15.27	gy	16.22			
		16.24	20.27	gn	
13.14	vt/we	16.26			
15.30	vt/we	16.28			
A.06	vt/we	16.29			Repeat ind
A.07	rd/be	16.32			Wait ind
11.09	vt/we	16.33			

Table 2.18 SRS panel AB. Card No 16 connections (Card type DAF 2/10)

From	Colour	Terminal	To	Colour	Note
16.04	be	17.02	18.02	be	- 12 V
16.02	rd	17.06	18.06	rd	+ 6 V
		17.08	17.12	gn	
		17.09	17.32	we	
		17.11	19.26	rd/be	
13.12	vt/we	17.14	18.16	gn	
12.24	gn	17.15	19.24	vt/we	
12.12	gy	17.16	19.10	we	
16.14	bk	17.18	18.18	bk	0 V
		17.20	19.28	oe	
		17.23	19.27	gy	
		17.26	17.27	vt/we	

Table 2.19 SRS panel AB. Card No 17 connections (Card type DAF 2/14)

From	Colour	Terminal	To	Colour	Note
17.02	be	18.02	19.02	be	- 12 V
17.06	rd	18.06	19.22	rd	+ 6 V
		18.08	18.12	gy	
		18.09	19.12	we	
		18.13	19.16	gn	
17.14	gn	18.16	19.19	oe	
16.05	we	18.17			
17.18	bk	18.18	19.21	bk	0 V
14.16	oe	18.28			
A.04	rd/be	18.28			
14.32	we	18.30			
13.30	gy	18.32			

Table 2.20 SRS panel AB. Card No 18 connections (Card type DAF 2/14)

From	Colour	Terminal	To	Colour	Note
18.02	be	19.02	20.05	be	- 12 V
14.08	gn	19.04			
14.10	we	19.05			
14.22	vt/we	19.06			
13.10	rd/be	19.07			
14.06	gy	19.08			
17.16	we	19.10			
18.09	we	19.12			
18.13	gn	19.16			
18.16	oe	19.19	20.30	vt/we	
13.31	we	19.20			
18.18	bk	19.21	20.18	bk	0 V
18.06	rd	19.22	20.06	rd	+ 6 V
17.15	vt/we	19.24			
17.11	rd/be	19.26	19.11	gy	
17.23	gy	19.27	19.18	vt/we	
17.20	oe	19.28	19.13	gn	
A.08	oe	19.29			
19.30	rd/be	19.09			
19.32	we	19.14			
19.33	rd/be	19.17			
19.34	oe	19.15			

Table 2.21 SRS panel AB. Card No 19 connections (Card type DAF 2/15)

From	Colour	Terminal	To	Colour	Note
12.33	we	20.03			
19.02	be	20.05	21.04	be	- 12 V
19.22	rd	20.06	21.02	rd	+ 6 V
14.12	oe	20.13			
		20.14	20.16	gy	
		20.16	20.26	gn	
14.14	rd/be	20.17	20.25	gy	
19.21	bk	20.18	21.28	bk	0 V
03.32	gn	20.21	13.32	gn	
		20.25	20.34	gn	
		20.26	20.29	we	
16.24	gn	20.27			
16.11	oe	20.28			
		20.29	20.31	vt/we	
19.19	vt/we	20.30			
		20.31	20.33	rd/be	
		20.33	20.19	oe	

Table 2.22 SRS panel AB. Card No 20 connections (Card type DAF 2/12)

From	Colour	Terminal	To	Colour	Note
20.06	rd	21.02	22.14	rd	+ 6 V
20.05	be	21.04	22.04	be	- 12 V
A.11	rd/be	21.06			
A.12	oe	21.08			
A.10	vt/we	21.10			
A.13	gn	21.12			
A.16	rd/be	21.14			
A.17	we	21.16			
A.15	vt/we	21.18			
A.18	gy	21.20			
		21.20	21.32	oe	
A.14	we	21.22			
A.09	we	21.24			
20.18	bk	21.28	21.30	bk	0 V
		21.30	22.30	bk	0 V
A.24	gn	21.34			

Table 2.23 SRS panel AB. Card No 21 connections (Card type DAF 2/3)

From	Colour	Terminal	To	Colour	Note
A.29	oe	22.02			
A.19	be	22.04			- 12 V
21.04	be	22.04			- 12 V
A.35	vt/we	22.06	22.16	oe	
A.34	rd/be	22.08			
A.33	oe	22.10			
A.21	rd	22.14			+ 6 V
21.02	rd	22.14			+ 6 V
A.23	vt/we	22.16			
		22.18	22.26	gy	
		22.24	22.22	vt/we	
A.32	gy	22.26			Rx relay
A.31	gn	22.28	22.20	gn	Rx relay
A.22	bk	22.30			0 V
21.30	bk	22.30			0 V
A.30	rd/be	22.32			

Table 2.24 SRS panel AB. Card No 22 connections (Card type DAF 1/14)

From	Colour	Terminal	To	Colour	Note
E. 02	gn	C. 02	17. 32	gn	
E. 03	gy	C. 03	17. 30	gy	
E. 04	gn	C. 04	18. 32	gn	
E. 05	gy	C. 05	18. 30	gy	
E. 06	gn	C. 06	19. 32	gn	
E. 07	gy	C. 07	19. 30	gy	
E. 08	gn	C. 08	20. 32	gn	
E. 09	gy	C. 09	20. 30	gy	
E. 10	gn	C. 10	21. 32	gn	
E. 11	gy	C. 11	21. 30	gy	
E. 12	oe	C. 12	17. 12	oe	
E. 13	vt/we	C. 13	17. 10	vt/we	
E. 14	oe	C. 14	18. 12	oe	
E. 15	vt/we	C. 15	18. 10	vt/we	
E. 16	oe	C. 16	19. 12	oe	
E. 17	vt/we	C. 17	19. 10	vt/we	
E. 18	oe	C. 18	20. 12	oe	
E. 19	vt/we	C. 19	20. 10	vt/we	
E. 20	oe	C. 20	21. 12	oe	
E. 21	we	C. 21	17. 08	we	
SW4. 06b	we	C. 21			
E. 22	rd/be	C. 22	17. 24	rd/be	
SW4. 08b	rd/be	C. 22			
E. 23	we	C. 23	18. 08	we	
SW4. 10b	we	C. 23			
E. 24	rd/be	C. 24	18. 24	rd/be	
SW4. 12b	rd/be	C. 24			
E. 25	we	C. 25	19. 08	we	
SW4. 14b	we	C. 25			
E. 26	rd/be	C. 26	19. 24	rd/be	
SW4. 16b	rd/be	C. 26			
E. 27	we	C. 27	20. 08	we	
SW4. 18b	we	C. 27			
E. 28	rd/be	C. 28	20. 24	rd/be	
SW4. 20b	rd/be	C. 28			
E. 29	we	C. 29	21. 08	we	
SW4. 22b	we	C. 29			
E. 30	rd/be	C. 30	21. 24	rd/be	
SW4. 24b	rd/be	C. 30			
E. 31	vt/we	C. 31	10. 32	vt/we	
A3. 02	be	C. 32	21. 03	bk	- 12 V
A. 20	be	C. 32			
A. 22	bk	C. 33			
A. 21	rd	C. 34			
PS3. 10	bk	C. 33	21. 18	bk	0 V
A4. 02	rd	C. 34	21. 02	rd	+ 6 V

Table 3. 1 SRS panel CD. Plug C connections (Plug card type DAF 1/2/12)

From	Colour	Terminal	To	Colour	Note
M. 21	gy	D. 02	11. 04	gy	
M. 22	oe	D. 03	11. 18	oe	
M. 23	we	D. 04	11. 20	we	
M. 24	rd/be	D. 05	11. 32	rd/be	
M. 25	vt/we	D. 06	12. 04	vt/we	
M. 26	gy	D. 07	12. 18	gy	
M. 27	oe	D. 08	12. 20	oe	
M. 28	we	D. 09	12. 32	we	
M. 29	rd/be	D. 10	13. 04	rd/be	
M. 30	vt/we	D. 11	13. 18	vt/we	
M. 31	gy	D. 12	13. 20	gy	
M. 32	oe	D. 13	13. 32	oe	
M. 33	we	D. 14	14. 04	we	
M. 34	rd/be	D. 15	14. 18	rd/be	
M. 35	vt/we	D. 16	14. 20	vt/we	
G. 02	vt/we	D. 17	17. 07	vt/we	
G. 03	rd/be	D. 18	17. 22	rd/be	
G. 04	oe	D. 19	18. 07	oe	
G. 05	we	D. 20	18. 22	we	
G. 06	gn	D. 21	19. 07	gn	
G. 07	gy	D. 22	19. 22	gy	
G. 08	vt/we	D. 23	20. 07	vt/we	
G. 09	rd/be	D. 24	20. 22	rd/be	
G. 10	oe	D. 25	21. 07	oe	
G. 11	we	D. 26	21. 22	we	
SW3. 17a	oe	D. 27	06. 06	oe	
SW4. 13a	rd/be	D. 28	21. 20	rd/be	

Table 3. 2 SRS panel CD. Plug D connections
(Plug card type DAF 1/2/13)

From	Colour	Terminal	To	Colour	Note
		01. 02	02. 06	rd	+ 6 V
		01. 04	02. 02	be	- 12 V
		01. 10	01. 24	we	
		01. 22	01. 32	we	
		01. 22	01. 18	we	
		01. 28	15. 16	we	
		01. 30	02. 34	bk	0 V
		01. 34	02. 16	we	
		01. 34	04. 10	we	

Table 3. 3 SRS panel CD. Card No 1 connections
(Card type DAF 2/3)

From	Colour	Terminal	To	Colour	Note
01.04	be	02.02	03.02	be	- 12 V
01.02	rd	02.06	03.06	rd	+ 6 V
		02.09	04.17	vt/we	B
		02.09	02.32	we	
		02.10	07.30	rd/be	
		02.11	04.08	oe	$\overline{B}$
		02.13	02.12	oe	
		02.15	07.06		$\overline{A}$
		02.15	04.09	gy	
01.34	we	02.16			
		02.20	07.08	vt/we	C
		02.20	04.07	we	
		02.23	04.26	gy	$\overline{D}$
		02.23	07.10	rd/be	
		02.26	02.24	vt/we	
01.30	bk	02.34	03.34	bk	0 V

Table 3.4 SRS panel CD. Card No 2 connections (Card type DAF 2/14)

From	Colour	Terminal	To	Colour	Note
02.02	be	03.02	04.02	be	- 12 V
02.06	rd	03.06	06.02	rd	+ 6 V
		03.09	05.12	rd/be	
		03.10	03.28	gy	
		03.13	03.12	oe	
		03.14	03.10	rd/be	
		03.15	05.11	vt/we	
		03.16	08.14	gy	
		03.20	03.24	we	
		03.20	05.13	gy	
		03.21	05.28	rd/be	
		03.21	05.14	oe	
		03.22	16.28	we	
		03.23	05.18	we	
		03.28	03.22	oe	
		03.30	05.29	gy	
		03.32	07.28	vt/we	
02.34	bk	03.34	06.34	bk	0 V

Table 3.5 SRS panel CD. Card No 3 connections (Card type DAF 2/14)

From	Colour	Terminal	To	Colour	Note
03.02	be	04.02	05.02	be	- 12 V
		04.03	07.22	gy	$S\bar{A}\bar{B}CD$
		04.04	07.24	oe	SACD
		04.05	07.26	we	$AB\bar{C}D$
		04.06	07.12	rd/be	D
		04.06	04.14	gy	D
02.20	we	04.07	04.13	rd/be	C
02.11	oe	04.08	04.28	we	$\bar{B}$
02.15	gy	04.09	05.10	gy	$\bar{A}$
01.34	we	04.10	04.11	rd/be	S
		04.11	05.06	vt/we	
		04.12	07.16	vt/we	A
		04.12	04.16	rd/be	
		04.14	04.19	oe	D
		04.16	04.29	gy	A
02.09	vt/we	04.17	05.09	oe	B
		04.18	07.14	we	$\bar{C}$
		04.18	04.27	vt/we	
		04.19	05.07	we	D
		04.21	04.22	oe	$A\bar{B}\bar{C}\bar{D}$
		04.21	15.22	vt/we	
		04.24	04.34	rd/be	
		04.24	16.26	rd/be	
02.23	gy	04.26			$\bar{D}$
		04.27	05.08	rd/be	$\bar{C}$
		04.30	08.12	gy	
		04.31	08.30	oe	

Table 3.6 SRS panel CD. Card No 4 connections
(Card type DAF 3/9)

From	Colour	Terminal	To	Colour	Note
04.02	be	05.02	06.04	be	- 12 V
		05.03	15.24	oe	$\bar{A}B\bar{C}D$
		05.04	15.08	oe	
		05.05	10.22	we	
04.11	vt/we	05.06			
04.19	we	05.07			
04.27	rd/be	05.08			
04.17	oe	05.09			
04.09	gy	05.10			
03.15	vt/we	05.11	05.16	we	
03.09	rd/be	05.12			
03.20	gy	05.13	05.17	vt/we	
03.21	oe	05.14			
03.23	we	05.18			
		05.19	09.21	rd/be	
		05.20	15.12	gy	
		05.22	05.34	vt/we	
		05.27	08.12	oe	
03.21	rd/be	05.28			
03.30	gy	05.29			
		05.34	15.26	gy	

Table 3.7 SRS panel CD. Card No 5 connections
(Card type DAF 3/9)

From	Colour	Terminal	To	Colour	Note
03.06	rd	06.02	07.02	rd	+ 6 V
05.02	be	06.04	07.04	be	- 12 V
		06.05	11.15	vt/we	
D.27	oe	06.06			
		06.08	14.30	gy	
		06.10	14.11	oe	
		06.12	10.03	oe	
		06.14	10.02	gy	
		06.16	09.16	rd/be	
		06.22	14.16	we	
		06.24	13.25	vt/we	
		06.26	13.30	rd/be	
		06.28	10.06	rd/be	
		06.30	10.05	vt/we	
		06.32	10.04	we	
03.34	bk	06.34	07.34	bk	0 V

Table 3.8 SRS panel CD. Card No 6 connections
(Card type DAF 3/10)

From	Colour	Terminal	To	Colour	Note
06.02	rd	07.02	08.02	rd	+ 6 V
06.04	be	07.04	08.03	be	- 12 V
02.15	we	07.06			
02.20	vt/we	07.08			
02.23	rd/be	07.10			
04.06	rd/be	07.12			
04.18	we	07.14			
04.12	vt/we	07.16	08.22	oe	
04.03	gy	07.22			
04.04	oe	07.24			
04.05	we	07.26			
03.32	vt/we	07.28			
02.10	rd/be	07.30	09.13	vt/we	
		07.32	08.10	gy	
06.34	bk	07.34	08.35	bk	0 V

Table 3.9 SRS panel CD. Card No 7 connections
(Card type DAF 3/10)

From	Colour	Terminal	To	Colour	Note
07.02	rd	08.02	09.06	rd	+ 6 V
07.04	be	08.03	09.05	be	- 12 V
		08.08	11.07	gy	
07.32	gy	08.10	09.25	rd/be	
04.30	gy	08.12			
05.27	oe	08.12			
03.16	gy	08.14			
07.16	oe	08.22			
		08.24	09.21	gn	
		08.26	11.14	vt/we	
		08.28	11.03	rd/be	
04.31	oe	08.30			
		08.31	08.06	oe	
		08.32	09.02	gy	
		08.33	08.18	bk	
07.34	bk	08.35	09.35	bk	0 V

Table 3.10 SRS panel CD. Card No 8 connections
(Card type DAF 2/16)

From	Colour	Terminal	To	Colour	Note
08.32	gy	09.02			
08.03	be	09.05	10.18	be	- 12 V
08.02	rd	09.06	10.20	rd	+ 6 V
		09.08	09.30	we	
		09.08	15.30	oe	
		09.09	09.19	bk	
		09.11	15.32	oe	
		09.12	09.09	bk	
07.30	vt/we	09.13			
		09.14	09.33	bk	
		09.15	15.06	gy	
06.16	rd/be	09.16			
		09.17	16.10	vt/we	
05.19	rd/be	09.21			
08.24	gn	09.21			
		09.22	16.22	gn	
		09.23	16.22	vt/we	
		09.24	16.12	rd/be	
08.10	rd/be	09.25			
		09.26	09.18	bk	
		09.28	09.11	gy	
		09.29	09.18	bk	
		09.30	15.10	rd/be	
		09.31	15.14	gy	
		09.33	09.19	bk	
		09.34	15.28	rd/be	
08.35	bk	09.35	10.34	bk	0 V

Table 3.11 SRS panel CD. Card No 9 connections (Card type DAF 2/12)

From	Colour	Terminal	To	Colour	Note
06.14	gy	10.02			
06.12	oe	10.03			
06.32	we	10.04			
06.30	vt/we	10.05			
06.28	rd/be	10.06			
		10.07	17.26	we	
		10.08	17.28	vt/we	
		10.10	18.26	rd/be	
		10.11	18.28	gy	
		10.12	19.26	oe	
		10.13	19.28	we	
		10.14	20.26	vt/we	
		10.15	20.28	rd/be	
		10.16	21.26	gy	
		10.17	21.28	oe	
09.05	be	10.18	11.05	be	- 12 V
09.06	rd	10.20	11.06	rd	+ 6 V
05.05	we	10.22			
		10.26	17.14	we	
C.31	vt/we	10.32			
09.35	bk	10.34	11.35	bk	0 V

Table 3.12 SRS panel CD. Card No 10 connections (Card type DAF 3/6)

From	Colour	Terminal	To	Colour	Note
08.28	rd/be	11.03	16.06	vt/we	
D.02	gy	11.04			
10.18	be	11.05	12.05	be	- 12 V
10.20	rd	11.06	12.06	rd	+ 6 V
08.08	gy	11.07			
		11.08	11.31	gy	
		11.08	17.04	rd/be	
		11.11	11.27	oe	
		11.13	11.02	be	
08.26	vt/we	11.14			
06.05	vt/we	11.15			
		11.17	11.19	bk	
D.03	oe	11.18			
D.04	we	11.20			
		11.21	17.05	gy	
		11.22	18.04	oe	
		11.22	12.17	we	
		11.25	12.13	vt/we	
D.05	rd/be	11.32			
10.34	bk	11.35	12.35	bk	0 V

Table 3.13 SRS panel CD. Card No 11 connections (Card type DAF 2/13)

From	Colour	Terminal	To	Colour	Note
		12.03	13.03	we	
D.06	vt/we	12.04			
11.05	be	12.05	13.05	be	- 12 V
11.06	rd	12.06	13.06	rd	+ 6 V
		12.07	18.05	we	
		12.08	12.31	vt/we	
		12.08	19.04	vt/we	
		12.11	12.27	rd/be	
11.25	vt/we	12.13			
11.22	we	12.17			
D.07	gy	12.18			
D.08	oe	12.20			
		12.21	19.05	rd/be	
		12.22	20.04	gy	
		12.22	13.17	gy	
		12.25	13.13	oe	
D.09	we	12.32			
11.35	bk	12.35	13.35	bk	0 V

Table 3.14 SRS panel CD. Card No 12 connections (Card type DAF 2/13)

From	Colour	Terminal	To	Colour	Note
12.03	we	13.03	14.03	oe	
D.10	rd/be	13.04			
12.05	be	13.05	14.05	be	- 12 V
12.06	rd	13.06	14.06	rd	+ 6 V
		13.07	20.05	oe	
		13.08	21.04	we	
		13.08	13.31	we	
		13.11	13.27	vt/we	
12.25	oe	13.13			
12.22	gy	13.17			
D.11	vt/we	13.18			
D.12	gy	13.20			
		13.22	14.17	rd/be	
06.24	vt/we	13.25	14.13	gy	
06.26	rd/be	13.30			
D.13	oe	13.32			
12.35	bk	13.35	14.35	bk	0 V

Table 3.15 SRS panel CD. Card No 13 connections
(Card type DAF 2/13)

From	Colour	Terminal	To	Colour	Note
13.03	oe	14.03			
D.14	we	14.04			
13.05	be	14.05	15.04	be	- 12 V
13.06	rd	14.06	15.02	rd	+ 6 V
		14.08	14.31	vt/we	
06.10	oe	14.11	14.27	rd/be	
13.25	gy	14.13			
06.22	we	14.16			
13.22	rd/be	14.17			
D.15	rd/be	14.18			
D.16	vt/we	14.20			
06.08	gy	14.30			
		14.34	16.24	bk	
13.35	bk	14.35	15.34	bk	0 V

Table 3.16 SRS panel CD. Card No 14 connections
(Card type DAF 2/13)

From	Colour	Terminal	To	Colour	Note
14.06	rd	15.02	16.02	rd	+ 6 V
14.05	be	15.04	16.04	be	- 12 V
09.15	gy	15.06			
05.04	oe	15.08			
09.30	rd/be	15.10			
05.20	gy	15.12			
09.31	gy	15.14			
01.28	we	15.16			
04.21	vt/we	15.22			
05.03	oe	15.24			
05.34	gy	15.26			
09.34	rd/be	15.28			
09.08	oe	15.30			
09.11	oe	15.32			
14.35	bk	15.34	16.18	bk	0 V

Table 3.17 SRS panel CD. Card No 15 connections
(Card type DAF 3/10)

From	Colour	Terminal	To	Colour	Note
15.02	rd	16.02	17.02	rd	+ 6 V
15.04	be	16.04	17.03	be	- 12 V
11.03	vt/we	16.06			
		16.08	16.20	oe	
09.17	vt/we	16.10			
09.24	rd/be	16.12			
15.34	bk	16.18	17.18	bk	0 V
09.22	gn	16.22			
09.23	vt/we	16.22			
04.24	rd/be	16.26			
03.22	we	16.28			
14.34	bk	16.24			

Table 3.18 SRS panel CD. Card No 16 connections
(Card type DAF 3/11)

From	Colour	Terminal	To	Colour	Note
16.02	rd	17.02	18.02	rd	+ 6 V
16.04	be	17.03	18.03	be	- 12 V
11.08	rd/be	17.04			
11.21	gy	17.05			
		17.06	17.20	oe	
D.17	vt/we	17.07			
C.21	we	17.08			
10.26	we	17.14	17.16	gy	
		17.16	18.14	gy	
16.18	bk	17.18	18.18	bk	0 V
		17.20	18.06	oe	
D.18	rd/be	17.22			
C.22	rd/be	17.24			
10.07	we	17.26			
10.08	vt/we	17.28			
C.03	gy	17.30			
C.02	gn	17.32			
C.13	vt/we	17.10			
C.12	oe	17.12			

Table 3.19 SRS panel CD. Card No 17 connections
(Card type DAF 3/7)

From	Colour	Terminal	To	Colour	Note
17.02	rd	18.02	19.02	rd	+ 6 V
17.03	be	18.03	19.03	be	- 12 V
11.22	oe	18.04			
12.07	we	18.05			
17.20	oe	18.06	18.20	oe	
D.19	oe	18.07			
C.23	we	18.08			
17.16	gy	18.14	18.16	gy	
		18.16	19.14	gy	
17.18	bk	18.18	19.18	bk	0 V
		18.20	19.06	oe	
D.20	we	18.22			
C.24	rd/be	18.24			
10.10	rd/be	18.26			
10.11	gy	18.28			
C.05	gy	18.30			
C.04	gn	18.32			
C.15	vt/we	18.10			
C.14	oe	18.12			

Table 3.20 SRS panel CD. Card No 18 connections
(Card type DAF 3/7)

From	Colour	Terminal	To	Colour	Note
18.02	rd	19.02	20.02	rd	+ 6 V
18.03	be	19.03	20.03	be	- 12 V
12.08	vt/we	19.04			
12.21	rd/be	19.05			
18.20	oe	19.06	19.20	oe	
D.21	gn	19.07			
C.25	we	19.08			
18.16	gy	19.14	19.16	gy	
		19.16	20.14	gy	
18.18	bk	19.18	20.18	bk	0 V
		19.20	20.06	oe	
D.22	gy	19.22			
C.26	rd/be	19.24			
10.12	oe	19.26			
10.13	we	19.28			
C.07	gy	19.30			
C.06	gn	19.32			
C.17	vt/we	19.10			
C.16	oe	19.12			

Table 3.21 SRS panel CD. Card No 19 connections
(Card type DAF 3/7)

From	Colour	Terminal	To	Colour	Note
19.02	rd	20.02	21.02	rd	+ 6 V
19.03	be	20.03	21.03	be	- 12 V
12.22	gy	20.04			
13.07	oe	20.05			
19.20	oe	20.06	20.20	oe	
D.23	vt/we	20.07			
C.27	we	20.08			
19.16	gy	20.14	20.16	gy	
		20.16	21.14	gy	
19.18	bk	20.18	21.18	bk	0 V
		20.20	21.06	oe	
D.24	rd/be	20.22			
C.28	rd/be	20.24			
10.14	vt/we	20.26			
10.15	rd/be	20.28			
C.09	gy	20.30			
C.08	gn	20.32			
C.19	vt/we	20.10			
C.18	oe	20.12			

Table 3.22 SRS panel CD. Card No 20 connections
(Card type DAF 3/7)

From	Colour	Terminal	To	Colour	Note
C.34	rd	21.02			+ 6 V
20.02	rd	21.02			+ 6 V
C.32	be	21.03			- 12 V
20.03	be	21.03			- 12 V
13.08	we	21.04			
20.20	oe	21.06	21.20	oe	
D.25	oe	21.07			
C.29	we	21.08			
20.16	gy	21.14	21.16	gy	
20.18	bk	21.18			0 V
C.33	bk	21.18			0 V
D.28	rd/be	21.20			
D.26	we	21.22			
C.30	rd/be	21.24			
10.16	gy	21.26			
10.17	oe	21.28			
C.11	gy	21.30			
C.10	gn	21.32			
C.20	oe	21.12			

Table 3.23 SRS panel CD. Card No 21 connections
(Card type DAF 3/7)

From	Colour	Terminal	To	Colour	Note
C.02	gn	E.02	17.14	gn	
C.03	gy	E.03	17.12	gn	
C.04	gn	E.04	17.10	gn	
C.05	gy	E.05	17.32	gn	
C.06	gn	E.06	17.30	gn	
C.07	gy	E.07	18.14	gn	
C.08	gn	E.08	18.12	gn	
C.09	gy	E.09	18.10	gn	
C.10	gn	E.10	18.32	gn	
C.11	gy	E.11	18.30	gn	
C.12	oe	E.12	02.04	we	
C.13	vt/we	E.13	04.04	we	
C.14	oe	E.14	06.04	we	
C.15	vt/we	E.15	08.04	we	
C.16	oe	E.16	10.04	we	
C.17	vt/we	E.17	12.04	we	
C.18	oe	E.18	14.04	we	
C.19	vt/we	E.19	16.04	we	
C.20	oe	E.20	18.04	we	
C.21	we	E.21	17.18	oe	
C.22	rd/be	E.22	17.20	oe	
C.23	we	E.23	17.22	oe	
C.24	rd/be	E.24	17.24	oe	
C.25	we	E.25	17.26	oe	
C.26	rd/be	E.26	18.18	oe	
C.27	we	E.27	18.20	oe	
C.28	rd/be	E.28	18.22	oe	
C.29	we	E.29	18.24	oe	
C.30	rd/be	E.30	18.26	oe	
C.31	vt/we	E.31	18.02	vt/we	
G.24	be	E.32	18.06	be	- 12 V
G.25	bk	E.33	18.16	bk	0 V
G.26	rd	E.34	18.08	rd	+ 6 V

Table 4.1 SRS panel EF. Plug E connections
(Plug card type DAF 1/2/14)

From	Colour	Terminal	To	Colour	Note
M.15	gy	F.02	01.34	gy	
M.14	we	F.03	03.34	we	
M.13	rd/be	F.04	05.34	rd/be	
M.12	gy	F.05	07.34	gy	
M.11	gn	F.06	09.34	gn	
M.10	oe	F.07	11.34	oe	
M.09	we	F.08	13.34	we	
M.08	vt/we	F.09	15.34	vt/we	
M.07	rd/be	F.10	17.34	rd/be	
H.12	gy	F.20	02.28	gy	
H.13	vt/we	F.21	04.28	vt/we	
H.14	rd/be	F.22	06.28	rd/be	
H.15	oe	F.23	08.28	oe	
H.16	we	F.24	10.28	we	
H.17	gn	F.25	12.28	gn	
H.18	gy	F.26	14.28	gy	
H.19	vt/we	F.27	16.28	vt/we	
H.20	rd/be	F.28	18.28	rd/be	

Table 4.2 SRS panel EF. Plug F connections
(Plug card type DAF 1/2/15)

From	Colour	Terminal	To	Colour	Note
12.02	gy	13.02	14.02	gy	
		13.04	14.04	we	
12.06	be	13.06	14.06	be	- 12 V
12.08	rd	13.08	14.08	rd	+ 6 V
11.10	gn	13.10	15.10	gn	
11.12	gn	13.12	15.12	gn	
11.14	gn	13.14	15.14	gn	
12.16	bk	13.16	14.16	bk	0 V
11.18	oe	13.18	15.18	oe	
11.20	oe	13.20	15.20	oe	
11.22	oe	13.22	15.22	oe	
11.24	oe	13.24	15.24	oe	
11.26	oe	13.26	15.26	oe	
		13.28	13.34	vt/we	
		13.28	14.28	rd/be	
11.30	gn	13.30	15.30	gn	
11.32	gn	13.32	15.32	gn	
F.08	we	13.34			

Table 4.15 SRS panel EF. Card No 13 connections (Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
13.02	gy	14.02	15.02	gy	
13.04	we	14.04			
E.18	we	14.04			
13.06	be	14.06	15.06	be	- 12 V
13.08	rd	14.08	15.08	rd	+ 6 V
12.10	gn	14.10	16.10	gn	
12.12	gn	14.12	16.12	gn	
12.14	gn	14.14	16.14	gn	
13.16	bk	14.16	15.16	bk	0 V
12.18	oe	14.18	16.18	oe	
12.20	oe	14.20	16.20	oe	
12.22	oe	14.22	16.22	oe	
12.24	oe	14.24	16.24	oe	
12.26	oe	14.26	16.26	oe	
13.28	rd/be	14.28			
F.26	gy	14.28			
12.30	gn	14.30	16.30	gn	
12.32	gn	14.32	16.32	gn	

Table 4.16 SRS panel EF. Card No 14 connections (Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
14.02	gy	15.02	16.02	gy	
		15.04	16.04	we	
14.06	be	15.06	16.06	be	- 12 V
14.08	rd	15.08	16.08	rd	+ 6 V
13.10	gn	15.10	17.10	gn	
13 12	gn	15.12	17.12	gn	
13.14	gn	15.14	17.14	gn	
14.16	bk	15.16	16.16	bk	0 V
13.18	oe	15.18	17.18	oe	
13.20	oe	15.20	17.20	oe	
13.22	oe	15.22	17.22	oe	
13.24	oe	15.24	17.24	oe	
13.26	oe	15.26	17.26	oe	
		15.28	15.34	vt/we	
		15.28	16.28	rd/be	
13.30	gn	15.30	17.30	gn	
13.32	gn	15.32	17.32	gn	
F.09	vt/we	15.34			

Table 4.17 SRS panel EF. Card No 15 connections
(Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
15.02	gy	16.02	17.02	gy	
15.04	we	16.04			
E.19	we	16.04			
15.06	be	16.06	17.06	be	- 12 V
15.08	rd	16.08	17.08	rd	+ 6 V
14.10	gn	16.10	18.10	gn	
14.12	gn	16.12	18.12	gn	
14.14	gn	16.14	18.14	gn	
15.16	bk	16.16	17.16	bk	0 V
14.18	oe	16.18	18.18	oe	
14.20	oe	16.20	18.20	oe	
14.22	oe	16.22	18.22	oe	
14.24	oe	16.24	18.24	oe	
14.26	oe	16.26	18.26	oe	
15.28	rd/be	16.28			
F.27	vt/we	16.28			
14.30	gn	16.30	18.30	gn	
14.32	gn	16.32	18.32	gn	

Table 4.18 SRS panel EF. Card No 16 connections
(Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
		01.04	02.04	be	- 12 V
		01.06	02.02	rd	+ 6 V
		01.08	02.10	we	$\overline{A}$
		01.09	01.32	vt/we	
		01.09	02.24	gy	$\overline{B}$
		01.10	01.28	gn	$\overline{A}$+B+C+D
		01.11	02.22	gn	B
		01.13	01.12	gy	
		01.15	02.08	oe	A
		01.16	12.05	oe	S
		01.16	04.11	gn	
		01.20	01.24	rd/be	
		01.21	03.10	we	$\overline{D}$
		01.23	03.08	oe	D
		01.26	03.06	rd/be	$\overline{C}$
		01.28	03.32	gy	
		01.30	02.26	vt/we	C

Table 5.3 SRS panel GH. Card No 1 connections (Card type DAF 2/14)

From	Colour	Terminal	To	Colour	Note
01.06	rd	02.02	03.02	rd	+ 6 V
01.04	be	02.04	03.04	be	- 12 V
01.15	oe	02.08	02.14	oe	A
01.08	we	02.10	02.12	we	$\overline{A}$
		02.12	04.12	we	$\overline{A}$
		02.14	04.09	vt/we	A
01.11	gn	02.22	02.32	gn	B
01.09	gy	02.24	02.30	gy	$\overline{B}$
01.30	vt/we	02.26	02.28	vt/we	C
		02.28	04.14	gy	C
		02.30	04.08	rd/be	$\overline{B}$
		02.32	04.13	gn	B
01.34	bk	02.34	03.34	bk	0 V

Table 5.4 SRS panel GH. Card No 2 connections (Card type DAF 3/10)

From	Colour	Terminal	To	Colour	Note
02.02	rd	03.02	07.23	rd	+ 6 V
02.04	be	03.04	04.02	be	- 12 V
01.26	rd/be	03.06	03.16	rd/be	$\overline{C}$
01.23	oe	03.08	03.14	oe	D
01.21	we	03.10	03.12	we	$\overline{D}$
		03.12	04.06	rd/be	$\overline{D}$
		03.14	04.15	we	D
		03.16	04.07	vt/we	$\overline{C}$
		03.22	04.03	oe	$A\overline{B}\overline{C}\overline{D}$
		03.24	08.16	gn	
		03.26	07.29	vt/we	
		03.28	12.12	rd/be	
		03.30	07.30	gy	
01.28	gy	03.32	07.33	oe	
02.34	bk	03.34	07.22	bk	0 V

Table 5.5 SRS panel GH. Card No 3 connections (Card type DAF 3/10)

From	Colour	Terminal	To	Colour	Note
03.04	be	04.02	05.02	be	- 12 V
03.22	oe	04.03			
		04.04	07.02	gy	$S\bar{A}BCD$
		04.05	07.09	gn	SABCD
03.12	rd/be	04.06	04.25	oe	$\bar{D}$
03.16	vt/we	04.07	05.07	vt/we	$\bar{C}$
02.30	rd/be	04.08	05.08	gy	$\bar{B}$
02.14	vt/we	04.09	04.17	vt/we	A
01.16	gn	04.11	04.16	gy	S
02.12	we	04.12	04.26	rd/be	$\bar{A}$
02.32	gn	04.13	04.18	rd/be	B
02.28	gy	04.14	04.19	oe	C
03.14	we	04.15	04.20	we	D
		04.16	04.27	vt/we	S
		04.17	04.32	vt/we	A
		04.18	05.18	we	B
		04.19	06.14	gn	C,
		04.20	05.06	rd/be	D
		04.21	04.22	gy	
		04.21	07.04	we	$S\bar{A}\bar{D}$
		04.23	04.24	gy	
		04.23	07.05	oe	$SA\bar{D}$
		04.25	04.33	rd/be	$\bar{D}$
		04.26	05.09	gn	$\bar{A}$
		04.27	04.31	gy	S
		04.31	05.10	we	S
		04.32	05.12	oe	A

Table 5.6 SRS panel GH. Card No 4 connections (Card type DAF 3/10)

From	Colour	Terminal	To	Colour	Note
04.02	be	05.02	06.02	be	- 12 V
		05.03	07.06	gy	$S\bar{A}\bar{B}\bar{C}D$
		05.04	07.07	gn	$SA\bar{B}\bar{C}D$
		05.05	07.08	we	$S\bar{A}B\bar{C}D$
04.20	rd/be	05.06	05.15	we	D
04.07	vt/we	05.07	05.14	oe	$\bar{C}$
04.08	gy	05.08	05.13	rd/be	$\bar{B}$
04.26	gn	05.09	05.17	vt/we	$\bar{A}$
04.31	we	05.10	05.11	vt/we	S
		05.11	05.16	gy	S
04.32	oe	05.12	06.09	gy	A
		05.13	06.13	gn	$\bar{B}$
		05.14	05.19	rd/be	$\bar{C}$
		05.15	05.20	oe	D
		05.16	06.10	gn	S
		05.17	06.12	we	$\bar{A}$
04.18	we	05.18	06.08	vt/we	B
		05.19	06.07	rd/be	$\bar{C}$
		05.20	06.06	oe	D
		05.21	05.22	gn	
		05.22	05.24	we	
		05.23	14.22	vt/we	
		05.24	05.23	gy	
		05.25	09.15	gy	
		05.26	08.23	we	
		05.27	08.30	gn	
		05.28	08.11	oe	
		05.29	08.15	rd/be	
		05.30	09.11	vt/we	
		05.31	09.30	rd/be	
		05.32	09.23	oe	
		05.33	10.15	gn	

Table 5.7 SRS panel GH. Card No 5 connections (Card type DAF 3/9)

From	Colour	Terminal	To	Colour	Note
05.02	be	06.02	07.35	be	- 12 V
		06.03	07.09	gy	SAB$\overline{C}$D
		06.04	07.10	oe	S$\overline{A}$BCD
		06.05	07.11	oe	SA$\overline{B}$CD
05.20	oe	06.06	06.15	rd/be	D
05.19	rd/be	06.07			
05.18	vt/we	06.08			
05.12	gy	06.09	06.17	gn	A
05.16	gn	06.10	06.11	vt/we	S
		06.11	06.16	we	S
05.17	we	06.12			
05.13	gn	06.13	06.18	gy	$\overline{B}$
04.19	gn	06.14	06.19	vt/we	C
		06.15	06.20	rd/be	D
		06.22	06.34	vt/we	
		06.27	14.30	rd/be	
		06.28	18.07	rd/be	
		06.34	19.08	gy	

Table 5.8 SRS panel GH. Card No 6 connection
(Card type DAF 3/9)

From	Colour	Terminal	To	Colour	Note
04.04	gy	07.02			
04.21	we	07.04			
04.23	oe	07.05			
05.03	gy	07.06			
05.04	gn	07.07			
05.05	we	07.08			
06.03	gy	07.09			
04.05	gn	07.09			
06.04	oe	07.10			
06.05	oe	07.11			
G.02	vt/we	07.12			
G.03	rd/be	07.13			
G.04	oe	07.14			
G.05	we	07.15			
G.06	gn	07.16			
G 07	gy	07.17			
G.08	vt/we	07.18			
G.09	rd/be	07.19			
G.10	oe	07.20			
G.11	we	07.21			
03.34	bk	07.22	08.18	bk	0 V
03.02	rd	07.23	08.06	rd	+ 6 V
		07.24	12.34	gn	
		07.25	14.28	vt/we	
		07.28	12.22	gn	
03.26	vt/we	07.29			
03.30	gy	07.30	12.18	we	
03.32	oe	07.33			
		07.34	12.19	gy	
06.02	be	07.35	08.03	be	- 12 V

Table 5.9 SRS panel GH. Card No 7 connections
(Card type DAF 3/14)

From	Colour	Terminal	To	Colour	Note
07.35	be	08.03	09.03	be	- 12 V
07.23	rd	08.06	09.06	rd	+ 6 V
		08.08	11.04	rd/be	
		08.09	11.05	oe	
		08.09	08.32	vt/we	
		08.10	08.28	gn	
05.28	oe	08.11			
		08.13	08.12	gy	
		08.14	08.10	we	
05.29	rd/be	08.15			
03.24	gn	08.16	20.16	we	1600 c/s
07.22	bk	08.18	09.18	bk	
		08.20	08.24	rd/be	
		08.21	09.16	oe	
		08.21	11.07	gn	
		08.22	09.14	vt/we	
05.26	we	08.23			
		08.26	11.06	we	
		08.28	08.22	gy	
05.27	gn	08.30			

Table 5.10 SRS panel GH. Card No 8 connections (Card type DAF 2/14)

From	Colour	Terminal	To	Colour	Note
08.03	be	09.03	10.03	be	- 12 V
08.06	rd	09.06	10.06	rd	+ 6 V
		09.13	11.08	rd/be	
		09.09	11.21	oe	
		09.09	09.32	vt/we	
		09.10	09.28	gn	
05.30	vt/we	09.11			
		09.13	09.12	gy	
08.22	vt/we	09.14	09.10	we	
05.25	gy	09.15			
08.21	oe	09.16			
08.18	bk	09.18	10.18	bk	0 V
		09.20	09.24	rd/be	
		09.21	10.16	oe	
		09.21	11.23	gn	
		09.22	10.14	vt/we	
05.32	oe	09.23			
		09.28	09.22	gy	
05.31	rd/be	09.30			

Table 5.11 SRS panel GH. Card No 9 connections (Card type DAF 2/14)

From	Colour	Terminal	To	Colour	Note
09.03	be	10.03	11.03	be	- 12 V
09.06	rd	10.06	11.02	rd	+ 6 V
		10.08	11.24	gy	
09.22	vt/we	10.14			
G.21	gn	10.14			Reset
05.33	gn	10.15			
09.21	oe	10.16			
10.18	bk	10.18	12.14	bk	

Table 5.12 SRS panel GH. Card No 10 connections (Card type DAF 2/14)

From	Colour	Terminal	To	Colour	Note
10.06	rd	11.02	12.04	rd	+ 6 V
10.03	be	11.03	12.03	be	- 12 V
08.08	rd/be	11.04			
08.09	oe	11.05			
08.26	we	11.06			
08.21	gn	11.07			
09.13	vd/be	11.08			
		11.09	12.28	we	
		11.10	12.27	oe	
		11.11	12.26	rd/be	
		11.12	12.25	vt/we	
		11.13	13.16	we	
		11.14	13.14	gn	
		11.15	13.12	gy	
		11.16	13.32	vt/we	
		11.17	13.30	rd/be	
		11.18	12.29	gn	
09.09	oe	11.21			
09.21	gn	11.23			
10.08	gy	11.24			
		11.26	12.33	oe	
		11.27	12.32	rd/be	
		11.28	12.31	vt/we	
		11.29	12.30	gy	
		11.30	13.28	oe	
		11.31	14.16	we	
		11.32	14.14	gn	
		11.33	14.12	gy	

Table 5.13 SRS panel GH. Card No 11 connections
(Card type DAF 3/13)

From	Colour	Terminal	To	Colour	Note
11.03	be	12.03	13.04	be	- 12 V
11.02	rd	12.04	13.02	rd	+ 6 V
01.16	oe	12.05			
		12.06	12.24	rd/be	
		12.06	12.02	oe	
		12.10	12.09	we	
		12.11	12.23	vt/we	
03.28	rd/be	12.12			
10.18	bk	12.14	13.18	bk	0 V
07.30	we	12.18			
07.34	gy	12.19			
		12.20	14.26	gn	
		12.20	17.14	rd/be	Set pulse
07.28	gn	12.22			
11.12	vt/we	12.25			
11.11	rd/be	12.26			
11.10	oe	12.27			
11.09	we	12.28			
11.18	gn	12.29			
11.29	gy	12.30			
11.28	vt/we	12.31			
11.27	rd/be	12.32			
11.26	oe	12.33			
07.24	gn	12.34			
		12.35	14.32	we	

Table 5.14 SRS panel GH. Card No 12 connections
(Card type DAF 3/12)

From	Colour	Terminal	To	Colour	Note
12.04	rd	13.02	14.02	rd	+ 6 V
12.03	be	13.04	14.04	be	- 12 V
H.12	gy	13.06			
H.13	vt/we	13.08			
H.14	rd/be	13.10			
11.15	gy	13.12			
11.14	gn	13.14			
11.13	we	13.16			
12.14	bk	13.18	14.18	bk	0 V
H.15	oe	13.22			
H.16	we	13.24			
H.17	gn	13.26			
11.30	oe	13.28			
11.17	rd/be	13.30			
11.16	vt/we	13.32			

Table 5.15 SRS panel GH. Card No 13 connections
(Card type DAF 3/10)

From	Colour	Terminal	To	Colour	Note
13.02	rd	14.02	15.02	rd	+ 6 V
13.04	be	14.04	15.04	be	- 12 V
H.18	gy	14.06			
H.19	vt/we	14.08			
H.20	rd/be	14.10			
11.33	gy	14.12			
11.32	gn	14.14			
11.31	we	14.16			
13.18	bk	14.18	15.18	bk	0 V
05.23	vt/we	14.22			
		14.24	18.03	gy	
12.20	gn	14.26			
07.25	vt/we	14.28			
06.27	rd/be	14.30			
12.35	we	14.32			

Table 5.16 SRS panel GH. Card No 14 connections
(Card type DAF 3/10)

From	Colour	Terminal	To	Colour	Note
14.02	rd	15.02	16.05	rd	+ 6 V
14.04	be	15.04	16.10	be	- 12 V
		15.06	16.19	we	
		15.08	16.22	vt/we	
		15.10	15.14	we	
		15.12	16.34	rd/be	
		15.16	16.07	vt/we	
14.18	bk	15.18	16.04	bk	0 V
		15.22	16.20	rd/be	
		15.24	15.32	rd/be	
		15.26	16.02	we	
		15.28	17.03	we	
H.22	vt/we	15.30			E
H.21	rd/be	15.32			$\overline{E}$

Table 5.17 SRS panel GH. Card No 15 connections
(Card type DAF 2/7)

From	Colour	Terminal	Colour	Note	
15.26	we	16.02	20.16	we	
G.12	gn	16.03			
15.18	bk	16.04	17.19	bk	0 V
15.02	rd	16.05	17.06	rd	+ 6 V
		16.06	19.10	we	
15.16	vt/we	16.07			
		16.08	19.14	rd/be	
		16.09	20.20	rd/be	
15.04	be	16.10	17.05	be	- 12 V
		16.11	18.16	vt/we	
		16.12	17.25	we	
		16.13	17.30	rd/be	
		16.14	17.11	vt/we	
		16.15	17.16	we	
		16.16	18.25	vt/we	
		16.17	18.30	rd/be	
		16.18	18.11	we	
15.06	we	16.19			
15.22	vt/we	16.20			
15.08	vt/we	16.22			
G.13	vt/we	16.23			
G.14	rd/be	16.24			
G.23	vt/we	16.26			- 50 V
G.15	we	16.28			
G.16	we	16.30			
15.12	rd/be	16.34			

Table 5.18 SRS panel GH. Card No 16 connections
(Card type DAF 1/5)

From	Colour	Terminal	To	Colour	Note
		17.02	17.10	be	
15.28	we	17.03	18.03	we	
16.10	be	17.05	18.05	be	- 12 V
16.05	rd	17.06	18.06	rd	+ 6 V
		17.08	17.31	vt/we	
		17.10	17.13	be	
16.14	vt/we	17.11	17.27	vt/we	
		17.13	17.24	be	
12.20	rd/be	17.14			
		17.15	17.17	bk	
16.15	we	17.16			
		17.17	17.34	bk	
16.04	bk	17.19	18.19	bk	0 V
		17.22	18.17	vt/we	
		17.24	17.29	be	
16.12	we	17.25	18.13	we	
16.13	rd/be	17.30			

Table 5.19 SRS panel GH. Card No 17 connections
(Card type DAF 2/13)

From	Colour	Terminal	To	Colour	Note
		18.02	18.10	be	
14.24	gy	18.03			
17.03	we	18.03			
17.05	be	18.05	19.04	be	- 12 V
17.06	rd	18.06	19.02	rd	+ 6 V
06.28	rd/be	18.07			
		18.08	18.31	vt/we	
16.18	we	18.11	18.27	we	
17.25	we	18.13			
		18.15	18.24	be	
16.11	vt/we	18.16			
17.22	vt/we	18.17			
17.19	bk	18.19	19.18	bk	0 V
		18.24	18.29	be	
16.16	vt/we	18.25			
16.17	rd/be	18.30			

Table 5.20 SRS panel GH. Card No 18 connections (Card type DAF 2/13)

From	Colour	Terminal	To	Colour	Note
18.06	rd	19.02	20.06	rd	+ 6 V
18.05	be	19.04	20.04	be	- 12 V
		19.06	20.09	vt/we	
06.34	gy	19.08			
16.06	we	19.10	19.22	we	
G.17	vt/we	19.12			
16.08	rd/be	19.14			
G.18	we	19.16			
18.19	bk	19.18	20.18	bk	0 V
		19.22	20.23	we	
G.19	rd/be	19.24			
G.20	vt/we	19.30			
		19.32	19.24	rd/be	

Table 5.21 SRS panel GH. Card No 19 connections (Card type DAF 2/7)

From	Colour	Terminal	To	Colour	Note
G.24	be	20.04			- 12 V
19.04	be	20.04			
G.26	rd	20.06			+ 6 V
19.02	rd	20.06			
		20.08	20.12	we	
		20.09	20.32	vt/we	
19.06	vt/we	20.09			
08.16	we	20.16			
16.02	we	20.16			
G.25	bk	20.18			0 V
19.18	bk	20.18			
16.09	rd/be	20.20	20.24	rd/be	
19.22	we	20.23			

Table 5.22 SRS panel GH. Card No 20 connections (Card type DAF 2/14)

From	Colour	Terminal	To	Colour	Note
SW7.12a	be	I.02	01.01	be	- 12 V
FI1.02	be	I.02	04.04	be	
PH.08	be	I.03	01.02	be	- 12 V filtered
		I.03	03.02	be	
PS2.10	bk	I.04	I.16	bk	0 V
		I.04	01.03	bk	
A4.02	rd	I.05	04.18	rd	+ 6 V
K.29	vt/we	I.06	09.33	vt/we	+ 50 V 50 mA
VM1.09	vt/we	I.06			
VM1.10	vt/we	I.07			
K.30	vt/we	I.07	06.12	vt/we	- 50 V 50 mA
6.23	vt/we	I.07			
SW7.17a	gn	I.08	07.28	gn	Gate 1 control
SW7.08a	gn	I.09	07.30	gn	I.08 neg. for sig.
SW7.17b	oe	I.10	08.28	oe	Gate 2 control
SW7.08b	oe	I.11	08.30	oe	I.10 neg, for rdbk
PH.01	scrd	I.12	09.29	scrd	X1 screens to I.16
PH.02	scrd	I.13	09.31	scrd	X2
PH.04	scrd	I.14	10.29	scrd	Y1
PH.03	scrd	I.15	10.31	scrd	Y2
PI.10	bk	I.16	I.22	bk	0 V
PH.05	bk	I.16	scrs		0 V
PH.13	we	I.17	04.24	we	IFF sens.
PH.12	we	I.18	04.34	we	IFF output
SW8.13a	gy	I.19	05.26	gy	Mod input
PH.14	gy	I.20	05.08	gy	Zero circle
PI.09	gn	I.21	06.14	gn	
PF.08	bk	I.22	I.24	bk	0 V
PH.10	bk	I.22			
G.12	gn	I.23	03.30	gn	1600 c/s
VM1.E	bk	I.24	I.28	bk	0 V
SW7.14a	bk	I.24	scrs		
PF.07	scrd	I.25	05.20	scrd	RS1.S1 scrs to I.24
PF.01	scrd	I.26	07.12	scrd	RS1.R1
PF.04	scrd	I.27	07.08	scrd	RS1.R4
K.14	bk	I.28	I.32	bk	0 V
M.17	bk	I.28	scrs	bk	
PB.07	scrd	I.29	03.16	scrd	RS2.S1 scrs to I.28
PB.01	scrd	I.30	08.16	scrd	RS2.R1
PB.04	scrd	I.31	07.16	scrd	RS2.R4
J.02	bk	I.32	scrs	bk	0 V
PB.08	bk	I.32	03.24	bk	0 V
K.15	scrd	I.33	03.18	scrd	RS3.S1 scrs to I.32
K.16	scrd	I.34	08.08	scrd	RS3.R1
K.17	scrd	I.35	08.12	scrd	RS3.R4

Table 6.1 SRS panel IJ. Plug I connections
(Plug card type DAF 1/2/4)

From	Colour	Terminal	To	Colour	Note
I. 32	bk	J. 02	J. 14	bk	0 V
PE. 15	bk	J. 02			
PH. 24	we	J. 03	06. 20	we	
PF. 24	gy	J. 04	06. 10	gy	
PF. 23	gy	J. 05	06. 16	gy	
PE. 09	scrd	J. 06	11. 12	scrd	U_c
PE. 13	scr	J. 07	11. 10	scr	scr for U_c
PE. 25	scrd	J. 08	11. 08	scrd	U_f
PE. 23	scr	J. 09	11. 06	scr	scr for U_f
		J. 10	11. 10	bk	0 V
		J. 11	11. 18	bk	0 V
PE. 19	bk	J. 12	11. 22	bk	0 V
		J. 13	11. 30	bk	0 V
J. 02	bk	J. 14			
PS2. 09	bk	J. 15	01. 03	bk	0 V sense
PS2. 05	be	J. 17	01. 01	be	- 12 V sense
A2. 02	be	J. 22	06. 08	be	- 12 V no 6
PE. 06	rd/be	J. 24	11. 24	rd/be	115 VAC
TA. 22	rd/be	J. 24			
PE. 01	rd/be	J. 25	11. 26	rd/be	
TA. 24	rd/be	J. 25			
SW8. 14a	gn	J. 27	11. 20	gn	Servo normal/free
SW8. 16a	gn	J. 28	11. 14	gn	
PE. 21	we	J. 30	12. 26	we	Servo motor M2
PE. 17	rd/be	J. 31	12. 18	rd/be	Servo motor M2, CT
PE. 22	we	J. 32	12. 34	we	Servo motor M2
T1. 28	oe	J. 34	12. 02	oe	51 VAC
T1. 30	oe	J. 35	12. 10	oe	

Table 6. 2 SRS panel IJ. Plug J connections
(Plug card type dAF 1/2/5)

From	Colour	Terminal	To	Colour	Note
J. 17	be	01. 01			- 12 V sense
I. 02	be	01. 01			- 12 V no 1
I. 03	be	01. 02	02. 01	be	- 12 V filtered
		01. 02	09. 09	be	
J. 15	bk	01. 03	09. 19	bk	0 V sense
I. 04	bk	01. 03			

Table 6. 3 SRS panel IJ. Card No 1 connections
(Card type FI2)

From	Colour	Terminal	To	Colour	Note
01. 02	be	02. 01			
		02. 03	03. 06	gn	
		02. 07	03. 20	oe	
		02. 08	03. 12	gy	

Table 6. 4 SRS panel IJ. Card No 2 connections
(Card type TF1)

From	Colour	Terminal	To	Colour	Note
I. 03	be	03. 02			- 12 V
		03. 02	05. 28	be	
02. 03	gn	03. 06			
02. 08	gy	03. 12			
I. 29	scr	03. 16			RS2
I. 33	scr	03. 18			RS3
02. 07	oe	03. 20			
I. 32	bk	03. 24	04. 12	bk	0 V
		03. 28	05. 32	gn	1600 c/s
I. 23	gn	03. 30			1600 c/s

Table 6. 5 SRS panel IJ. Card No 3 connections
(Card type DAF 1/2)

From	Colour	Terminal	To	Colour	Note
I. 02	be	04. 04	11. 02	be	- 12 V
PN	gn	04. 08	06. 30	oe	Radar trig
PN. scr	bk	04. 10			0 V
03. 24	bk	04. 12	05. 16	bk	0 V
I. 05	rd	04. 18	05. 34	rd	+ 6 V
I. 17	we	04. 24			IFF sense
PO	gy	04. 28			IFF pulse
PO. scr	bk	04. 30			0 V
I. 18	we	04. 34			

100 ohm 1/4 between PN and PO screen

Table 6. 6 SRS panel IJ. Card No 4 connections
(Card type DAF 1/3)

From	Colour	Terminal	To	Colour	Note
		05. 04	05. 18	oe	
I. 20	gy	05. 08			Zero circle
04. 12	bk	05. 16	06. 02	bk	0 V
I. 25	scrd	05. 20	06. 04	oe	RS1. S1
I. 19	gy	05. 26			Mod input
03. 02	be	05. 28	07. 02	be	- 12 V
03. 28	gn	05. 32			
04. 18	rd	05. 34	06. 34	rd	+ 6 V

Table 6. 7 SRS panel IJ. Card No 5 connections
(Card type DAF 1/4 A)

From	Colour	Terminal	To	Colour	Note
05.16	bk	06.02	07.34	bk	0 V
05.20	oe	06.04			
J.22	be	06.08			- 12 V
J.04	gy	06.10			
I.07	vt/we	06.12	09.03	vt/we	- 50 V
I.21	gn	06.14			Recorder
J.05	gy	06.16			
J.03	we	06.20			DAF 1
04.08	oe	06.30			
05.34	rd	06.34			

Table 6.8 SRS panel IJ. Card No 6 connections (Card type DAF 1/10)

From	Colour	Terminal	To	Colour	Note
05.28	be	07.02	08.02	be	- 12 V
		07.04	07.18	we	
I.27	scrd	07.08			Sine sig
I.26	scrd	07.12			Cos sig
I.31	scrd	07.16			Sine cursor
		07.20	08.04	we	
		07.24	08.20	rd/be	
		07.26	08.18	rd/be	
I.08	gn	07.28			
I.09	gn	07.30			
		07.32	08.32	rd	+ 6 V
06.02	bk	07.34	08.34	bk	0 V

Table 6.9 SRS panel IJ. Card No 7 connections (Card type DAF 1/8)

From	Colour	Terminal	To	Colour	Note
07.02	be	08.02		be	- 12 V
07.20	we	08.04			
I.34	scrd	08.08			Sine rdbk
I.35	scrd	08.12			Cos rdbk
I.30	scrd	08.16			Cos cursor
07.26	rd/be	08.18			
07.24	rd/be	08.20			
		08.24	10.05	gn	Cos out
		08.26	09.05	gn	Sine out
I.10	oe	08.28			
I.11	oe	08.30			
07.32	rd	08.32	11.16	rd	+ 6 V
07.34	bk	08.34	11.06	bk	0 V

Table 6.10 SRS panel IJ. Card No 8 connections (Card type DAF 1/8)

From	Colour	Terminal	To	Colour	Note
06.12	vt/we	09.03	10.03	vt/we	- 50 V
08.26	gn	09.05			
01.02	be	09.09	10.09	be	- 12 V
01.03	bk	09.19	10.19	bk	0 V
I.12	scrd	09.29			X_1 out
I.13	scrd	09.31			X_2 out
I.06	vt/we	09.33	10.33	vt/we	+ 50 V

Table 6.11 SRS panel IJ. Card No 9 connections (Card type DAF 1/9)

From	Colour	Terminal	To	Colour	Note
09.03	vt/we	10.03			
08.24	gn	10.05			
09.09	be	10.09			12 V
09.19	bk	10.19		bk	0 V
I.14	scrd	10.29			Y_1 out
I.15	scrd	10.31			Y_2 out
09.33	vt/we	10.33			

Table 6.12 SRS panel IJ. Card No 10 connections (Card type DAF 1/9)

From	Colour	Terminal	To	Colour	Note
04.04	be	11.02			
J.09	scr	11.06			
08.34	bk	11.06	12.08	bk	0 V
J.08	scrd	11.08			U_f
J.07	scr	11.10			
J.10	bk	11.10			
J.06	scrd	11.12			U_c
J.28	gn	11.14			
08.32	rd	11.16			
J.11	bk	11.18			
J.27	gn	11.20			
J.12	bk	11.22			
J.24	rd/be	11.24			115 VAC
J.25	rd/be	11.26			115 VAC
		11.28	12.22	oe	Output A
J.13	bk	11.30			0 V
		11.32	12.30	oe	Output A

Table 6.13 SRS panel IJ. Card No 11 connections (Card type DAF 1/11)

From	Colour	Terminal	To	Colour	Note
J.34	oe	12.02			51 VAC
11.06	bk	12.08			
J.35	oe	12.10			51 VAC
J.31	rd/be	12.18			
11.28	oe	12.22			
J.30	we	12.26			
11.32	oe	12.30			
J.32	we	12.34			

Table 6.14 SRS panel IJ. Card No 12 connections (Card type DAF 1/12)

From	Colour	Terminal	To	Colour	Note
A1.02	be	K.02	01.04	be	- 12 V
PS1.10	bk	K.03	01.02	bk	0 V
A4.02	rd	K.04	01.08	rd	+ 6 V
T1.08	gn	K.05	05.02	gn	120 VAC No 1
T1.10	gn	K.06	05.04	gn	
T1.12	gn	K.07	06.02	gn	120 VAC No 2
T1.14	gn	K.08	06.04	gn	
T1.16	oe	K.09	03.02	oe	55 VAC No 1
T1.18	oe	K.10	03.04	oe	
T1.20	oe	K.11	04.02	oe	55 VAC No 2
T1.22	oe	K.12	04.04	oe	
G.18	rd/be	K.13	01.10	rd/be	400 c/s sq w
I.28	bk	K.14	01.20	bk	0 V
I.33	scrd	K.15	01.24	scrd	RS3.S1 screen to K.14
I.34	scrd	K.16	01.22	scrd	RS3.R1
I.35	scrd	K.17	01.26	scrd	RS3.R4
PB.16	bk	K.18	03.06	bk	0 V
PG.08	bk	K.18	K.34	bk	0 V
G.21	gy	K.19	02.34	gy	Photocell output
PG.02	we	K.20	03.16	vt/we	+ 50 V No 1
TA.38	vt/we	K.20			+ 50 V No 1
PG.03	oe	K.21	03.22	gy	
PG.05	yw	K.22	03.24	gy	
PB.24	yw	K.23	03.26	gy	
PB.25	oe	K.24	03.28	gy	
PG.01	oe	K.25	03.32	gy	
PB.23	we	K.26	03.34	gy	
PI.03	oe	K.27	04.28	oe	
PI.01	oe	K.28	04.24	oe	
I.06	vt/we	K.29	05.22	vt/we	+ 50 V No 3
M.19	vt/we	K.29			
G.23	vt/we	K.30	06.24	vt/we	- 50 V No 4
I.07	vt/we	K.30			
TA.40	vt/we	K.31	04.06	vt/we	- 50 V No 2
PG.06	gn	K.32			
PB.22	gn	K.32			
PG.07	bn	K.33			
PB.21	bn	K.33			
PI.02	bk	K.34	K.18	bk	
VMI.E	bk	K.34	K.35	bk	0 V
TA.35	bk	K.35		bk	0 V

Table 7.1 SRS panel K. Plug K connections
(Plug card type DAF 1/2/7)

From	Colour	Terminal	To	Colour	Note
K.03	bk	01.02	02.30	bk	0 V
K.02	be	01.04	02.04	be	- 12 V
K.04	rd	01.08	02.32	rd	+ 6 V
K.13	rd/be	01.10			400 c/s
K.14	bk	01.20	05.08	bk	0 V
K.16	scrd	01.22			RS3.R1
K.15	scrd	01.24			RS3.S1
K.17	scrd	01.26			RS3.R4

Table 7.2 SRS panel K. Card No 1 connections
(Card type DAF 1/15)

From	Colour	Terminal	To	Colour	Note
01.04	be	02.04			- 12 V
01.02	bk	02.30			0 V
01.08	rd	02.32			+ 6 V
K.19	gy	02.34			Photocell

Table 7.3 SRS panel K. Card No 2 connections
(Card type DAF 1/16)

From	Colour	Terminal	To	Colour	Note
K. 09	oe	03. 02			50 VAC
K. 10	oe	03. 04			50 VAC
K. 18	bk	03. 06			0 V sep
K.		03. 06	04. 16	bk	0 V
K. 20	vt/we	03. 16			+ 50 V
K. 21	gy	03. 22			
K. 22	gy	03. 24			
K. 23	gy	03. 26			
K. 24	gy	03. 28			
K. 25	gy	03. 32			
K. 26	gy	03. 34			

Table 7. 4 SRS panel K. Card No 3 connections
(Card type DAF 11/12)

From	Colour	Terminal	To	Colour	Note
K. 11	oe	04. 02			50 VAC
K. 12	oe	04. 04			50 VAC
		04. 06	04. 22	vt/we	
K. 31	vt/we	04. 06			- 50 V
03. 06	bk	04. 16			0 V
K. 28	oe	04. 24			Paper drive
K. 27	oe	04. 28			Paper drive

Table 7. 5 SRS panel K. Card No 4 connections
(Card type DAF 11/12)

From	Colour	Terminal	To	Colour	Note
K. 05	gn	05. 02			120 VAC
K. 06	gn	05. 04			120 VAC
		05. 06	05. 16	gn	
01. 20	bk	05. 08			0 V
		05. 08	05. 14	bk	0 V
		05. 14	05. 24	bk	0 V
		05. 20	05. 22	vt/we	
K. 29	vt/we	05. 22			+ 50 V
		05. 24	06. 06	bk	

Table 7. 6 SRS panel K. Card No 5 connections
(Card type DAF 11/13)

From	Colour	Terminal	To	Colour	Note
K. 07	gn	06. 02			120 VAC
K. 08	gn	06. 04			
05. 24	bk	06. 06			0 V
		06. 06	06. 08	bk	0 V
		06. 14	06. 16	bk	0 V
		06. 20	06. 24	vt/we	
K. 30	vt/we	06. 24			- 50 V

Table 7. 7 SRS panel K. Card No 6 connections
(Card type DAF 11/13)

From	Colour	Terminal	To	Colour	Note
B. 02	gy	L. 02			
B. 03	oe	L. 03			
B. 04	gn	L. 04			
B. 05	gy	L. 05			
B. 06	oe	L. 06			
B. 07	rd/be	L. 07			
B. 08	we	L. 08			
B. 09	gn	L. 09			
B. 10	gy	L. 10			
B. 11	oe	L. 11			
B. 12	we	L. 12			
B. 13	gn	L. 13			
B. 14	oe	L. 14			
B. 15	gy	L. 15			
B. 16	gn	L. 16			
M. 17	bk	L. 17			0 V
M. 18	rd/be	L. 18			1 VAC
M. 19	vt/we	L. 19			+ 50 V
B. 21	gn	L. 21			
B. 22	gy	L. 22			
B. 23	we	L. 23			
B. 24	vt/we	L. 24			
B. 25	rd/be	L. 25			
B. 26	oe	L. 26			
B. 27	we	L. 27			
B. 28	rd/be	L. 28			
B. 29	oe	L. 29			
B. 30	gy	L. 30			
B. 31	gn	L. 31			
B. 32	vt/we	L. 32			
B. 33	oe	L. 33			
B. 34	rd/be	L. 34			
B. 35	gy	L. 35			

Table 8.1 SRS Indicator card L connections
(Card type DAF 15/16)

From	Colour	Terminal	To	Colour	Note
F. 10	rd/be	M. 07			
F. 09	vt/we	M. 08			
F. 08	we	M. 09			
F. 07	oe	M. 10			
F. 06	gn	M. 11			
F. 05	gy	M. 12			
F. 04	rd/be	M. 13			
F. 03	we	M. 14			
F. 02	gy	M. 15			
L. 17	bk	M. 17			0 V
I. 28	bk	M. 17			
L. 18	rd/be	M. 18			1 VAC
T1. 25	rd/be	M. 18			
L. 19	vt/we	M. 19			+ 50 V
K. 29	vt/we	M. 19			
T1. 24	bk	M. 20			0 V
D. 02	gy	M. 21			
D. 03	oe	M. 22			
D. 04	we	M. 23			
D. 05	rd/be	M. 24			
D. 06	vt/we	M. 25			
D. 07	gy	M. 26			
D. 08	oe	M. 27			
D. 09	we	M. 28			
D. 10	rd/be	M. 29			
D. 11	vt/we	M. 30			
D. 12	gy	M. 31			
D. 13	oe	M. 32			
D. 14	we	M. 33			
D. 15	rd/be	M. 34			
D. 16	vt/we	M. 35			

Table 8.2 SRS Indicator card M connections
(Card type DAF 15/16)

From	To	Colour	Note
PS1.01	PS2.01	spec	220 VAC
PS1.01	TA.03	spec	
PS1.02	PS2.02	spec	
PS1.02	TA.04	spec	
PS1.03	PS2.03		
PS1.04	PS1.05		
PS1.04	A1.01	be	
PS1.09	PS1.10		
PS1.10	K.03	bk	0 V panel K
PS1.10	FI1.03	bk	

Table 9.1a SRS power supply PS1 connections

From	To	Colour	Note
PS2.01	PS3.01	spec	220 VAC
PS2.02	PS3.02	spec	
PS2.03	PS3.03		
PS2.04	A2.01	be	
PS2.05	J.17	be	- 12 V sense
PS2.09	J.15	bk	0 V sense
PS2.10	PS3.10		
PS2.10	I.04	bk	
PS2.10	G.25	bk	
PS2.10	PH.25	bk	

Table 9.1b SRS power supply PS2 connections

From	To	Colour	Note
PS3.01	PS4.01	spec	220 VAC
PS3.02	PS4.02	spec	
PS3.03	PS4.03		
PS3.03	PS3.10		
PS3.04	A3.01	be	
PS3.05	PS3.04		
PS3.09	PS3.10		
PS3.10	PS4.04		
PS3.10	C.33	bk	

Table 9.1c SRS power supply PS3 connections

From	To	Colour	Note
PS4.04	PS4.05		
PS4.09	A4.02	rd	
PS4.10	A4.01	rd	

Table 9.1d SRS power supply PS4 connections

From	To	Colour	Note
A1.01	PS1.04	be	
A1.02	K.02	be	- 12 V panel K

Table 9.2a SRS amperemeter A1 connections

From	To	Colour	Note
A2.01	PS2.04	be	
A2.02	FI1.01	be	- 12 V
A2.02	PH.18	be	- 12 V
A2.02	G.24	be	- 12 V
A2.02	J.22	be	- 12 V

Table 9.2b SRS amperemeter A2 connections

From	To	Colour	Note
A3.01	PS3.04	be	
A3.02	C.32	be	

Table 9.2c SRS amperemeter A3 connections

From	To	Colour	Note
A4.01	PS4.10	rd	
A4.02	PS4.09	rd	
A4.02	PH.17	rd	
A4.02	C.34	rd	
A4.02	G.26	rd	
A4.02	I.05	rd	
A4.02	K.04	rd	

Table 9.2d SRS amperemeter A4 connections

From	To	Colour	Note
FI1.01	A2.02	be	
FI1.02	I.02	be	- 12 V pannel IJ
FI1.03	PS1.10	bk	

Table 9.3 SRS filter FI1 connections

From	To	Colour	Note
T1.01			0 V
T1.02	TA.03	spec	10 V
T1.03			20 V — Mains connections
T1.04	TA.04	spec	230 V
T1.05			250 V
T1.02	TA.07	spec	220 VAC to PS5
T1.04	TA.08	spec	
T1.06	TA.25	rd/be	115 VAC
T1.06	PI.11	rd/be	
T1.07	PI.12	rd/be	115 VAC
T1.07	TA.27	rd/be	
T1.08	K.05	gn	120 VAC No 1
T1.10	K.06	gn	
T1.12	K.07	gn	120 VAC No 2
T1.14	K.08	gn	
T1.16	K.09	oe	55 VAC No 1
T1.18	K.10	oe	
T1.20	K.11	oe	55 VAC No 2
T1.22	K.12	oe	
T1.24	M.20	bk	1.0 VAC
T1.25	M.18	rd/be	
T1.26	PH.21		6.3 VAC
T1.26	PF.22		
T1.27	PH.22		
T1.27	PI.06		
T1.28	J.34	oe	51 VAC
T1.30	J.35	oe.	

Table 9.4 SRS transformer T1 connections

From	To	Colour	Note
VM1.AC1	TA.05	spec	220 VAC
VM1.AC1	TA.06	spec	
VM1.02	PS1.05	be	- 12 V
VM1.03	PS2.05	be	- 12 V
VM1.04	PS3.05	be	- 12 V
VM1.06	PS4.09	rd	+ 6 V
VM1.07	TA.38	vt/we	+ 50 V No 1
VM1.08	K.31	vt/we	- 50 V No 2
VM1.09	I.06	vt/we	+ 50 V No 3
VM1.10	I.07	vt/we	- 50 V No 4
VM1.E	I.24	bk	
VM1.E	K.34	bk	

Table 9.5 SRS voltmeter VM1 connections

From	Colour	Terminal	To	Colour	Note
I. 30	scrd	PB. 01	RS2. R1	rd	
PB. 03		PB. 02	RS2. R3	bk	0 V
PB. 08		PB. 03	RS2. R2	yw	0 V
I. 31	scrd	PB. 04	RS2. R4	be	
I. 29	scrd	PB. 07	RS2. S1	rd	
I. 32	bk	PB. 08	RS2. S3	bk	0 V
		PB. 09	RS2. C3	gn	
		PB. 10	RS2. C1	bn	
		PB. 17	RS2. S4	be	
		PB. 18	RS2. S2	yw	
PB. 20		PB. 19	RS2. C4	we	
		PB. 20	RS2. C2	oe	
K. 18	bk	PB. 16	M1. A2	bk	
K. 33	bn	PB. 21	M1. F1	bn	
K. 32	gn	PB. 22	M1. F2	gn	
K. 24	oe	PB. 25	M1. A1	oe	
K. 26	we	PB. 23	CL1	we	
K. 23	yw	PB. 24	CL2	yw	

Table 9. 6a SRS plug PB connections

From	Colour	Terminal	To	Colour	Note
J. 25	rd/be	PE. 01	M2. X1	we	115 VAC
TA. 20	rd/gn	PE. 02	SF. S3	oe	
TA. 10	we/gn	PE. 04	SC. S1	be	
TA. 12	we/gn	PE. 05	SC. S2	rd	
J. 24	rd/be	PE. 06	M2. X2	yw	115 VAC
J. 06	scrd	PE. 09	SC. R1	scrd	U_c
TA. 14	we/gn	PE. 10	SC. S3	yw	
PE. 21		PE. 11	C_{M1} 50µ [1]	gn	
J. 07	scr	PE. 13		scr	scr for U_c
J. 02	bk	PE. 15	SC. R2	bk	0 V
PE. 22		PE. 16	C_{M1} 50µ [1]	gn	
J. 31	rd/be	PE. 17	M2. CT	rd/bk, gn	
J. 12	bk	PE. 19	SF. R2	bk	
TA. 18	rd/gn	PE. 20	SF. S2	bn	
J. 30	we	PE. 21	M2. C2	bk	
J. 32	we	PE. 22	M2. C1	rd	
J. 09	scr	PE. 23		scr	scr for U_f
TA. 16	rd/gn	PE. 24	SF. S1	gy	
J. 08	scrd	PE. 25	SF. R1	scrd	U_f

[1] C_{M1} = 50 µF is connected between PE. 11 - PE. 16

Table 9. 6b SRS plug PE connections

From	Colour	Terminal	To	Colour	Note
I. 26	scrd	PF. 01	RS1. R1	rd	
PF. 03		PF. 03	RS1. R3	bk	0 V
PF. 08		PF. 02	RS1. R2	yw	0 V
I. 27	scrd	PF. 04	RS1. R4	be	
I. 25	scrd	PF. 07	RS1. S1	rd	
I. 22	bk	PF. 08	RS1. S3	bk	0 V
		PF. 09	RS1. C3	gn	
		PF. 10	RS1. C1	bn	
		PF. 17	RS1. S4	be	
		PF. 18	RS1. S2	yw	
PF. 20		PF. 19	RS1. C4	we	
		PF. 20	RS1. C2	oe	
PI. 05	oe	PF. 21	P6. 02	oe	
T1. 26	oe	PF. 22	P6. 01	oe	6 VAC
		PF. 08	P7. 03	bk	0 V
J. 05	gy	PF. 23	P7. 02	gy	
J. 04	gy	PF. 24	P7. 01	gy	

Table 9. 6c SRS plug PF connections

From	Colour	Terminal	To	Colour	Note
K. 25	oe	PG. 01	SW10. 1		
K. 20	we	PG. 02	SW10. 2		
K. 21	oe	PG. 03	SW10. 3		
K. 22	yw	PG. 05	P1. 01		
		PG. 05	P2. 03		
K. 32	gn	PG. 06	P1. 02		
K. 33	bn	PG. 07	P2. 02		
K. 18	bk	PG. 08	P1. 03		0 V
		PG. 08	P2. 01		

Table 9. 6d SRS plug PG connections

From	Colour	Terminal	To	Colour	Note
I. 12	scrd	PH. 01	PJ. 10	rd/be	X1
I. 13	scrd	PH. 02	PJ. 11	rd/be	X2
I. 15	scrd	PH. 03	PJ. 08	rd/be	Y2
I. 14	scrd	PH. 04	PJ. 07	rd/be	Y1
I. 16	bk	PH. 05	PS5. 0	bk	0 V PS5
TA. 07	spec	PH. 06	PS5. 220 V	spec	220 VAC
TA. 17	vt/we	PH. 07	SW9. 1a	vt/we	IFF - chall
I. 03	be	PH. 08	P5. 01	be	- 12 V
G. 16	gy	PH. 09	PS5. G1 ~	gy	
I. 22	bk	PH. 10	P5. 03	bk	0 V
G. 13	vt/we	PH. 11	P1. 02	vt/we	
I. 18	we	PH. 12	SW9. 3b	we	
I. 17	we	PH. 13	P2. 02	we	
I. 20	gy	PH. 14	P5. 02	gy	
SW8. 01	gy	PH. 15	SW9. 1b	gy	
TA. 08	spec	PH. 16	PS5. 220 V	spec	220 VAC
A4. 02	rd	PH. 17	PK. 06	rd	+ 6 V
		PH. 17	PL. 05	rd	+ 6 V
A2. 02	be	PH. 18	PK. 09	be	- 12 V
		PH. 18	PL. 01	be	
TA. 21	vt/we	PH. 19	SW9. 3a	vt/we	
G. 14	rd/be	PH. 20	P1. 01	rd/be	
T1. 26	oe	PH. 21	P3. 01	oe	Scale ill
T1. 27	oe	PH. 22	Scale lamps	oe	6. 3 VAC
G. 15	we	PH. 23	P1. 03	we	
J. 03	we	PH. 24	PL. 02	we	Gating pulse DAF1
PS2. 10	bk	PH. 25	PK. 07	bk	0 V
		PH. 25	PL. 03	bk	0 V

Table 9. 6e SRS plug PH connections

From	Colour	Terminal	To	Colour	Note
K. 28	oe	PI. 01	M3. F1		
K. 34	bk	PI. 02	M3. F2		
PI. 04	bk	PI. 02			
K. 27	oe	PI. 03	M3. A2		
		PI. 04	M3. A1		
PF. 21	oe	PI. 05	Lamps		
T1. 27		PI. 06	Lamps		6 VAC
I. 21	gn	PI. 09	Helix		
I. 16	bk	PI. 10	Knife		0 V
T1. 06		PI. 11	M4. 01		115 VAC
T1. 07		PI. 12	M4. 02		

Table 9. 6f SRS plug PI connections

From	Colour	Terminal	To	Colour	Note
PS5. 6. 3~	oe	PJ. 01			
PS5. K	spec	PJ. 02			- 2500 V
PS5. G1=	spec	PJ. 03			
PS5. G3	spec	PJ. 05			
PH. 03	rd/be	PJ. 07			Y2
PH. 04	rd/be	PJ. 08			Y1
PS5. A1	spec	PJ. 09			
PH. 01	rd/be	PJ. 10			X1
PH. 02	rd/be	PJ. 11			X2
PS5. 6. 3~	oe	PJ. 14			
PS5. 0	bk	Screen			
PS5. A2	spec	Cap			+ 2500 V

Table 9. 6g SRS plug PJ connections

From	Colour	Terminal	To	Colour	Note
PH. 17	rd	PK. 06			+ 6 V
PH. 25	bk	PK. 07			0 V
SW9. 2b	gy	PK. 08			Ouput
PH. 18	be	PK. 09			- 12 V

Table 9. 6h SRS plug PK connections

From	Colour	Terminal	To	Colour	Note
PH. 18	be	PL. 01			- 12 V
PH. 24	we	PL. 02			Blanking pulse
PH. 25	bk	PL. 03			0 V
PH. 17	rd	PL. 05			+ 6 V

Table 9. 6i SRS plug PL connections

From	Colour	Terminal	To	Colour	Note
1306		PM			IF
1307		PN	IJ. 06. 30		Pretrig
1308		PO	IJ. 04. 28		IFF
		PQ	PR		
PQ		PR			Input DAF 1
		PS	PT		
PS		PT			Input DAF 2

Table 9. 6j SRS coaxial plug connections

From	To	Colour	Note
P1.01	PH.20	rd/be	
P1.02	PH.11	vt/we	
P1.03	PH.23	we	
P2.01	P5.01	be	- 12 V
P2.02	PH.13	we	
P3.03	PH.21	oe	
P3.02	Lamps	oe	
P5.01	PH.08	be	- 12 V
P5.02	PH.14	gy	
P5.03	PH.10	bk	0 V
P6.01	PF.22	oe	6 VAC
P6.02	PI.05	oe	
P7.01	PF.24	gy	
P7.02	PF.23	gy	
P7.03	PF.08	bk	0 V

Table 9.7 SRS potentiometer connections

From	To	Colour	Note
SW1.1a	Fuse 1	spec	
SW1.1b	Fuse 2	spec	
SW1.2a	TA.03	spec	
SW1.2b	TA.04	spec	

Table 9.8a SRS switch SW1 connections (MAINS)

From	To	Colour	Note
SW2.03a	A.16	rd/be	
SW2.05a	A.17	we	
SW2.07a	A.15	vt/we	
SW2.09a	A.18	gy	
SW2.13a	A.14	we	
SW2.16a	A.11	rd/be	
SW2.18a	A.12	oe	
SW2.20a	A.10	vt/we	
SW2.22a	A.13	gn	
SW2.26a	A.09	we	

Table 9.8b SRS switch SW2 connections (TEST GENERATOR)

From	To	Colour	Note
SW3.01a	A.29	oe	
SW3.08a	A.08	oe	
SW3.10a	A.30	rd/be	
SW3.17a	D.27	oe	
SW3.23a	A.24	gn	
SW3.26a	A.25	gy	
SW3.01b	A.26	bk	
SW3.05b	SW4.04a	bk	
SW3.08b	A.03	gy	
SW3.17b	A.02	rd/be	
SW3.12b	A.04	rd/be	
SW3.19a	F.17	rd/be	

Table 9.8c SRS switch SW3 connections (MODE)

From	To	Colour	Note
SW4.04a	SW3.05b	bk	0 V
SW4.13a	D.28	rd/be	
SW4.06b	C.21	we	
SW4.08b	C.22	rd/be	
SW4.10b	C.23	we	
SW4.12b	C.24	rd/be	
SW4.13b	Lamps[1]	be	
SW4.14b	C.25	we	
SW4.16b	C.26	rd/be	
SW4.18b	C.27	we	
SW4.20b	C.28	rd/be	
SW4.22b	C.29	we	
SW4.24b	C.30	rd/be	
SW4.26b	A.20	be	- 12 V

[1] - 12 V to WAIT - REPEAT lamps

Table 9.8d <u>SRS switch SW4 connections</u>

From	To	Colour	Note
SW7.12a	I.02	be	- 12 V
SW7.14a	I.24	bk	0 V
SW7.10a	G.19	gn	
SW7.17a	I.08	gn	
SW7.01a	G.20	gn	
SW7.08a	I.09	gn	
SW7.10b	H.21	oe	
SW7.17b	I.10	oe	
SW7.01b	H.22	oe	
SW7.08b	I.11	oe	
SW7.16a	SW8.08	bk	0 V
SW7.12a	SW8.26	be	- 12 V

Table 9.8e <u>SRS switch SW7 connections</u>

From	To	Colour	Note
SW8.01	PH.15	gy	
SW8.14a	J.27	gn	
SW8.26	SW7.12	be	- 12 V
SW8.13a	I.19	gy	
SW8.08	SW7.16a	bk	0 V
SW8.16a	J.28	gn	

Table 9.8f <u>SRS switch SW8 connections (SERVO)</u>

From	To	Colour	Note
SW9.1b	PH.15	gy	
SW9.2b	PK.08	gy	
SW9.3b	PH.12	we	
SW9.1a	PH.07	vt/we	} IFF - challenge
SW9.3a	PH.19	vt/we	} IFF - challenge

Table 9.8g <u>SRS switch SW9 connections (NORMAL - IFF)</u>

APPENDIX C

CENTRAL STROBE RECEIVING EQUIPMENT CSR-1

CABLING TABLES

Table 10.2	External cabling
" 10.3	Terminal board X
" 10.4	Terminal board Y
" 10.5	Terminal board VC
" 10.6	Coaxial plugs
" 11.1	Panel AB. Plug A
" 11.2	Panel AB. Plug B
" 11.3-11.31	Panel AB. Card No 1-29
" 12.1	Panel CD. Plug C
" 12.2	Panel CD. Plug D
" 12.3-12.29	Panel CD. Card No 1-27
" 13.1	Panel EF. Plug E
" 13.2	Panel EF. Plug F
" 13.3-13.21	Panel EF. Card No 1-19
" 14.1	Panel GH. Plug G
" 14.2	Panel GH. Plug H
" 14.3-14.24	Panel GH. Card No 1-22
" 15.1	Panel IJ. Plug I
" 15.2	Panel IJ. Plug J
" 15.3-15.20	Panel IJ. Card No 1-18
" 16.1	Panel KL. Plug K
" 16.2	Panel KL. Plug L
" 16.3-16.24	Panel KL. Card No 1-22
" 17.1	Panel MN. Plug M
" 17.2	Panel MN. Plug N
" 17.3-17.20	Panel MN. Card No 1-18
" 18.1	Panel OP. Plug O
" 18.2	Panel OP. Plug P
" 18.3-18.24	Panel OP. Card No 1-22
" 19.1	Panel QR. Plug Q
" 19.2	Panel QR. Plug R
" 19.3-19.20	Panel QR. Card No 1-18
" 20.1	Panel ST. Plug S
" 20.2	Panel ST. Plug T
" 20.3-20.24	Panel ST. Card No 1-22
" 21	Indicator card plug U
" 22.1	Power supplies
" 22.2	Amperemeters A1-A7
" 22.3	Voltmeter VM1
" 22.4	Transformer T1
" 22.5	Oven plug ON
" 22.6	Strobe erasure panel
" 22.7	TTY Tx plug W
" 22.8	Switches

Table 10.1 CSR cabling tables

From	Cable No	To	Colour	Note
VA. 1	1302. 6a	X. 31	be	W1 stn A
VA. 2	" 6b	X. 32	gy	W2 stn A
VA. 3	" 7a	X. 33	gn	W3 stn A
VA. 4	" 7b	X. 34	bk	W4 stn A
VA. 5	" 8a	X. 35	oe	W5 stn A
VA. 6	" 8b	X. 36	be	W6 stn A
VA. 7	" 9a	X. 37	bk	W7 stn A
VA. 8	" 9b	X. 38	be	W8 stn A
VA. 9	" 10a	X. 39	be	W9 stn A
VA. 10	" 10b	X. 40	bn	W10 stn A
VA. 11	" 1a	X. 21	be	W1 stn B
VA. 12	" 1b	X. 22	we	W2 stn B
VA. 13	" 2a	X. 23	gn	W3 stn B
VA. 14	" 2b	X. 24	oe	W4 stn B
VA. 15	" 3a	X. 25	bk	W5 stn B
VA. 16	" 3b	X. 26	bn	W6 stn B
VA. 17	" 4a	X. 27	oe	W7 stn B
VA. 18	" 4b	X. 28	we	W8 stn B
VA. 19	" 5a	X. 29	be	W9 stn B
VA. 20	" 5b	X. 30	gn	W10 stn B
	"	X. 0	screen	gnd. conn.
VA. 21	1301. 6a	X. 11	be	W1 stn C
VA. 22	" 6b	X. 12	gy	W2 stn C
VA. 23	" 7a	X. 13	gn	W3 stn C
VA. 24	" 7b	X. 14	bk	W4 stn C
VA. 25	" 8a	X. 15	oe	W5 stn C
VA. 26	" 8b	X. 16	be	W6 stn C
VA. 27	" 9a	X. 17	bk	W7 stn C
VA. 28	" 9b	X. 18	oe	W8 stn C
VA. 29	" 10a	X. 19	be	W9 stn C
VA. 30	" 10b	X. 20	bn	W10 stn C
VA. 31	" 1a	X. 01	be	W1 stn D
VA. 32	" 1b	X. 02	we	W2 stn D
VA. 33	" 2a	X. 03	gn	W3 stn D
VA. 34	" 2b	X. 04	oe	W4 stn D
VA. 35	" 3a	X. 05	bk	W5 stn D
VA. 36	" 3b	X. 06	bn	W6 stn D
VA. 37	" 4a	X. 07	oe	W7 stn D
VA. 38	" 4b	X. 08	we	W8 stn D
VA. 39	" 5a	X. 09	be	W9 stn D
VA. 40	" 5b	X. 10	gn	W10 stn D

Table 10. 2a CSR external cable 1301 and 1302 connections (Strobe erasure panel)

From	Cable No	To	Colour	Note
SRS/TA. 36	1303. 1a	Y. 15	bn	} TTY from stn A
SRS/TA. 37	" 1b	Y. 16	be	
SRS/TA. 35	" 2a	Y. 40	be	
SRS/TA. 31	" 2b	Y. 36	oe	
	" 3a	Y. 09	be	
	" 3b	Y. 10	bk	
	" 4a	Y. 13	bk	
	" 4b	Y. 14	gy	
	" 5a	Y. 12	bk	
	" 5b	Y. 11	oe	
	1304. 1a	Y. 40	gy	
	" 1b	Y. 36	bk	
	" 2a	Y. 39	gy	
	" 2b	Y. 38	gn	
FFSB	" 3a	Y. 35	gy	} TTY from stn B
FFSB	" 3b	Y. 31	bn	
	" 4a	Y. 34	gy	
	" 4b	Y. 33	we	
FFSB	" 5a	Y. 30	gy	} TTY from stn C
FFSB	" 5b	Y. 26	be	
	" 6a	Y. 29	gy	
	" 6b	Y. 28	oe	
FFSB	" 7a	Y. 25	be	} TTY from stn D
FFSB	" 7b	Y. 21	we	
	" 8a	Y. 24	be	
	" 8b	Y. 23	gn	
	" 9a	Y. 08	be	
	" 9b	Y. 07	oe	
	" 10a	Y. 06	be	
	" 10b	Y. 05	bk	
	" 11a	Y. 04	be	
	" 11b	Y. 03	bn	
	" 12a	Y. 02	bn	
	" 12b	Y. 01	we	

Table 10. 2b CSR external cable 1303 and 1304 connections (Teletype signals)

From	Cable No	To	Colour	Note
P2. 106. 26	1305	VC. 01	we	} 220 VAC to
P2. 106. 26	"	VC. 02	bk	CSR
	"	VC. gnd	screen	gnd
TTY Tx/W. 1	1311	Y. 17	be	- 12 V to TTY Tx
TTY Tx/W. 3	"	Y. 18	bk	0 V to TTY Tx
TTY Tx/W. 4	"	Y. 19	yw	Photocell output
TTY Tx/W. 2	"	Y. 20	we	TTY sig
TTY Tx/W. 8	1312	VC. 03	bn	} 220 VAC to
TTY Tx/W. 7	"	VC. 04	bn	TTY Tx
TTY Tx/W. 6	"	VC. gnd		
	1316	VB. 05	we	} 220 VAC to
	"	VB. 06	bk	SEP
8GE1751/PS26. A	1203-1	Z4	coax	cos φ
8GE1751/PS26. C	1203-2	Z5	"	sin φ
8GE1751/PS26. E	1203-3	Z6	"	Y_o
8GE1751/PS26. G	1203-4	Z7	"	X_o
8GE1751/PS26. J	1203-5	Z8	"	Blank strobe
8GE1751/PS26. L	1203-6	Z9	"	Blank origin
8GE1751/PS26. I	1203-7	Z10	"	Stop line
8GE1751/PS25	1204	Z11	"	Sync
8GE1751/PS27	1205	Z12	"	Stop sweep
8GE1751/PS28	1206	Z13	"	40 n m markers
8GE750/PS104	1207	Z14	"	15. 347 V ref

Table 10. 2c CSR external cable connections

From	Colour	Terminal	Colour	To	Colour	Further connection	Note
1301. 1a	be	X. 01	gy	T. 02	gy	ST . 17. 17	Rx D
1301. 1b	we	X. 02	oe	T. 03	oe	ST . 17. 34	Rx D
1301. 2a	gn	X. 03	we	T. 04	we	ST . 18. 17	Rx D
1301. 2b	oe	X. 04	rd/be	T. 05	rd/be	ST . 18. 34	Rx D
1301. 3a	bk	X. 05	vt/we	T. 06	vt/we	ST . 19. 17	Rx D
1301. 3b	bn	X. 06	gy	T. 07	gy	ST . 19. 34	Rx D
1301. 4a	oe	X. 07	oe	T. 08	oe	ST . 20. 17	Rx D
1301. 4b	we	X. 08	we	T. 09	we	ST . 20. 34	Rx D
1301. 5a	be	X. 09	rd/be	T. 10	rd/be	ST . 21. 17	Rx D
1301. 5b	gn	X. 10	vt/we	T. 11	vt/we	ST . 21. 34	Rx D
1301. 6a	be	X. 11	gy	P. 02	gy	OP. 17. 17	Rx C
1301. 6b	gy	X. 12	oe	P. 03	oe	OP. 17. 34	Rx C
1301. 7a	gn	X. 13	we	P. 04	we	OP. 18. 17	Rx C
1301. 7b	bk	X. 14	rd/be	P. 05	rd/be	OP. 18. 34	Rx C
1301. 8a	oe	X. 15	vt/we	P. 06	vt/we	OP. 19. 17	Rx C
1301. 8b	be	X. 16	gy	P. 07	gy	OP. 19. 34	Rx C
1301. 9a	bk	X. 17	oe	P. 08	oe	OP. 20. 17	Rx C
1301. 9b	oe	X. 18	we	P. 09	we	OP. 20. 34	Rx C
1301. 10a	be	X. 19	rd/be	P. 10	rd/be	OP. 21. 17	Rx C
1301. 10b	bn	X. 20	vt/we	P. 11	vt/we	OP. 21. 34	Rx C
1302. 1a	be	X. 21	gy	L. 02	gy	KL. 17. 17	Rx B
1302. 1b	we	X. 22	oe	L. 03	oe	KL. 17. 34	Rx B
1302. 2a	gn	X. 23	we	L. 04	we	KL. 18. 17	Rx B
1302. 2b	oe	X. 24	rd/be	L. 05	rd/be	KL. 18. 34	Rx B
1302. 3a	bk	X. 25	vt/we	L. 06	vt/we	KL. 19. 17	Rx B
1302. 3b	bn	X. 26	gy	L. 07	gy	KL. 19. 34	Rx B
1302. 4a	oe	X. 27	oe	L. 08	oe	KL. 20. 17	Rx B
1302. 4b	we	X. 28	we	L. 09	we	KL. 20. 34	Rx B
1302. 5a	be	X. 29	rd/be	L. 10	rd/be	KL. 21. 17	Rx B
1302. 5b	gn	X. 30	vt/we	L. 11	vt/we	KL. 21. 34	Rx B
1302. 6a	be	X. 31	gy	H. 02	gy	GH. 17. 17	Rx A
1302. 6b	gy	X. 32	oe	H. 03	oe	GH. 17. 34	Rx A
1302. 7a	gn	X. 33	we	H. 04	we	GH. 18. 17	Rx A
1302. 7b	bk	X. 34	rd/be	H. 05	rd/be	GH. 18. 34	Rx A
1302. 8a	oe	X. 35	vt/we	H. 06	vt/we	GH. 19. 17	Rx A
1302. 8b	be	X. 36	gy	H. 07	gy	GH. 19. 34	Rx A
1302. 9a	bk	X. 37	oe	H. 08	oe	GH. 20. 17	Rx A
1302. 9b	oe	X. 38	we	H. 09	we	GH. 20. 34	Rx A
1302. 10a	be	X. 39	rd/be	H. 10	rd/be	GH. 21. 17	Rx A
1302. 10b	bn	X. 40	vt/we	H. 11	vt/we	GH. 21. 34	Rx A

Table 10. 3 CSR terminal board X connections

From	Colour	Terminal	Colour	To	Colour	Further connection	Note
1304.12b	we	Y.01					
1304.12a	bn	Y.02					
1304.11b	bn	Y.03					
1304.11a	be	Y.04					
1304.10b	bk	Y.05					
1304.10a	be	Y.06					
1304.9b	oe	Y.07					
1304.9a	be	Y.08					
1303.3a	be	Y.09					
1303.3b	bk	Y.10					
1303.5b	oe	Y.11					
1303.5a	bk	Y.12					
1303.4a	bk	Y.13					
1303.4b	gy	Y.14					
1303.1a	bn	Y.15					
1303.1b	be	Y.16	vt/we				
1311	be	Y.17	be				
1311	bk	Y.18	bk				
1311	yw	Y.19	we	D.30	we	CD.26.02	
1311	we	Y.20	gy	D.29	gy	CD.26.16	
1304.7b	we	Y.21	gy	T.32	gy	ST.22.28	Rx D
		Y.22	gn	T.31	gn	ST.22.10	Rx D
1304.8b	gn	Y.23	vt/we	T.30	vt/we	ST.22.08	Rx D
1304.8a	be	Y.24	rd/be	T.29	rd/be	ST.22.06	Rx D
1304.7a	be	Y.25	oe	T.33	oe	ST.22.26	Rx D
1304.5b	be	Y.26	gy	P.32	gy	OP.22.28	Rx C
		Y.27	gn	P.31	gn	OP.22.10	Rx C
1304.6b	oe	Y.28	vt/we	P.30	vt/we	OP.22.08	Rx C
1304.6a	gy	Y.29	rd/be	P.29	rd/be	OP.22.06	Rx C
1304.5a	gy	Y.30	oe	P.33	oe	OP.22.26	Rx C
1304.3b	bn	Y.31	gy	L.32	gy	KL.22.28	Rx B
		Y.32	gn	L.31	gn	KL.22.10	Rx B
1304.4b	we	Y.33	vt/we	L.30	vt/we	KL.22.08	Rx B
1304.4a	gy	Y.34	rd/be	L.29	rd/be	KL.22.06	Rx B
1304.3a	gy	Y.35	oe	L.33	oe	KL.22.26	Rx B
1303.2b	oe	Y.36	gy	H.32	gy	GH.22.28	Rx A
		Y.37	gn	H.31	gn	GH.22.10	Rx A
1304.2b	gn	Y.38	vt/we	H.30	vt/we	GH.22.08	Rx A
1304.2a	gy	Y.39	rd/be	H.29	rd/be	GH.22.06	Rx A
1303.2a	be	Y.40	oe	H.33	oe	GH.22.26	Rx A

Table 10.4 CSR terminal board Y connections

From	Colour	Terminal	To	Colour	Note
1305	we	VC. 01	SW13. 1a		
1305	bk	VC. 02	SW13. 1b		
		VC. 01	1305	we	220 VAC
		VC. 02	1305	bk	to SEP
Fuse 1	bk	VC. 03	1312	bn	220 VAC
Fuse 2	bk	VC. 04	1312	bn	to TTY Tx
		VC. 03	PS7. 01	bk	
		VC. 04	PS7. 02	bk	
VC. 03	bn	VC. 05	PS4. 01	bk	
VC. 04	bn	VC. 06	PS4. 02	bk	
VC. 05	bn	VC. 07	T1. 07	rd/yw	220 VAC
VC. 06	bn	VC. 09	T1. 08	rd/yw	to T1

Table 10. 5 CSR terminal board VC connections

From	Terminal	Colour	To	Colour	Further connection	Note
1203-1	Z. 04	gn	B. 30	oe	AB. 29. 34	cos φ
1203-2	Z. 05	oe	B. 31	gn	AB. 28. 34	sin φ
1203-3	Z. 06	we	B. 35	oe	AB. 13. 35	Y_o
1203-4	Z. 07	gy	B. 34	we	AB. 13. 34	X_o
1203-5	Z. 08	rd/be	B. 32	vt/we	AB. 11. 28	Blank strobe
1203-6	Z. 09	vt/we	B. 33	gn	AB. 14. 30	Blank origin
1203-7	Z. 10	rd/be	B. 23	rd/be	AB. 13. 24	Stop line
1204	Z. 11	gn	B. 26	gn	AB. 13. 30	Sync sweep
1205	Z. 12					Stop sweep
1206	Z. 13	vt/we	A. 24	vt/we	AB. 13. 26	40 nm markers
1207	Z. 14	rd/be	A. 35	we	AB. 13. 04	15. 347 V ref

Table 10. 6 CSR coaxial plug connections

From	Colour	Terminal	To	Colour	Note
D. 25	gn	A. 02	06. 31	gn	P6
D. 26	gy	A. 03	06. 32	gy	G
D. 27	vt/we	A. 04	06. 33	vt/we	H
D. 24	we	A. 05	10. 26	we	GHP6
C. 20	we	A. 06	16. 14	vt/we	X_1
C. 21	oe	A. 07	16. 09	rd/be	X_2
C. 22	gy	A. 08	16. 31	oe	X_3
C. 23	gn	A. 09	16. 26	we	X_4
C. 24	rd/be	A. 10	17. 14	rd/be	X_5
C. 25	we	A. 11	17. 09	oe	X_6
C. 26	gn	A. 12	17. 31	we	X_7
C. 27	oe	A. 13	17. 26	gn	X_8
SW9. 02	gn	A. 14	22. 28	we	
SW10. 01	rd/be	A. 15	27. 33	oe	
SW10. 02	gn	A. 16	27. 31	we	
C. 15	rd/be	A. 17	16. 13	oe	P4P8
C. 14	gn	A. 18	16. 17	gn	P4P7
D. 22	gy	A. 19	20. 06	we	P6
C. 12	vt/we	A. 20	15. 14	rd/be	
SW4. 17b	vt/we	A. 20			
SW9. 01	gy	A. 21	11. 31	oe	
C. 11	rd/be	A. 22	11. 12	vt/we	
Z. 10	rd/be	A. 23	13. 24	rd/be	Stop line
Z. 13	vt/we	A. 24	13. 26	vt/we	40 n m marker
D. 35	gy	A. 25	27. 30	gy	Shift
Z. 11	gn	A. 26	13. 30	gn	Sync sweep
ON. 04	oe	A. 27	29. 20	oe	+ 18 V
ON. 02	gy	A. 28	29. 32	gy	- 18 V
gnd	bk	A. 29			
C. 33	bk	A. 29	29. 22	bk	0 V
A5. 02	rd	A. 30			+ 6 V
C. 34	rd	A. 30	27. 06	rd	+ 6 V
A1. 02q	be	A. 31			- 12 V
C. 32	be	A. 31	27. 05	be	- 12 V
A7. 02	rd/be	A. 32	29. 28	rd/be	- 24 V
A6. 02	vt/we	A. 33	29. 02	vt/we	+ 24 V
ON. 05	rd/be	A. 34	13. 04	we	- 1 V
Z. 14	we	A. 35	13. 02	rd/be	15. 347 V ref

Table 11. 1 CSR panel AB. Plug A connections
(Plug card type DAF 1/2/16)

From	Colour	Terminal	To	Colour	Note
H. 17	gy	B. 02	07. 12	gn	Read W1
SW2. 17	gy	B. 02			
H. 18	vt/we	B. 03	07. 13	gy	Read W2
SW2. 19	vt/we	B. 03			
H. 19	rd/be	B. 04	07. 14	vt/we	Read W3
SW2. 21	rd/be	B. 04			
H. 20	oe	B. 05	07. 15	rd/be	Read W4
SW2. 23	oe	B. 05			
H. 21	we	B. 06	07. 16	oe	Read W5
SW2. 25	we	B. 06			
H. 22	gn	B. 07	07. 17	we	Read W6
SW2. 1	gn	B. 07			
H. 23	gy	B. 08	07. 18	gn	Read W7
SW2. 03	gy	B. 08			
H. 24	vt/we	B. 09	07. 19	gy	Read W8
SW2. 05	vt/we	B. 09			
H. 25	rd/be	B. 10	07. 20	vt/we	Read W9
SW2. 07	rd/be	B. 10			
H. 26	we	B. 11	07. 21	rd/be	Read W10
SW2. 09	we	B. 11			
SW1. 03b	oe	B. 12	09. 05	gy	Stn A
SW1. 16b	gn	B. 13	09. 20	oe	Stn B
SW1. 03c	gy	B. 14	10. 05	gy	Stn C
SW1. 16c	we	B. 15	10. 20	rd/be	Stn D
C. 16	we	B. 16	14. 24	rd/be	$\overline{S+}$
C. 17	vt/we	B. 17	14. 23	gy	$\overline{S-}$
C. 18	gy	B. 18	14. 25	we	$\overline{C+}$
C. 19	oe	B. 19	14. 26	gy	$\overline{C-}$
C. 13	rd/be	B. 20	27. 17	gy	P1
U. 16	gn	B. 21	16. 06	gn	$\overline{S1}$
U. 15	we	B. 22	16. 07	we	$\overline{S2}$
U. 14	vt/we	B. 23	16. 23	vt/we	$\overline{S3}$
U. 13	we	B. 24	16. 24	we	$\overline{S4}$
U. 12	rd/be	B. 25	17. 06	rd/be	$\overline{S5}$
U. 21	we	B. 26	17. 07	we	$\overline{S6}$
U. 22	rd/be	B. 27	17. 23	rd/be	$\overline{S7}$
U. 23	we	B. 28	17. 24	we	$\overline{S8}$
SW1. 13a	gn	B. 29	01. 16	gn	Inhibit S
Z. 04	gn	B. 30	29. 34	oe	Cosine
Z. 05	oe	B. 31	28. 34	gn	Sine
Z. 08	rd/be	B. 32	11. 28	vt/we	Blank strobe
Z. 09	vt/we	B. 33	14. 30	gn	Blank origin
Z. 07	gy	B. 34	13. 34	we	X shift
Z. 06	we	B. 35	13. 35	oe	Y shift

Table 11. 2 CSR panel AB. Plug B connections
(Plug card type DAF 1/3/4)

From	Colour	Terminal	To	Colour	Note
		01.04	02.04	be	-12 V
		01.06	02.02	rd	+ 6 V
		01.08	02.10	we	
		01.09	01.32	vt/we	
		01.09	02.24	gy	
		01.10	01.28	gn	
		01.11	02.22	gn	
		01.13	01.12	gy	
		01.15	02.08	oe	
B.29	gn	01.16	02.16	gn	Inhibit S
		01.18	02.18	bk	0 V
		01.20	01.24	rd/be	
		01.21	03.10	we	
		01.23	03.08	oe	
		01.26	03.06	rd/be	
01.10	gn	01.28	03.32	gy	
		01.30	02.26	we	

Table 11.3 CSR panel AB. Card No 1 connections
(Card type DAF 2/14)

From	Colour	Terminal	To	Colour	Note
01.06	rd	02.02	03.02	rd	+ 6 V
01.04	be	02.04	03.04	be	-12 V
		02.06	07.24	vt/we	
01.15	oe	02.08			
01.08	we	02.10			
		02.12	04.12	we	
		02.14	04.09	vt/we	A
01.16	gn	02.16	04.11	oe	S
01.18	bk	02.18	03.18	bk	0 V
01.11	gn	02.22			
01.09	gy	02.24			
01.30	we	02.26			
		02.28	04.14	gy	C
		02.30	04.08	rd/be	
		02.32	04.13	gn	B

Table 11.4 CSR panel AB. Card No 2 connections
(Card type DAF 3/10)

From	Colour	Terminal	To	Colour	Note
02.02	rd	03.02	07.23	rd	+ 6 V
02.04	be	03.04	04.02	be	-12 V
01.26	rd/be	03.06			
01.23	oe	03.08			
01.21	we	03.10			
		03.12	04.06	rd/be	
		03.14	04.15	we	
		03.16	04.07	vt/we	
02.18	bk	03.18	07.22	bk	0 V
		03.22	04.03	oe	
		03.24	07.21	gn	R10
		03.28	08.16	rd/be	
		03.30	03.26	gy	
01.28	gy	03.32			

Table 11.5 CSR panel AB. Card No 3 connections (Card type DAF 3/10)

From	Colour	Terminal	To	Colour	Note
03.04	be	04.02	05.02	be	-12 V
03.22	oe	04.03			
		04.04	07.02	gn	
		04.05	07.03	gn	
03.12	rd/be	04.06	04.25	oe	
03.16	vt/we	04.07	05.07	vt/we	
02.30	rd/be	04.08	05.08	gy	
02.14	vt/we	04.09	04.17	vt/we	
02.16	oe	04.11	04.16	gy	
02.12	we	04.12	04.26	rd/be	
02.32	gn	04.13	04.18	rd/be	
02.28	gy	04.14	04.19	oe	
03.14	we	04.15	04.20	we	
04.11	gy	04.16	04.30	vt/we	
04.09	vt/we	04.17	04.28	vt/we	
04.13	rd/be	04.18	05.18	we	
04.14	oe	04.19	06.14	gy	
04.15	we	04.20	05.06	rd/be	
		04.21	04.24	gy	
		04.21	07.04	we	
		04.22	04.34	gn	
		04.22	07.05	oe	
		04.23	09.08	oe	
04.06	oe	04.25	04.27	rd/be	
04.21	gy	04.24			
04.12	rd/be	04.26	05.09	gn	
04.25	rd/be	04.27			
04.17	vt/we	04.28	05.12	oe	
		04.29	05.10	we	
04.16	vt/we	04.30	04.29	gy	
		04.32	05.30	gn	
		04.32	08.15	vt/we	
		04.33	08.11	rd/be	
		04.33	05.25	rd/be	
04.22	gn	04.34			

Table 11.6 CSR panel AB. Card No 4 connections (Card type DAF 3/9)

From	Colour	Terminal	To	Colour	Note
04.02	be	05.02	06.02	be	-12 V
		05.03	07.06	gy	
		05.04	07.07	gn	
		05.05	07.08	we	
04.20	rd/be	05.06	05.15	we	
04.07	vt/we	05.07	05.14	oe	
04.08	gy	05.08	05.13	rd/be	
04.26	gn	05.09	05.17	vt/we	
04.29	we	05.10	05.11	vt/we	
05.10	vt/we	05.11	05.16	gy	
04.28	oe	05.12	06.09	gy	
05.08	rd/be	05.13	06.13	gn	
05.07	oe	05.14	05.19	rd/be	
05.06	we	05.15	05.20	oe	
05.11	gy	05.16	06.10	gn	
05.09	vt/we	05.17	06.12	we	
04.18	we	05.18	06.08	vt/we	
05.14	rd/be	05.19	06.07	rd/be	
05.15	oe	05.20	06.06	oe	
		05.21	09.24	oe	
		05.22	05.34	gy	
		05.23	10.24	we	
		05.24	05.35	we	
04.33	rd/be	05.25			
		05.26	05.32	rd/be	
		05.27	08.23	gn	
		05.27	06.27	gy	
		05.28	06.26	vt/we	
		05.28	08.30	we	
		05.29	20.06	vt/we	P6
		05.29	06.29	gn	
04.32	gn	05.30			
		05.31	05.33	oe	
		05.31	08.09	gy	
05.26	rd/be	05.32			
05.31	oe	05.33			
05.22	gy	05.34	09.10	gy	
05.24	we	05.35	10.08	vt/we	

Table 11.7 CSR panel AB. Card No 5 connections
(Card type DAF 3/9)

From	Colour	Terminal	To	Colour	Note
05.02	be	06.02	07.35	be	-12 V
		06.03	07.09	gy	
		06.04	07.10	oe	
		06.05	07.11	oe	
05.20	oe	06.06	06.15	rd/be	
05.19	rd/be	06.07			
05.18	vt/we	06.08			
05.12	gy	06.09	06.17	gn	
05.16	gn	06.10	06.11	vt/we	
		06.11	06.16	we	
05.17	we	06.12			
05.13	gn	06.13	06.18	gy	
04.19	gy	06.14	06.19	vt/we	
06.06	rd/be	06.15	06.20	rd/be	
		06.21	06.24	vt/we	
		06.21	10.10	we	
		06.22	06.34	we	
		06.23	11.06	we	
		06.25	08.21	oe	
		06.25	06.33	oe	
05.28	vt/we	06.26			
05.27	gy	06.27			
		06.28	08.20	gn	
		06.28	06.32	rd/be	
05.29	gn	06.29	06.31	rd/be	
A.02	gn	06.31			
A.03	gy	06.32			
A.04	vt/we	06.33			
		06.34	09.26	gy	

Table 11.8 CSR panel AB. Card No 6 connections
(Card type DAF 3/9)

From	Colour	Terminal	To	Colour	Note
04 04	gn	07.02			
04.05		07.03			
04.21	we	07.04			
04.22	oe	07.05			
05.03	gy	07.06			
05.04	gn	07.07			
05.05	we	07.08			
06.03	gy	07.09			
06.04	oe	07.10			
06.05	oe	07.11			
B.02	gn	07.12			R1
B.03	gy	07.13	11.08	oe	R2
B.04	vt/we	07.14			R3
B.05	rd/be	07.15			R4
B.06	oe	07.16			R5
B.07	we	07.17			R6
B.08	gn	07.18			R7
B.09	gy	07.19			R8
B.10	vt/we	07.20			R9
B.11	rd/be	07.21			
03.24	gn	07.21			
03.18	bk	07.22	08.18	bk	0 V
03.02	rd	07.23	08.06	rd	+ 6 V
02.06	vt/we	07.24			
		07.30	13.29	we	
		07.32	13.25	gn	
06.02	be	07.35	08.02	be	-12 V

Table 11.9 CSR panel AB. Card No 7 connections
(Card type DAF 3/14)

From	Colour	Terminal	To	Colour	Note
07.35	be	08.02	09.04	be	-12 V
07.23	rd	08.06	09.02	rd	+ 6 V
05.31	gy	08.09			
04.33	rd/be	08.11			
05.26	vt/we	08.13	08.12	gy	
		08.14	08.10	rd/be	Reset
		08.14	11.16	oe	
04.32	vt/we	08.15			
03.28	rd/be	08.16			
07.22	bk	08.18	09.18	bk	0 V
06.28	gn	08.20	08.24	vt/we	
06.25	oe	08.21			
05.27	gn	08.23			
05.28	we	08.30			
		08.32	11.14	we	

Table 11.10 CSR panel AB. Card No 8 connections (Card type DAF 2/14)

From	Colour	Terminal	To	Colour	Note
08.06	rd	09.02	10.02	rd	+ 6 V
08.02	be	09.04	10.04	be	-12 V
B.12	gy	09.05			
04.23	oe	09.08			
05.34	gy	09.10			
		09.12	12.14	vt/we	
		09.14	09.06	gn	
08.18	bk	09.18	10.18	bk	0 V
B.13	oe	09.20			
05.21	oe	09.24			
06.34	gy	09.26			
		09.28	12.06	we	
		09.30	09.22	rd/be	

Table 11.11 CSR panel AB. Card No 9 connections (Card type DAF 3/10)

From	Colour	Terminal	To	Colour	Note
09.02	rd	10.02	11.02	rd	+ 6 V
09.04	be	10.04	11.03	be	-12 V
B.14	gy	10.05			
05.35	vt/we	10.08			
06.21	we	10.10			
		10.12	12.30	oe	
		10.14	10.06	gn	
09.18	bk	10.18	11.18	bk	0 V
B.15	rd/be	10.20			
05.23	we	10.24			
A.05	we	10.26			
		10.28	12.22	gn	
		10.30	10.22	vt/we	

Table 11.12 CSR panel AB. Card No 10 connections (Card type DAF 3/10)

From	Colour	Terminal	To	Colour	Note
10.02	rd	11.02	14.03	rd	+ 6 V
10.04	be	11.03	13.21	be	-12 V
06.23	we	11.06			
07.13	oe	11.08	14.22	oe	R2
		11.10	13.23	gy	
A.22	vt/we	11.12	11.22	rd/be	
08.32	we	11.14			
08.14	oe	11.16			
10.18	bk	11.18	13.31	bk	0 V
		11.26	15.21	gy	
B.32	vt/we	11.28			Blank strobe
A.21	oe	11.31			
		11.32	11.35	bk	

Table 11.13 CSR panel AB. Card No 11 connections
(Card type DAF 2/16)

From	Colour	Terminal	To	Colour	Note
		12.02	13.33	vt/we	+24 V
		12.03	13.32	rd/be	-24 V
		12.04	13.08	oe	
09.28	we	12.06	12.16	oe	
		12.10	13.09	rd/be	
		12.12	13.05	vt/we	
09.12	vt/we	12.14	12.24	rd/be	
		12.18	13 06	gy	
		12.20	13.15	vt/we	
10.28	gn	12.22	12.32	gn	
		12.26	13.17	gy	
		12.28	13.11	gn	
10.12	oe	12.30	12.08	we	
		12.34	13.13	we	

Table 11.14 CSR panel AB. Card No 12 connections
(Card type DAF 4/8)

From	Colour	Terminal	To	Colour	Note
A. 35	rd/be	13. 02			15. 347 V ref
A. 34	we	13. 04	13. 07	rd/be	-1 V
12. 12	vt/we	13. 05			
12. 18	gy	13. 06			
		13. 07	13. 12	we	
12. 04	oe	13. 08			
12. 10	rd/be	13. 09			
		13. 10	13. 14	gn	
		13. 10	27. 19	bk	
12. 28	gn	13. 11			
12. 34	we	13. 13			
		13. 14	13. 16	gy	
12. 20	vt/we	13. 15			
		13. 16	13. 18	vt/we	
12. 26	gy	13. 17			
		13. 18	13. 19	rd/be	
11. 03	be	13. 21	14. 02	be	-12 V
11. 10	gy	13. 23			
A. 23	rd/be	13. 24			Stop line
07. 32	gn	13. 25			
A. 24	vt/we	13. 26			40 nm
07. 30	we	13. 29			
A. 26	gn	13. 30			Sync sweep
11. 18	bk	13. 31	14. 13	bk	0 V
12. 03	rd/be	13. 32	28. 28	vt/we	-24 V
12. 02	vt/we	13. 33	28. 02	rd/be	+24 V
B. 34	we	13. 34			X coord
B. 35	oe	13. 35			Y coord

Table 11. 15 CSR panel AB. Card No 13 connections (Card type DAF 4/7)

From	Colour	Terminal	To	Colour	Note
13. 21	be	14. 02	15. 02	be	-12 V
11. 02	rd	14. 03	15. 06	rd	+ 6 V
13. 31	bk	14. 13	15. 19	bk	0 V
11. 08	oe	14. 22			
B. 17	gy	14. 23	25. 13	rd/be	
B. 16	rd/be	14. 24			
B. 18	we	14. 25			
B. 19	gy	14. 26	27. 08	oe	
		14. 29	18. 08	vt/we	S-
B. 33	gn	14. 30			Blank origin
		14. 33	18. 09	oe	S+
		14. 34	18. 11	gn	C+
		14. 35	18. 12	vt/we	C -

Table 11. 16 CSR panel AB. Card No 14 connections (Card type DAF 4/11)

From	Colour	Terminal	To	Colour	Note
14.02	be	15.02	16.02	be	-12 V
		15.03	20.16	we	
		15.05	16.20	be	
		15.05	16.16	be	
14.03	rd	15.06	16.03	rd	+ 6 V
		15.08	15.31	we	
		15.11	15.27	gn	
		15.13	15.05	gy	
A.20	rd/be	15.14			
		15.15	15.17	oe	
		15.17	15.35	vt/we	
14.13	bk	15.19	16.19	bk	0 V
11.26	gy	15.21			
		15.34	16.18	bk	

Table 11.17 CSR panel AB. Card No 15 connections
(Card type DAF 2/13)

From	Colour	Terminal	To	Colour	Note
15.02	be	16.02	17.02	be	-12 V
15.06	rd	16.03	17.03	rd	+ 6 V
B.21	gn	16.06	18.07	gn	
B.22	we	16.07	18.14	vt/we	
		16.08	16.30	we	
A.07	rd/be	16.09			
		16.10	18.16	gy	
		16.11	16.35	gn	
		16.12	16.34	vt/we	
A.17	oe	16.13	16.08	oe	
A.06	vt/we	16.14			
		16.15	18.10	we	
15.05	be	16.16	17.16	be	
A.18	gn	16.17	16.12	gy	
15.34	bk	16.18	16.11	we	
15.19	bk	16.19	17.19	bk	0 V
15.05	be	16.20	17.20	be	
B.23	vt/we	16.23	18.24	oe	
B.24	we	16.24	18.31	gn	
		16.25	17.13	gy	
A.09	we	16.26			
		16.27	18.33	we	
		16.28	17.18	vt/we	
		16.29	17.17	oe	
		16.30	16.25	gn	
A.08	oe	16.31			
		16.32	18.27	rd/be	
		16.34	16.29	rd/be	
		16.35	16.28	gy	

Table 11.18 CSR panel AB. Card No 16 connections
(Card type DAF 3/5)

From	Colour	Terminal	To	Colour	Note
16.02	be	17.02	18.02	be	-12 V
16.03	rd	17.03	18.19	rd	+ 6 V
B.25	rd/be	17.06	19.07	vt/we	
B.26	we	17.07	19.14	oe	
		17.08	17.30	gy	
A.11	oe	17.09			
		17.10	19.16	rd/be	
		17.11	17.35	oe	
		17.12	17.34	vt/we	
16.25	gy	17.13	17.08	gn	
A.10	rd/be	17.14			
		17.15	19.10	gy	
16.16	be	17.16			
16.29	oe	17.17	17.12	gy	
16.28	vt/we	17.18	17.11	rd/be	
16.19	bk	17.19	20.34	bk	0 V
16.20	be	17.20			
B.27	rd/be	17.23	19.24	gn	
B.28	we	17.24	19.31	vt/we	
A.13	gn	17.26			
		17.27	19.33	gy	
		17.30	17.25	vt/we	
A.12	we	17.31			
		17.32	19.27	we	
		17.34	17.29	rd/be	
		17.35	17.28	we	

Table 11.19 CSR panel AB. Card No 17 connections
(Card type DAF 3/5)

From	Colour	Terminal	To	Colour	Note
17.02	be	18.02	19.02	be	-12 V
		18.03	20.08	gn	sin 1
		18.04	21.22	we	cos 1
		18.05	20.10	vt/we	sin 2
		18.06	21.24	gn	cos 2
16.06	gn	18.07			
14.29	vt/we	18.08	18.13	rd/be	
14.33	oe	18.09	18.15	gy	
16.15	we	18.10			
14.34	gn	18.11	18.17	we	
14.35	vt/we	18.12	18.18	rd/be	
		18.13	18.25	oe	
16.07	vt/we	18.14			
		18.15	18.26	vt/we	
16.10	gy	18.16			
		18.17	18.28	gn	
		18.18	18.29	oe	
17.03	rd	18.19	19.19	rd	+6 V
		18.20	20.22	rd/be	sin 3
		18.21	21.26	gy	cos 3
		18.22	20.24	oe	sin 4
		18.23	22.06	vt/we	cos 4
16.23	oe	18.24			
		18.25	18.30	we	
		18.26	18.32	rd/be	
16.32	rd/be	18.27			
		18.28	18.34	gy	
		18.29	18.35	we	
		18.30	19.30	gn	
16.24	gn	18.31			
		18.32	19.32	oe	
16.27	we	18.33			
		18.34	19.34	vt/we	
		18.35	19.35	gn	

Table 11.20 CSR panel AB. Card No 18 connections
(Card type DAF 3/4)

From	Colour	Terminal	To	Colour	Note
18.02	be	19.02	20.04	be	-12 V
		19.03	20.26	rd/be	sin 5
		19.04	22.08	gy	cos 5
		19.05	21.06	oe	sin 6
		19.06	22.10	vt/we	cos 6
17.06	vt/we	19.07			
17.15	gy	19.10			
		19.13	19.08	we	
17.07	oe	19.14			
		19.15	19.09	vt/we	
17.10	rd/be	19.16			
		19.17	19.11	we	
		19.18	19.12	vt/we	
18.19	rd	19.19	20.02	rd	+6 V
		19.20	21.08	we	sin 7
		19.21	22.22	rd/be	cos 7
		19.22	21.10	gn	sin 8
		19.23	22.24	oe	cos 8
17.23	gn	19.24			
		19.25	19.13	oe	
		19.26	19.15	gy	
17.32	we	19.27			
		19.28	19.17	oe	
		19.29	19.18	gy	
18.30	gn	19.30	19.25	rd/be	
17.24	vt/we	19.31			
18.32	oe	19.32	19.26	gn	
17.27	gy	19.33			
18.34	vt/we	19.34	19.28	rd/be	
18.35	gn	19.35	19.29	gn	

Table 11.21 CSR panel AB. Card No 19 connections
(Card type DAF 3/4)

From	Colour	Terminal	To	Colour	Note
19.19	rd	20.02	21.02	rd	+ 6 V
19.02	be	20.04	21.04	be	-12 V
05.29	vt/we	20.06			
A.19	we	20.06			
18.03	gy	20.08			
18.05	vt/we	20.10			
		20.12	23.08	gy	sin 2
		20.14	23.13	gn	sin 1
15.03	we	20.16			
18.20	rd/be	20.22			
18.22	oe	20.24			
19.03	rd/be	20.26			
		20.28	24.13	oe	sin 5
		20.30	23.25	rd/be	sin 4
		20.32	23.30	vt/we	sin 3
17.19	bk	20.34	21.34	bk	0 V

Table 11.22 CSR panel AB. Card No 20 connections
(Card type DAF 3/10)

From	Colour	Terminal	To	Colour	Note
20.02	rd	21.02	22.02	rd	+ 6 V
20.04	be	21.04	22.04	be	-12 V
19.05	oe	21.06			
19.20	we	21.08			
19.22	gn	21.10			
		21.12	24.25	gy	sin 8
		21.14	24.30	gn	sin 7
		21.16	24.08	we	sin 6
18.04	we	21.22			
18.06	gn	21.24			
18.21	gy	21.26			
		21.28	25.25	oe	cos 3
		21.30	25.30	rd/be	cos 2
		21.32	25.08	vt/we	cos 1
20.34	bk	21.34	22.34	bk	0 V

Table 11.23 CSR panel AB. Card No 21 connections
(Card type DAF 3/10)

From	Colour	Terminal	To	Colour	Note
21.02	rd	22.02	23.06	rd	+ 6 V
21.04	be	22.04	23.05	be	-12 V
18.23	vt/we	22.06			
19.04	gy	22.08			
19.06	vt/we	22.10			
		22.12	26.30	gy	cos 6
		22.14	26.08	gn	cos 5
		22.16	26.13	we	cos 4
19.21	rd/be	22.22			
19.23	oe	22.24			
		22.26	27.21	rd/be	
A.14	we	22.28			
		22.30	27.13	rd/be	cos 8
		22.32	26.25	vt/we	cos 7
21.34	bk	22.34	23.18	bk	0 V

Table 11.24 CSR panel AB. Card No 21 connections
(Card type DAF 3/10)

From	Colour	Terminal	To	Colour	Note
		23.02	28.16	we	
		23.03	28.18	oe	
22.04	be	23.05	24.05	be	-12 V
22.02	rd	23.06	24.06	rd	+ 6 V
20.12	gy	23.08			
		23.09	23.12	oe	
		23.11	23.17	gn	
		23.12	23.14	we	
20.14	gn	23.13			
		23.14	23.16	gn	
		23.16	23.26	gy	
		23.17	23.28	gy	
22.34	bk	23.18	24.18	bk	0 V
		23.21	28.14	gn	
		23.24	28.12	gy	
20.30	rd/be	23.25			
		23.26	23.29	vt/we	
		23.28	23.34	vt/we	
		23.29	23.31	rd/be	
20.32	vt/we	23.30			
		23.31	23.33	oe	
		23.33	23.35	we	
		23.34	24.34	rd/be	

Table 11.25 CSR panel AB. Card No 23 connections
(Card type DAF 2/12)

From	Colour	Terminal	To	Colour	Note
		24.02	28.08	rd/be	
		24.03	28.10	vt/we	
23.05	be	24.05	25.05	be	-12 V
23.06	rd	24.06	25.06	rd	+ 6 V
21.16	we	24.08			
		24.09	24.12	vt/we	
		24.11	25.11	gy	
		24.12	24.14	rd/be	
20.28	oe	24.13			
		24.14	24.16	oe	
		24.16	24.26	we	
		24.17	24.11	gn	
23.18	bk	24.18	25.18	bk	0 V
		24.21	28.06	oe	
		24.24	28.04	we	
21.12	gy	24.25			
		24.26	24.29	gn	
		24.28	24.17	we	
		24.29	24.31	gy	
21.14	gn	24.30			
		24.31	24.33	vt/we	
		24.33	24.35	rd/be	
23.34	rd/be	24.34	24.28	oe	

Table 11.26 CSR panel AB. Card No 24 connections
(Card type DAF 2/12)

From	Colour	Terminal	To	Colour	Note
		25.02	29.18	gy	
24.05	be	25.05	26.05	be	-12 V
24.06	rd	25.06	26.06	rd	+ 6 V
21.32	vt/we	25.08			
		25.09	25.12	gn	
24.11	gy	25.11	25.17	vt/we	
		25.12	25.14	gy	
14.23	rd/be	25.13			
		25.14	25.16	vt/we	
		25.15	28.30	gn	
		25.16	25.26	rd/be	
		25.17	25.28	rd/be	
24.18	bk	25.18	26.18	bk	0 V
		25.21	29.16	vt/we	
		25.24	29.14	rd/be	
21.28	oe	25.25			
		25.26	25.29	oe	
		25.28	25.34	oe	
		25.29	25.31	we	
21.30	rd/be	25.30			
		25.31	25.33	gn	
		25.33	25.35	gy	
		25.34	26.34	we	

Table 11.27 CSR panel AB. Card No 25 connections
(Card type DAF 2/12)

From	Colour	Terminal	To	Colour	Note
		26.02	29.10	we	
		26.03	29.12	oe	
25.05	be	26.05	27.05	be	-12 V
25.06	rd	26.06	27.06	rd	+ 6 V
22.14	gn	26.08			
		26.09	26.12	oe	
		26.11	27.11	rd/be	
		26.12	26.14	we	
22.16	we	26.13			
		26.14	26.16	gn	
		26.16	26.26	gy	
		26.17	26.11	vt/we	
25.18	bk	26.18	27.18	bk	0 V
		26.21	29.08	gn	
		26.24	29.06	gy	
22.32	vt/we	26.25			
		26.26	26.29	vt/we	
		26.28	26.17	gy	
		26.29	26.31	rd/be	
22.12	gy	26.30			
		26.31	26.33	oe	
		26.33	26.35	we	
25.34	we	26.34	26.28	gn	

Table 11.28 CSR panel AB. Card No 26 connections
(Card type DAF 2/12)

From	Colour	Terminal	To	Colour	Note
		27.03	29.04	vt/we	
A.31	be	27.05			-12 V
26.05	be	27.05			
A.30	rd	27.06			+ 6 V
26.06	rd	27.06			
14.26	oe	27.08			
		27.09	27.12	vt/we	
		27.10	29.30	rd/be	
26.11	rd/be	27.11	27.17	gn	
27.09	vt/we	27.12	27.14	rd/be	
22.30	rd/be	27.13			
27.12	rd/be	27.14	27.16	oe	
27.14	oe	27.16	27.19	we	
B.20	gy	27.17			
27.11	rd/be	27.17			
26.18	bk	27.18	28.22	bk	0 V
13.10	bk	27.19			
27.16	oe	27.19			
22.26	rd/be	27.21			
A.25	gy	27.30	27.34	rd/be	
A.16	we	27.31			
A.15	oe	27.33			
27.30	rd/be	27.34			

Table 11.29 CSR panel AB. Card No 27 connections
(Card type DAF 2/12)

From	Colour	Terminal	To	Colour	Note
13.33	rd/be	28.02	29.02	vt/we	+24 V
24.24	we	28.04			
24.21	oe	28.06			
24.02	rd/be	28.08			
24.03	vt/we	28.10			
23.24	gy	28.12			
23.21	gn	28.14			
23.02	we	28.16			
23.03	oe	28.18			
		28.20	29.20	gy	+18 V
27.18	bk	28.22	29.22	bk	0 V
13.32	vt/we	28.28	29.28	rd/be	-24 V
25.15	gn	28.30			
		28.32	29.32	vt/we	-18 V
B.31	gn	28.34			Sine

Table 11.30 CSR panel AB. Card No 28 connections
(Card type DAF 4/6)

From	Colour	Terminal	To	Colour	Note
28.02	vt/we	29.02			+24 V
A.33	vt/we	29.02			
27.03	vt/we	29.04			
26.24	gy	29.06			
26.21	gn	29.08			
26.02	we	29.10			
26.03	oe	29.12			
25.24	rd/be	29.14			
25.21	vt/we	29.16			
25.02	gy	29.18			
28.20	gy	29.20			
A.27	oe	29.20			+18 V
28.22	bk	29.22			
A.29	bk	29.22			Philips ground
28.28	rd/be	29.28			-24 V
A.32	rd/be	29.28			
27.10	rd/be	29.30			
28.32	vt/we	29.32			-18 V
A.28	gy	29.32			
B.30	oe	29.34			

Table 11.31 CSR panel AB. Card No 29 connections
(Card type DAF 4/6)

From	Colour	Terminal	To	Colour	Note
F.20	gy	C.02	18.23	gn	φ1
U.27	gn	C.02			
F.21	vt/we	C.03	18.24	oe	φ2
U.28	oe	C.03			
F.22	rd/be	C.04	18.25	gy	φ3
U.29	gy	C.04			
F.23	oe	C.05	18.26	we	φ4
U.30	we	C.05			
F.24	we	C.06	18.27	rd/be	φ5
U.31	rd/be	C.06			
F.25	gn	C.07	18.28	vt/we	φ6
U.32	vt/we	C.07			
F.26	gy	C.08	18.29	gn	φ7
U.33	gn	C.08			
F.27	vt/we	C.09	18.30	oe	φ8
U.34	oe	C.09			
F.28	rd/be	C.10	18.31	gy	φ9
U.35	gy	C.10			
A.22	rd/be	C.11	18.32	we	Stop line
A.20	vt/we	C.12	18.22	rd/be	Set blanking
B.20	rd/be	C.13	23.28	vt/we	$\overline{P1}$
A.18	gn	C.14	24.28	gn	$\overline{P4+P7}$
A.17	rd/be	C.15	24.14	oe	$\overline{P4+P8}$
B.16	we	C.16	08.31	gy	$\overline{S+}$
B.17	vt/we	C.17	09.31	we	$\overline{S-}$
B.18	gy	C.18	06.31	rd/be	$\overline{C+}$
B.19	oe	C.19	07.31	vt/we	$\overline{C-}$
A.06	we	C.20	16.10	gn	X1
A.07	oe	C.21	16.06	oe	X2
A.08	gy	C.22	16.32	gy	X3
A.09	gn	C.23	16.28	we	X4
A.10	rd/be	C.24	17.10	rd/be	X5
A.11	we	C.25	17.06	vt/we	X6
A.12	gn	C.26	17.32	gn	X7
A.13	oe	C.27	17.28	oe	X8
SW4.08a	gy	C.28	09.28	gy	$\overline{P3}$
SW4.17a	we	C.29	24.16	we	P2
SW4.26a	rd/be	C.30	10.28	rd/be	$\overline{P4}$
SW4.08a	vt/we	C.31	11.27	vt/we	
PS1.05	be	C.32	27.05	be	- 12 V
gnd	bk	C.33	27.19	bk	0 V
E.34	rd	C.34	27.06	rd	+ 6 V

Table 12.1 CSR panel CD. Plug C connections
(Plug card type DAF 1/3/6)

From	Colour	Terminal	To	Colour	Note
U.10	gn	D.02	11.16	gn	α1
U.09	oe	D.03	11.17	oe	α2
U.08	gy	D.04	11.18	gy	α3
U.07	we	D.05	11.19	we	α4
U.06	rd/be	D.06	11.20	rd/be	α5
U.05	vt/we	D.07	11.29	vt/we	α6
U.04	gn	D.08	11.28	gn	α7
U.03	oe	D.09	03.35	oe	α8
U.02	gy	D.10	03.28	gy	α9
U.24	we	D.11	12.29	we	$\overline{Q1}$
U.25	rd/be	D.12	12.17	rd/be	$\overline{Q2}$
gnd	bk	D.13	13.08	we	
gnd	bk	D.14	13.14	rd/be	
gnd	bk	D.15	13.25	vt/we	
gnd	bk	D.16	13.31	gn	
gnd	bk	D.17	14.08	oe	
gnd	bk	D.18	14.14	gy	
gnd	bk	D.19	14.25	we	
gnd	bk	D.20	14.22	rd/be	
SW4.08b	gn	D.21	03.13	gn	
A.19	gy	D.22	07.28	oe	P6
SW9.03	we	D.23	27.13	gy	
A.05	we	D.24	22.22	we	
A.02	gn	D.25	22.29	rd/be	
A.03	gy	D.26	22.28	vt/we	
A.04	vt/we	D.27	22.27	gn	
SW11.02	we	D.28	25.04	oe	Reset
Y.20	gy	D.29	26.16	gy	
Y.19	we	D.30	26.02	we	
SW7.02	gy	D.31	26.28	rd/be	L
SW6.02	vt/we	D.32	26.30	gn	K
SW5.02	rd/be	D.33	26.32	oe	J
SW8.02	gn	D.34	26.34	gy	M
A.25	gy	D.35	22.30	oe	Shift S

Table 12.2 CSR panel CD. Plug D connections
(Plug card type DAF 1/3/7)

From	Colour	Terminal	To	Colour	Note
		01.02	02.02	be	-12 V
		01.03	02.03	rd	+ 6 V
		01.06	04.07	gn	α1
		01.07	01.33	oe	
		01.07	04.14	gy	α2
		01.08	01.30	rd/be	
		01.09	01.31	gn	Reset
		01.10	04.16	we	
		01.11	18.24	rd/be	φ2
		01.12	01.34	gy	Set
		01.13	01.08	we	
		01.14	01.09	vt/we	Reset
		01.15	04.10	rd/be	
		01.16	10.30	vt/we	
		01.17	01.12	oe	Set
		01.18	18.23	we	φ1
		01.19	02.19	bk	0 V
		01.19	02.08	bk	
		01.20	02.20	gn	
		01.23	04.24	vt/we	α3
		01.24	02.16	gy	α4
		01.25	02.13	gn	
		01.26	02.14	gy	Reset
		01.27	04.33	gn	
		01.28	18.26	gn	φ4
		01.29	02.17	rd/be	Set
		01.30	01.25	vt/we	
		01.31	01.26	oe	Reset
		01.32	04.27	oe	
		01.34	01.29	we	Set
		01.35	18.25	vt/we	φ3

Table 12.3 CSR panel CD. Card No 1 connections
(Card type DAF 3/5)

From	Colour	Terminal	To	Colour	Note
01.02	be	02.02	03.02	be	-12 V
01.03	rd	02.03	03.03	rd	+ 6 V
		02.05	24.16	rd/be	
		02.06	05.07	oe	α5
		02.07	05.14	gy	α6
		02.07	02.33	gn	
01.19	bk	02.08			
		02.09	02.31	gn	Reset
		02.10	05.16	we	
		02.11	18.28	rd/be	φ6
		02.12	02.34	oe	Set
01.25	gn	02.13	02.08	vt/we	
01.26	gy	02.14	02.09	vt/we	
		02.15	05.10	rd/be	
01.24	gy	02.16	04.31	oe	α4
01.29	rd/be	02.17	02.12	oe	Set
		02.18	18.27	we	φ5
01.19	bk	02.19	03.19	bk	0 V
01.20	gn	02.20	03.20	gn	Inhibit
		02.23	05.24	vt/we	α7
		02.24	03.16	gy	α8
		02.25	03.13	rd/be	
		02.26	03.14	gy	Reset
		02.28	18.30	gn	φ8
		02.29	03.17	rd/be	Set
		02.30	02.25	we	
		02.31	02.26	oe	Reset
		02.32	05.27	gn	
		02.34	02.29	we	Set
		02.35	18.29	vt/we	φ7

Table 12.4 CSR panel CD. Card No 2 connections
(Card type DAF 3/5)

From	Colour	Terminal	To	Colour	Note
02.02	be	03.02	04.02	be	-12 V
02.03	rd	03.03	04.19	rd	+ 6 V
		03.06	03.28	oe	α9
D.21	gn	03.13			
02.25	rd/be	03.13			
02.26	gy	03.14	09.28	vt/we	$\overline{P3}$
02.24	gy	03.16	03.35	gn	$\overline{\alpha 8}$
02.29	rd/be	03.17	10.28	rd/be	$\overline{P4}$
		03.18	18.31	gy	φ9
02.19	bk	03.19			
02.20	gn	03.20	08.28	we	Inhibit
		03.23	11.11	vt/we	
		03.24	11.12	oe	
		03.25	03.19	gy	
		03.26	23.16	rd/be	P8
		03.27	11.09	gn	Q2
D.10	gy	03.28			
		03.29	03.34	vt/we	P9
		03.29	10.12	gn	P9
		03.30	03.25	oe	
		03.30	06.18	bk	0 V
		03.31	03.26	we	P8
		03.32	11.10	rd/be	Q1
D.09	oe	03.35			

Table 12.5 CSR panel CD. Card No 3 connections
(Card type DAF 3/5)

From	Colour	Terminal	To	Colour	Note
03.02	be	04.02	05.02	be	-12 V
		04.03	06.06	gn	$\alpha1$
		04.04	06.08	oe	
		04.05	06.10	gy	$\alpha2$
		04.06	07.06	we	
01.06	gn	04.07	11.16	gn	$\alpha1$
		04.08	06.28	vt/we	P10
		04.09	07.28	gn	P6
01.15	rd/be	04.10			
		04.11	04.08	rd/be	
		04.11	04.13	gy	
		04.12	04.15	oe	
		04.12	04.09	vt/we	
		04.13	04.17	gn	
01.07	gy	04.14	11.17	oe	$\alpha2$
		04.15	04.18	oe	
01.10	we	04.16			
		04.17	04.25	gy	
		04.18	04.26	we	
03.03	rd	04.19	05.19	rd	+ 6 V
		04.20	07.08	rd/be	$\alpha3$
		04.21	07.10	vt/we	
		04.22	08.06	gn	$\alpha4$
		04.23	08.08	oe	
01.23	vt/we	04.24	11.18	gy	$\alpha3$
		04.25	04.28	rd/be	
		04.26	04.29	vt/we	
01.32	oe	04.27			
		04.28	04.30	gn	
		04.29	04.32	oe	
		04.30	04.34	gy	
02.16	oe	04.31	11.19	we	$\alpha4$
		04.32	04.35	we	
01.27	gn	04.33			
		04.34	05.08	rd/be	
		04.35	05.09	vt/we	

Table 12.6 CSR panel CD. Card No 4 connections
(Card type DAF 3/4)

From	Colour	Terminal	To	Colour	Note
04.02	be	05.02	06.03	be	-12 V
		05.03	08.10	gn	
		05.04	09.06	oe	
		05.05	09.08	gy	
		05.06	09.10	we	
02.06	oe	05.07	11.20	rd/be	α5
04.34	rd/be	05.08	05.11	oe	
04.35	vt/we	05.09	05.12	gy	
02.15	rd/be	05.10			
		05.11	05.13	we	
		05.12	05.15	rd/be	
		05.13	05.17	vt/we	
02.07	gy	05.14	11.29	vt/we	α6
		05.15	05.18	gn	
02.10	we	05.16			
04.19	rd	05.19	06.02	rd	+ 6 V
		05.20	10.06	rd/be	
		05.21	10.08	vt/we	
02.23	vt/we	05.24	11.28	gn	α7
		05.25	05.28	we	
		05.26	05.29	rd/be	
02.32	gn	05.27			
		05.28	23.12	gy	
		05.29	23.14	we	

Table 12.7 CSR panel CD. Card No 5 connections
(Card type DAF 3/4)

From	Colour	Terminal	To	Colour	Note
05.19	rd	06.02	07.02	rd	+ 6 V
05.02	be	06.03	07.03	be	-12 V
04.03	gn	06.06			
04.04	oe	06.08			
04.05	gy	06.10			
		06.12	13.10	gy	α2
		06.14	13.07	oe	
		06.16	13.04	gn	α1
03.30	bk	06.18	07.18	bk	0 V
		06.22	11.03	we	
		06.24	11.04	rd/be	
		06.26	21.30	gy	
04.08	vt/we	06.28			
		06.30	06.31	oe	
C.18	rd/be	06.31			
		06.32	06.33	vt/we	
		06.33	06.34	gn	gnd

Table 12.8 CSR panel CD. Card No 6 connections
(Card type DAF 2/16)

From	Colour	Terminal	To	Colour	Note
06.02	rd	07.02	08.02	rd	+ 6 V
06.03	be	07.03	08.03	be	-12 V
04.06	we	07.06			
04.20	rd/be	07.08			
04.21	vt/we	07.10			
		07.12	13.26	rd/be	
		07.14	13.16	we	α3
		07.16	13.13	gy	
06.18	bk	07.18	08.18	bk	0 V
		07.22	11.23	vt/we	
		07.24	12.03	gn	
		07.26	20.30	gy	
D.22	oe	07.28			
04.09	gn	07.28			
		07.30	07.31	oe	
C.19	vt/we	07.31			
		07.32	07.33	gn	
		07.33	07.34	oe	

Table 12.9 CSR panel CD. Card No 7 connections (Card type DAF 2/16)

From	Colour	Terminal	To	Colour	Note
07.02	rd	08.02	09.02	rd	+ 6 V
07.03	be	08.03	09.03	be	-12 V
04.22	gn	08.06			
04.23	oe	08.08			
05.03	gn	08.10			
		08.12	14.04	rd/be	α5
		08.14	13.32	we	α4
		08.16	13.29	gy	α4
07.18	bk	08.18	09.18	bk	0 V
		08.22	12.04	vt/we	
		08.24	12.05	gn	
		08.26	22.05	gy	
03.20	we	08.28			
		08.30	08.31	oe	
C.16	gy	08.31			
		08.32	08.33	gn	
		08.33	08.34	oe	

Table 12.10 CSR panel CD. Card No 8 connections (Card type DAF 2/16)

From	Colour	Terminal	To	Colour	Note
08.02	rd	09.02	10.02	rd	+ 6 V
08.03	be	09.03	10.03	be	-12 V
05.04	oe	09.06			
05.05	gy	09.08			
05.06	we	09.10			
		09.12	14.13	oe	α6
		09.14	14.10	gn	α6
08.18	bk	09.18	10.18	bk	0 V
		09.16	14.07	vt/we	α5
		09.22	12.22	gy	
		09.24	12.23	we	
		09.26	19.22	vt/we	
C.28	gy	09.28			
03.14	vt/we	09.28			
		09.30	09.31	rd/be	
C.17	we	09.31			
		09.32	09.33	we	
		09.33	09.34	rd/be	

Table 12.11 CSR panel CD. Card No 9 connections
(Card type DAF 2/16)

From	Colour	Terminal	To	Colour	Note
09.02	rd	10.02	13.19	rd	+ 6 V
09.03	be	10.03	11.02	be	-12 V
05.20	rd/be	10.06			
05.21	vt/we	10.08			
		10.10	12.21	gy	
03.29	gn	10.12			
		10.14	14.26	oe	α7
		10.16	14.16	gn	α7
09.18	bk	10.18	13.33	bk	0 V
		10.22	11.05	rd/be	
		10.24	11.21	gn	
		10.26	20.07	oe	P4
C.30	gy	10.28			
03.17	rd/be	10.28			
01.16	vt/we	10.30			Sub One
		10.31	11.26	vt/we	
		10.32	10.33	gy	
		10.33	10.34	we	

Table 12.12 CSR panel CD. Card No 10 connections
(Card type DAF 2/16)

From	Colour	Terminal	To	Colour	Note
10.03	be	11.02	12.02	be	-12 V
06.22	we	11.03			
06.24	rd/be	11.04			
10.22	rd/be	11.05	11.22	oe	Sub one
		11.08	11.32	rd/be	P2
03.27	gn	11.09	12.09	oe	Q2
03.32	rd/be	11.10	11.30	vt/we	Q1
03.23	vt/we	11.11	12.10	gy	
03.24	oe	11.12	11.31	gy	
		11.13	12.08	rd/be	
D.02	gn	11.16			
04.07	gn	11.16			
D.03	oe	11.17			
04.14	oe	11.17			
D.04	gy	11.18			
04.24	gy	11.18			
D.05	we	11.19			
04.31	we	11.19			
D.06	rd/be	11.20			
05.07	rd/be	11.20			
10.24	gn	11.21			
07.22	vt/we	11.23	11.24	gn	
		11.25	21.07	vt/we	
10.31	vt/we	11.26			
C.31	vt/we	11.27			
D.08	gn	11.28			
05.24	gn	11.28			
D.07	vt/we	11.29			
05.14	vt/we	11.29			
		11.30	12.16	gn	Q1
		11.31	12.12	we	
		11.32	12.13	we	Q2

Table 12.13 CSR panel CD. Card No 11 connections
(Card type DAF 3/9)

From	Colour	Terminal	To	Colour	Note
11.02	be	12.02	13.02	be	-12 V
07.24	gn	12.03			
08.22	vt/we	12.04			
08.24	gn	12.05			
11.13	rd/be	12.08	12.18	we	P5
11.09	oe	12.09	12.28	gn	
11.11	gy	12.10	12.11	gn	
		12.11	12.29	vt/we	
11.31	we	12.12	12.17	gy	
11.32	we	12.13	12.27	oe	
11.30	gn	12.16	12.30	gy	
D.12	rd/be	12.17			
		12.18	12.32	rd/be	
10.10	gy	12.21			
09.22	gy	12.22	12.34	rd/be	
09.24	we	12.23	12.24	gn	
		12.25	18.05	oe	S
		12.26	21.08	gy	I
		12.27	19.21	oe	P2
		12.28	12.31	we	
D.11	we	12.29			
		12.32	20.08	vt/we	P5

Table 12.14 CSR panel CD. Card No 12 connections
(Card type DAF 3/9)

From	Colour	Terminal	To	Colour	Note
12.02	be	13.02	14.02	be	-12 V
06.16	gn	13.04			
		13.05	13.08	gy	
		13.05	15.19	we	
		13.06	15.15	gn	
06.14	oe	13.07			
D.13	we	13.08			
		13.09	15.17	oe	
06.12	gy	13.10			
		13.11	13.14	vt/we	
		13.11	15.27	rd/be	
		13.12	15.23	gy	
07.16	gy	13.13			
D.14	rd/be	13.14			
		13.15	15.25	we	
07.14	we	13.16			
		13.17	13.25	gn	
		13.17	15.32	oe	
		13.18	15.29	rd/be	
10.02	rd	13.19	14.19	rd	+ 6 V
		13.21	13.22	bk	
		13.22	13.23	bk	
		13.23	13.34	bk	
		13.24	15.31	vt/we	
D.15	vt/we	13.25			
07.12	rd/be	13.26			
		13.27	15.35	gn	
		13.28	13.31	we	
		13.28	15.33	rd/be	
08.16	gy	13.29			
		13.30	15.34	oe	
D.16	gn	13.31			
08.14	we	13.32			
10.18	bk	13.33	14.33	bk	0 V

Table 12.15 CSR panel CD. Card No 13 connections
(Card type DAF 4/9)

From	Colour	Terminal	To	Colour	Note
13.02	be	14.02	16.02	be	-12 V
08.12	rd/be	14.04			
		14.05	14.08	gn	
		14.05	15.24	oe	
09.16	vt/we	14.07			
		14.06	15.22	gn	
D.17	oe	14.08			
		14.09	15.20	oe	
09.14	gn	14.10			
		14.11	14.14	we	
		14.12	15.16	gy	
D.18	gy	14.14			
09.12	oe	14.13			
		14.15	15.14	we	
10.16	gn	14.16			
		14.17	14.25	gn	
		14.17	15.12	oe	
		14.18	15.10	rd/be	
13.19	rd	14.19	16.04	rd	+ 6 V
		14.21	15.26	rd/be	
D.20	rd/be	14.22	15.30	vt/we	
		14.23	22.24	we	P4* + P8*
		14.24	15.08	vt/we	
D.19	we	14.25			
10.14	oe	14.26			
		14.29	14.03	be	
		14.32	14.29	be	
13.33	bk	14.33	16.18	bk	0 V
		14.34	15.06	bk	X - return

Table 12.16 CSR panel CD. Card No 14 connections
(Card type DAF 4/9)

From	Colour	Terminal	To	Colour	Note
		15.02	16.30	gn	X4
		15.03	16.34	oe	X3
		15.04	16.08	gy	X2
		15.05	16.12	we	X1
14.34	bk	15.06	15.34	bk	X - return
		15.07	17.12	vt/we	X5
14.24	vt/we	15.08			
		15.09	17.08	gn	X6
14.18	rd/be	15.10			
		15.11	17.34	oe	X7
14.17	oe	15.12			
		15.13	17.30	gy	X8
14.15	we	15.14			
13.06	gn	15.15			
14.12	gy	15.16			
13.09	oe	15.17			
13.05	we	15.19	15.21	we	
14.09	oe	15.20			
14.06	gn	15.22			
13.12	gy	15.23			
14.05	oe	15.24			
13.15	we	15.25			
14.21	rd/be	15.26			
13.11	rd/be	15.27			
13.18	rd/be	15.29			
14.22	vt/we	15.30			
13.24	vt/we	15.31			
13.17	oe	15.32			
13.28	rd/be	15.33			
13.30	oe	15.34			
13.27	gn	15.35			

Table 12.17 CSR panel CD. Card No 15 connections
(Card type DAF 4/5)

From	Colour	Terminal	To	Colour	Note
14.02	be	16.02	17.02	be	-12 V
14.19	rd	16.04	17.04	rd	+ 6 V
C.21	oe	16.06			X2
15.04	gy	16.08			
C.20	gn	16.10			X1
15.05	we	16.12			
14.33	bk	16.18	17.18	bk	0 V
C.23	we	16.28			X4
15.02	gn	16.30			
C.22	gy	16.32			X3
15.03	oe	16.34			

Table 12.18 CSR panel CD. Card No 16 connections
(Card type DAF 4/10)

From	Colour	Terminal	To	Colour	Note
16.02	be	17.02	18.03	be	-12 V
16.04	rd	17.04	18.04	rd	+ 6 V
C.25	vt/we	17.06			X6
15.09	gn	17.08			
C.24	rd/be	17.10			X5
15.07	vt/we	17.12			
16.18	bk	17.18	18.14	bk	0 V
C.27	oe	17.28			X8
15.13	gy	17.30			
C.26	gn	17.32			X7
15.11	oe	17.34			

Table 12.19 CSR panel CD. Card No 17 connections
(Card type DAF 4/10)

From	Colour	Terminal	To	Colour	Note
17.02	be	18.03	19.02	be	-12 V
17.04	rd	18.04	19.06	rd	+ 6 V
12.25	oe	18.05	19.03	we	
		18.06	18.02	gy	
		18.06	22.09	vt/we	
		18.10	18.09	oe	A
		18.10	22.10	rd/be	
		18.12	18.14	gn	
		18.12	19.33	bk	0 V
17.18	bk	18.14			
C.12	rd/be	18.22			
01.18	we	18.23			
C.02	gn	18.23			φ1
01.11	rd/be	18.24			
C.03	oe	18.24			φ2
01.35	vt/we	18.25			
C.04	gy	18.25			φ3
01.28	gn	18.26			
C.05	we	18.26			φ4
C.06	rd/be	18.27			φ5
02.18	we	18.27			
C.07	vt/we	18.28			φ6
02.11	rd/be	18.28			
C.08	gn	18.29			φ7
02.35	vt/we	18.29			
C.09	oe	18.30			φ8
02.28	gn	18.30			
C.10	gy	18.31			φ9
03.18	gy	18.31			
C.11	we	18.32			

Table 12.20 CSR panel CD. Card No 18 connections
(Card type DAF 3/12)

From	Colour	Terminal	To	Colour	Note
18.03	be	19.02	20.02	be	-12 V
18.05	we	19.03	20.03	we	
18.04	rd	19.06	20.06	rd	+ 6 V
		19.08	19.31	rd/be	
		19.08	23.26	oe	P1
		19.11	19.27	gn	
		19.13	27.15	gy	
		19.15	19.19	oe	
		19.16	27.17	rd/be	
		19.17	27.03	oe	
12.27	oe	19.21			P2
09.26	vt/we	19.22	20.17	vt/we	P3
		19.25	20.13	vt/we	
		19.25	22.16	we	
		19.30	24.06	gy	

Table 12.21 CSR panel CD. Card No 19 connections
(Card type DAF 2/13)

From	Colour	Terminal	To	Colour	Note
19.02	be	20.02	21.02	be	-12 V
19.03	we	20.03	21.03	rd/be	
19.06	rd	20.06	21.06	rd	+ 6 V
10.26	oe	20.07			
12.32	vt/we	20.08	20.31	gn	P5
		20.11	20.27	oe	
19.25	vt/we	20.13			
		20.16	22.25	rd/be	
		20.16	22.17	vt/we	
19.22	vt/we	20.17			
		20.21	22.11	gn	P6
		20.22	21.17	gy	P7
		20.25	21.13	we	
		20.25	22.26	oe	
07.26	gy	20.30			
19.33	bk	20.33	21.33	bk	0 V

Table 12.22 CSR panel CD. Card No 20 connections
(Card type DAF 2/13)

From	Colour	Terminal	To	Colour	Note
20.02	be	21.02	22.02	be	-12 V
20.03	rd/be	21.03	22.30	gn	S
20.06	rd	21.06	23.02	rd	+ 6 V
11.25	vt/we	21.07	23.06	gy	P8
12.26	gy	21.08	21.31	gn	P9
		21.11	21.27	oe	
		21.11	22.18	rd/be	
20.25	we	21.13			
		21.16	22.33	we	
20.22	gy	21.17			
		21.21	22.08	vt/we	P10
06.26	gy	21.30			
20.33	bk	21.33	23.35	bk	0 V

Table 12.23 CSR panel CD. Card No 21 connections
(Card type DAF 2/13)

From	Colour	Terminal	To	Colour	Note
21.02	be	22.02	23.03	be	-12 V
		22.03	23.22	we	
		22.04	23.24	rd/be	
08.26	gy	22.05			
21.21	vt/we	22.08			P10
18.06	vt/we	22.09	22.12	gy	
18.10	rd/be	22.10	22.13	oe	
20.21	gn	22.11			P6
19.25	we	22.16			
20.16	vt/we	22.17	22.32	vt/we	
21.11	rd/be	22.18			
		22.21	24.24	rd/be	
D.24	we	22.22	22.35	vt/we	
		22.23	24.22	oe	
14.23	we	22.24			
20.16	rd/be	22.25	22.32	vt/we	
20.25	oe	22.26			
D.27	gn	22.27			
D.26	vt/we	22.28			
D.25	rd/be	22.29			
D.35	oe	22.30			S
21.03	gn	22.30			
		22.31	24.31	gy	
21.16	we	22.33			
		22.34	22.24	gn	

Table 12.24 CSR panel CD. Card No 22 connections
(Card type DAF 3/9)

From	Colour	Terminal	To	Colour	Note
21.06	rd	23.02	24.02	rd	+ 6 V
22.02	be	23.03	24.03	be	-12 V
21.07	gy	23.06			
05.28	gy	23.12			
05.29	we	23.14			
03.26	rd/be	23.16			
22.03	we	23.22			
22.04	rd/be	23.24			
19.08	oe	23.26			
C.13	vt/we	23.28			$\overline{P1}$
		23.30	23.10	gn	
		23.31	23.08	gy	
		23.32	23.33	we	
		23.33	23.34	oe	
21.33	bk	23.35	24.35	bk	0 V

Table 12.25 CSR panel CD. Card No 23 connections
(Card type DAF 2/16)

From	Colour	Terminal	To	Colour	Note
23.02	rd	24.02	25.03	rd	+ 6 V
23.03	be	24.03	25.02	be	-12 V
19.30	gy	24.06			
C.15	oe	24.14			$\overline{P4 + P8}$
02.05	rd/be	24.16			
C.29	we	24.16			
		24.18	25.18	bk	gnd
22.23	oe	24.22			
22.21	rd/be	24.24			
C.14	gn	24.28			$\overline{P4 + P7}$
		24.30	24.26	we	
22.31	gy	24.31	24.08	gn	
		24.32	24.33	oe	
		24.33	24.34	gy	
23.35	bk	24.35	25.19	bk	0 V

Table 12.26 CSR panel CD. Card No 24 connections
(Card type DAF 2/16)

From	Colour	Terminal	To	Colour	Note
24.03	be	25.02	26.04	be	-12 V
24.02	rd	25.03	26.08	rd	+ 6 V
D.28	oe	25.04	25.05	rd/be	reset
		25.05	25.21	vt/we	
		25.06	26.10	rd/be	
		25.07	25.33	oe	
		25.16	26.12	we	
		25.17	26.14	gn	set
24.18	bk	25.18			
24.35	bk	25.19	25.20	gy	
		25.20	26.06	bk	0 V
		25.21	25.22	gn	
		25.23	26.22	gy	
		25.24	26.24	rd/be	
		25.27	26.18	we	
		25.32	26.20	oe	
		25.33	26.11	vt/we	

Table 12.27 CSR panel CD. Card No 25 connections
(Card type DAF 3/5)

From	Colour	Terminal	To	Colour	Note
D.30	we	26.02			
25.02	be	26.04	27.05	be	-12 V
25.20	bk	26.06	27.19	bk	0 V
25.03	rd	26.08	27.06	rd	+ 6 V
25.06	rd/be	26.10			
25.33	vt/we	26.11			
25.16	we	26.12			
25.17	gn	26.14			
D.29	gy	26.16			
25.27	we	26.18			
25.32	oe	26.20			
25.23	gy	26.22			
25.24	rd/be	26.24			
D.31	rd/be	26.28			
D.32	gn	26.30			
D.33	oe	26.32			
D.34	gy	26.34			

Table 12.28 CSR panel CD. Card No 26 connections
(Card type DAF 1/13)

From	Colour	Terminal	To	Colour	Note
19.17	oe	27.03			
C.32	be	27.05			-12 V
26.04	be	27.05			-12 V
C.34	rd	27.06			+ 6 V
26.08	rd	27.06			+ 6 V
D.23	gy	27.13			
		27.14	27.16	bk	
19.13	gy	27.15			
		27.16	27.35	bk	
19.16	rd/be	27.17			
C.33	bk	27.19			0 V
26.06	bk	27.19			0 V

Table 12.29 CSR panel CD. Card No 27 connections
(Card type DAF 2/12)

From	Colour	Terminal	To	Colour	Note
G.02	gn	E.02	17.14	gn	Select W1
G.03	gy	E.03	17.12	gn	" W2
G.04	gn	E.04	17.10	gn	" W3
G.05	gy	E.05	17.32	gn	" W4
G.06	gn	E.06	17.30	gn	" W5
G.07	gy	E.07	18.14	gn	" W6
G.08	gn	E.08	18.12	gn	" W7
G.09	gy	E.09	18.10	gn	" W8
G.10	gn	E.10	18.32	gn	" W9
G.11	gy	E.11	18.30	gn	" W10
G.12	oe	E.12	02.04	we	Set φ1
G.13	vt/we	E.13	04.04	we	" φ2
G.14	oe	E.14	06.04	we	" φ3
G.15	vt/we	E.15	08.04	we	" φ4
G.16	oe	E.16	10.04	we	" φ5
G.17	vt/we	E.17	12.04	we	" φ6
G.18	oe	E.18	14.04	we	" φ7
G.19	vt/we	E.19	16.04	we	" φ8
G.20	oe	E.20	18.04	we	" φ9
G.21	we	E.21	17.18	oe	Read W1
G.22	rd/be	E.22	17.20	oe	" W2
G.23	we	E.23	17.22	oe	" W3
G.24	rd/be	E.24	17.24	oe	" W4
G.25	we	E.25	17.26	oe	" W5
G.26	rd/be	E.26	18.18	oe	" W6
G.27	we	E.27	18.20	oe	" W7
G.28	rd/be	E.28	18.22	oe	" W8
G.29	we	E.29	18.24	oe	" W9
G.30	rd/be	E.30	18.26	oe	" W10
G.31	vt/we	E.31	18.02	vt/we	Erase
A2.02	be	E.32	18.06	be	-12 V
G.32	be	E.32			
gnd	bk	E.33	19.24	bk	0 V
G.34	rd	E.34	18.08	rd	+ 6 V

Table 13.1 CSR panel EF. Plug E connections
(Plug card type DAF 1/2/14)

From	Colour	Terminal	To	Colour	Note
T1.05	rd/be	F.10	19.04	rd/be	} 120 VAC
T1.06	rd/be	F.11	19.02	oe	
U.19	vt/we	F.13	19.22	vt/we	+50 V
C.02	gy	F.20	02.28	gy	φ1
J.20	gy	F.20			
C.03	vt/we	F.21	04.28	vt/we	φ2
J.21	vt/we	F.21			
C.04	rd/be	F.22	06.28	rd/be	φ3
J.22	rd/be	F.22			
C.05	oe	F.23	08.28	oe	φ4
J.23	oe	F.23			
C.06	we	F.24	10.28	we	φ5
J.24	we	F.24			
C.07	gn	F.25	12.28	gn	φ6
J.25	gn	F.25			
C.08	gy	F.26	14.28	gy	φ7
J.26	gy	F.26			
C.09	vt/we	F.27	16.28	vt/we	φ8
J.27	vt/we	F.27			
C.10	rd/be	F.28	18.28	rd/be	φ9
J.28	rd/be	F.28			

Table 13.2 CSR panel EF. Plug F connections
(Plug card type DAF 1/2/15)

From	Colour	Terminal	To	Colour	Note
		01.02	02.02	gy	
		01.04	02.04	we	
		01.06	02.06	be	-12 V
		01.08	02.08	rd	+ 6 V
		01.10	03.10	gn	
		01.12	03.12	gn	
		01.14	03.14	gn	
		01.16	02.16	bk	0 V
		01.18	03.18	oe	
		01.20	03.20	oe	
		01.22	03.22	oe	
		01.24	03.24	oe	
		01.26	03.26	oe	
		01.28	01.34	vt/we	
		01.28	02.28	rd/be	
		01.30	03.30	gn	
		01.32	03.32	gn	

Table 13.3 CSR panel EF. Card No 1 connections
(Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
01.02	gy	02.02	03.02	gy	
01.04	we	02.04			
E.12	we	02.04			
01.06	be	02.06	03.06	be	-12 V
01.08	rd	02.08	03.08	rd	+ 6 V
		02.10	04.10	gn	
		02.12	04.12	gn	
		02.14	04.14	gn	
01.16	bk	02.16	03.16	bk	0 V
		02.18	04.18	oe	
		02.20	04.20	oe	
		02.22	04.22	oe	
		02.24	04.24	oe	
		02.26	04.26	oe	
01.28	rd/be	02.28			
F.20	gy	02.28			
		02.30	04.30	gn	
		02.32	04.32	gn	

Table 13.4 CSR panel EF. Card No 2 connections
(Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
02.02	gy	03.02	04.02	gy	
		03.04	04.04	we	
02.06	be	03.06	04.06	be	-12 V
02.08	rd	03.08	04.08	rd	+ 6 V
01.10	gn	03.10	05.10	gn	
01.12	gn	03.12	05.12	gn	
01.14	gn	03.14	05.14	gn	
02.16	bk	03.16	04.16	bk	0 V
01.18	oe	03.18	05.18	oe	
01.20	oe	03.20	05.20	oe	
01.22	oe	03.22	05.22	oe	
01.24	oe	03.24	05.24	oe	
01.26	oe	03.26	05.26	oe	
		03.28	03.34	vt/we	
		03.28	04.28	rd/be	
01.30	gn	03.30	05.30	gn	
01.32	gn	03.32	05.32	gn	

Table 13.5 CSR panel EF. Card No 3 connections
(Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
03.02	gy	04.02	05.02	gy	
03.04	we	04.04			
E.13	we	04.04			
03.06	be	04.06	05.06	be	-12 V
03.08	rd	04.08	05.08	rd	+ 6 V
02.10	gn	04.10	06.10	gn	
02.12	gn	04.12	06.12	gn	
02.14	gn	04.14	06.14	gn	
03.16	bk	04.16	05.16	bk	0 V
02.18	oe	04.18	06.18	oe	
02.20	oe	04.20	06.20	oe	
02.22	oe	04.22	06.22	oe	
02.24	oe	04.24	06.24	oe	
02.26	oe	04.26	06.26	oe	
03.28	rd/be	04.28			
F.21	vt/we	04.28			
02.30	gn	04.30	06.30	gn	
02.32	gn	04.32	06.32	gn	

Table 13.6 CSR panel EF. Card No 4 connections
(Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
04.02	gy	05.02	06.02	gy	
		05.04	06.04	we	
04.06	be	05.06	06.06	be	-12 V
04.08	rd	05.08	06.08	rd	+ 6 V
03.10	gn	05.10	07.10	gn	
03.12	gn	05.12	07.12	gn	
03.14	gn	05.14	07.14	gn	
04.16	bk	05.16	06.16	bk	0 V
03.18	oe	05.18	07.18	oe	
03.20	oe	05.20	07.20	oe	
03.22	oe	05.22	07.22	oe	
03.24	oe	05.24	07.24	oe	
03.26	oe	05.26	07.26	oe	
		05.28	05.34	vt/we	
		05.28	06.28	rd/be	
03.30	gn	05.30	07.30	gn	
03.32	gn	05.32	07.32	gn	

Table 13.7 CSR panel EF. Card No 5 connections
(Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
05.02	gy	06.02	07.02	gy	
05.04	we	06.04			
E.14	we	06.04			
05.06	be	06.06	07.06	be	-12 V
05.08	rd	06.08	07.08	rd	+ 6 V
04.10	gn	06.10	08.10	gn	
04.12	gn	06.12	08.12	gn	
04.14	gn	06.14	08.14	gn	
05.16	bk	06.16	07.16	bk	0 V
04.18	oe	06.18	08.18	oe	
04.20	oe	06.20	08.20	oe	
04.22	oe	06.22	08.22	oe	
04.24	oe	06.24	08.24	oe	
04.26	oe	06.26	08.26	oe	
05.28	rd/be	06.28			
F.22	rd/be	06.28			
04.30	gn	06.30	08.30	gn	
04.32	gn	06.32	08.32		

Table 13.8 CSR panel EF. Card No 6 connections
(Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
06.02	gy	07.02	08.02	gy	
		07.04	08.04	we	
06.06	be	07.06	08.06	be	-12 V
06.08	rd	07.08	08.08	rd	+ 6 V
05.10	gn	07.10	09.10	gn	
05.12	gn	07.12	09.12	gn	
05.14	gn	07.14	09.14	gn	
06.16	bk	07.16	08.16	bk	0 V
05.18	oe	07.18	09.18	oe	
05.20	oe	07.20	09.20	oe	
05.22	oe	07.22	09.22	oe	
05.24	oe	07.24	09.24	oe	
05.26	oe	07.26	09.26	oe	
		07.28	07.34	vt/we	
		07.28	08.28	rd/be	
05.30	gn	07.30	09.30	gn	
05.32	gn	07.32	09.32	gn	

Table 13.9 CSR panel EF. Card No 7 connections
(Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
07.02	gy	08.02	09.02	gy	
07.04	we	08.04			
E.15	we	08.04			
07.06	be	08.06	09.06	be	-12 V
07.08	rd	08.08	09.08	rd	+ 6 V
06.10	gn	08.10	10.10	gn	
06.12	gn	08.12	10.12	gn	
06.14	gn	08.14	10.14	gn	
07.16	bk	08.16	09.16	bk	0 V
06.18	oe	08.18	10.18	oe	
06.20	oe	08.20	10.20	oe	
06.22	oe	08.22	10.22	oe	
06.24	oe	08.24	10.24	oe	
06.26	oe	08.26	10.26	oe	
07.28	rd/be	08.28			
F.23	oe	08.28			
06.30	gn	08.30	10.30	gn	
06.32	gn	08.32	10.32	gn	

Table 13.10 CSR panel EF. Card No 8 connections
(Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
08.02	gy	09.02	10.02	gy	
		09.04	10.04	we	
08.06	be	09.06	10.06	be	-12 V
08.08	rd	09.08	10.08	rd	+ 6 V
07.10	gn	09.10	11.10	gn	
07.12	gn	09.12	11.12	gn	
07.14	gn	09.14	11.14	gn	
08.16	bk	09.16	10.16	bk	0 V
07.18	oe	09.18	11.18	oe	
07.20	oe	09.20	11.20	oe	
07.22	oe	09.22	11.22	oe	
07.24	oe	09.24	11.24	oe	
07.26	oe	09.26	11.26	oe	
		09.28	09.34	vt/we	
		09.28	10.28	rd/be	
07.30	gn	09.30	11.30	gn	
07.32	gn	09.32	11.32	gn	

Table 13.11 CSR panel EF. Card No 9 connections
(Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
09.02	gy	10.02	11.02	gy	
09.04	we	10.04			
E.16	we	10.04			
09.06	be	10.06	11.06	be	-12 V
09.08	rd	10.08	11.08	rd	+ 6 V
08.10	gn	10.10	12.10	gn	
08.12	gn	10.12	12.12	gn	
08.14	gn	10.14	12.14	gn	
09.16	bk	10.16	11.16	bk	0 V
08.18	oe	10.18	12.18	oe	
08.20	oe	10.20	12.20	oe	
08.22	oe	10.22	12.22	oe	
08.24	oe	10.24	12.24	oe	
08.26	oe	10.26	12.26	oe	
09.28	rd/be	10.28			
F.24	we	10.28			
08.30	gn	10.30	12.30	gn	
08.32	gn	10.32	12.32	gn	

Table 13.12 CSR panel EF. Card No 10 connections
(Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
10.02	gy	11.02	12.02	gy	
		11.04	12.04	we	
10.06	be	11.06	12.06	be	-12 V
10.08	rd	11.08	12.08	rd	+ 6 V
09.10	gn	11.10	13.10	gn	
09.12	gn	11.12	13.12	gn	
09.14	gn	11.14	13.14	gn	
10.16	bk	11.16	12.16	bk	0 V
09.18	oe	11.18	13.18	oe	
09.20	oe	11.20	13.20	oe	
09.22	oe	11.22	13.22	oe	
09.24	oe	11.24	13.24	oe	
09.26	oe	11.26	13.26	oe	
		11.28	11.34	vt/we	
		11.28	12.28	rd/be	
09.30	gn	11.30	13.30	gn	
09.32	gn	11.32	13.32	gn	

Table 13.13 CSR panel EF. Card No 11 connections
(Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
11.02	gy	12.02	13.02	gy	
11.04	we	12.04			
E.17	we	12.04			
11.06	be	12.06	13.06	be	-12 V
11.08	rd	12.08	13.08	rd	+ 6 V
10.10	gn	12.10	14.10	gn	
10.12	gn	12.12	14.12	gn	
10.14	gn	12.14	14.14	gn	
11.16	bk	12.16	13.16	bk	0 V
10.18	oe	12.18	14.18	oe	
10.20	oe	12.20	14.20	oe	
10.22	oe	12.22	14.22	oe	
10.24	oe	12.24	14.24	oe	
10.26	oe	12.26	14.26	oe	
11.28	rd/be	12.28			
F.25	gn	12.28			
10.30	gn	12.30	14.30	gn	
10.32	gn	12.32	14.32	gn	

Table 13.14 CSR panel EF. Card No 12 connections
(Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
12.02	gy	13.02	14.02	gy	
		13.04	14.04	we	
12.06	be	13.06	14.06	be	-12 V
12.08	rd	13.08	14.08	rd	+ 6 V
11.10	gn	13.10	15.10	gn	
11.12	gn	13.12	15.12	gn	
11.14	gn	13.14	15.14	gn	
12.16	bk	13.16	14.16	bk	0 V
11.18	oe	13.18	15.18	oe	
11.20	oe	13.20	15.20	oe	
11.22	oe	13.22	15.22	oe	
11.24	oe	13.24	15.24	oe	
11.26	oe	13.26	15.26	oe	
		13.28	13.34	vt/we	
		13.28	14.28	rd/be	
11.30	gn	13.30	15.30	gn	
11.32	gn	13.32	15.32	gn	

Table 13.15 CSR panel EF. Card No 13 connections
(Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
13.02	gy	14.02	15.02	gy	
13.04	we	14.04			
E.18	we	14.04			
13.06	be	14.06	15.06	be	-12 V
13.08	rd	14.08	15.08	rd	+ 6 V
12.10	gn	14.10	16.10	gn	
12.12	gn	14.12	16.12	gn	
12.14	gn	14.14	16.14	gn	
13.16	bk	14.16	15.16	bk	0 V
12.18	oe	14.18	16.18	oe	
12.20	oe	14.20	16.20	oe	
12.22	oe	14.22	16.22	oe	
12.24	oe	14.24	16.24	oe	
12.26	oe	14.26	16.26	oe	
13.28	rd/be	14.28			
F.26	gy	14.28			
12.30	gn	14.30	16.30	gn	
12.32	gn	14.32	16.32	gn	

Table 13.16 CSR panel EF. Card No 14 connections
(Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
14.02	gy	15.02	16.02	gy	
		15.04	16.04	we	
14.06	be	15.06	16.06	be	-12 V
14.08	rd	15.08	16.08	rd	+ 6 V
13.10	gn	15.10	17.10	gn	
13.12	gn	15.12	17.12	gn	
13.14	gn	15.14	17.14	gn	
14.16	bk	15.16	16.16	bk	0 V
13.18	oe	15.18	17.18	oe	
13.20	oe	15.20	17.20	oe	
13.22	oe	15.22	17.22	oe	
13.24	oe	15.24	17.24	oe	
13.26	oe	15.26	17.26	oe	
		15.28	15.34	vt/we	
		15.28	16.28	rd/be	
13.30	gn	15.30	17.30	gn	
13.32	gn	15.32	17.32	gn	

Table 13.17 CSR panel EF. Card No 15 connections
(Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
15.02	gy	16.02	17.02	gy	
15.04	we	16.04			
E.19	we	16.04			
15.06	be	16.06	17.06	be	-12 V
15.08	rd	16.08	17.08	rd	+ 6 V
14.10	gn	16.10	18.10	gn	
14.12	gn	16.12	18.12	gn	
14.14	gn	16.14	18.14	gn	
15.16	bk	16.16	17.16	bk	0 V
14.18	oe	16.18	18.18	oe	
14.20	oe	16.20	18.20	oe	
14.22	oe	16.22	18.22	oe	
14.24	oe	16.24	18.24	oe	
14.26	oe	16.26	18.26	oe	
15.28	rd/be	16.28			
F.27	vt/we	16.28			
14.30	gn	16.30	18.30	gn	
14.32	gn	16.32	18.32	gn	

Table 13.18 CSR panel EF. Card No 16 connections
(Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
16.02	gy	17.02	18.02	gy	
		17.04	18.04	we	
16.06	be	17.06	18.06	be	-12 V
16.08	rd	17.08	18.08	rd	+ 6 V
15.10	gn	17.10			
E.04	gn	17.10			
15.12	gn	17.12			
E.03	gn	17.12			
15.14	gn	17.14			
E.02	gn	17.14			
16.16	bk	17.16	18.16	bk	0 V
15.18	oe	17.18			
E.21	oe	17.18			
15.20	oe	17.20			
E.22	oe	17.20			
15.22	oe	17.22			
E.23	oe	17.22			
15.24	oe	17.24			
E.24	oe	17.24			
15.26	oe	17.26			
E.25	oe	17.26			
		17.28	17.34	vt/we	
		17.28	18.28	rd/be	
15.30	gn	17.30			
E.06	gn	17.30			
15.32	gn	17.32			
E.05	gn	17.32			

Table 13.19 CSR panel EF. Card No 17 connections
(Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
17.02	gy	18.02			
E.31	vt/we	18.02			
17.04	we	18.04			
E.20	we	18.04			
17.06	be	18.06			-12 V
E.32	be	18.06			
17.08	rd	18.08			+ 6 V
E.34	rd	18.08			
16.10	gn	18.10			
E.09	gn	18.10			
16.12	gn	18.12			
E.08	gn	18.12			
16.14	gn	18.14			
E.07	gn	18.14			
17.16	bk	18.16	19.08	bk	0 V
16.18	oe	18.18			
E.26	oe	18.18			
16.20	oe	18.20			
E.27	oe	18.20			
16.22	oe	18.22			
E.28	oe	18.22			
16.24	oe	18.24			
E.29	oe	18.24			
16.26	oe	18.26			
E.30	oe	18.26			
17.28	rd/be	18.28			
F.28	rd/be	18.28			
16.30	gn	18.30			
E.11	gn	18.30			
16.32	gn	18.32			
E.10	gn	18.32			

Table 13.20 CSR panel EF. Card No 18 connections
(Card type DAF 3/8)

From	Colour	Terminal	To	Colour	Note
F.11	oe	19.02			} 120 VAC
F.10	rd/be	19.04			
		19.06	19.16	bk	
18.16	bk	19.08	19.14	bk	
		19.14	19.24	bk	
F.13	vt/we	19.22	19.20	vt/we	+50 V
E.33	bk	19.24	19.14	bk	0 V

Table 13.21 CSR panel EF. Card No 19 connections
(Card type DAF 11/13)

From	Colour	Terminal	To	Colour	Note
E. 02	gn	G. 02	17. 32	gn	Select W1
E. 03	gy	G. 03	17. 30	gy	" W2
E. 04	gn	G. 04	18. 32	gn	" W3
E. 05	gy	G. 05	18. 30	gy	" W4
E. 06	gn	G. 06	19. 32	gn	" W5
E. 07	gy	G. 07	19. 30	gy	" W6
E. 08	gn	G. 08	20. 32	gn	" W7
E. 09	gy	G. 09	20. 30	gy	" W8
E. 10	gn	G. 10	21. 32	gn	" W9
E. 11	gy	G. 11	21. 30	gy	" W10
E. 12	oe	G. 12	17. 12	oe	Set φ1
E. 13	vt/we	G. 13	17. 10	vt/we	" φ2
E. 14	oe	G. 14	18. 12	oe	" φ3
E. 15	vt/we	G. 15	18. 10	vt/we	" φ4
E. 16	oe	G. 16	19. 12	oe	" φ5
E. 17	vt/we	G. 17	19. 10	vt/we	" φ6
E. 18	oe	G. 18	20. 12	oe	" φ7
E. 19	vt/we	G. 19	20. 10	vt/we	" φ8
E. 20	oe	G. 20	21. 12	oe	" φ9
E. 21	we	G. 21	17. 08	we	Read W1
E. 22	rd/be	G. 22	17. 24	rd/be	" W2
E. 23	we	G. 23	18. 08	we	" W3
E. 24	rd/be	G. 24	18. 24	rd/be	" W4
E. 25	we	G. 25	19. 08	we	" W5
E. 26	rd/be	G. 26	19. 24	rd/be	" W6
E. 27	we	G. 27	20. 08	we	" W7
E. 28	rd/be	G. 28	20. 24	rd/be	" W8
E. 29	we	G. 29	21. 08	we	" W9
E. 30	rd/be	G. 30	21. 24	rd/be	" W10
E. 31	vt/we	G. 31	10. 32	vt/we	Erase
I. 32	be	G. 32	22. 12	be	-12 V
gnd	bk	G. 33	22. 04	bk	0 V
I. 34	rd	G. 34	22. 14	rd	+ 6 V

Table 14. 1 CSR panel GH. Plug G connections
(Plug card type DAF 1/2/12)

From	Colour	Terminal	To	Colour	Note
X. 31	gy	H. 02	17. 17	gy	Suppress W1
X. 32	oe	H. 03	17. 34	oe	" W2
X. 33	we	H. 04	18. 17	we	" W3
X. 34	rd/be	H. 05	18. 34	rd/be	" W4
X. 35	vt/we	H. 06	19. 17	vt/we	" W5
X. 36	gy	H. 07	19. 34	gy	" W6
X. 37	oe	H. 08	20. 17	oe	" W7
X. 38	we	H. 09	20. 34	we	" W8
X. 39	rd/be	H. 10	21. 17	rd/be	" W9
X. 40	vt/we	H. 11	21. 34	vt/we	" W10
B. 02	gy	H. 17	17. 07	vt/we	Read W1
L. 17	gy	H. 17			
B. 03	vt/we	H. 18	17. 22	rd/be	Read W2
L. 18	vt/we	H. 18			
B. 04	rd/be	H. 19	18. 07	oe	Read W3
L. 19	rd/be	H. 19			
B. 05	oe	H. 20	18. 22	we	Read W4
L. 20	oe	H. 20			
B. 06	we	H. 21	19. 07	gn	Read W5
L. 21	we	H. 21			
B. 07	gn	H. 22	19. 22	gy	Read W6
L. 22	gn	H. 22			
B. 08	gy	H. 23	20. 07	vt/we	Read W7
L. 23	gy	H. 23			
B. 09	vt/we	H. 24	20. 22	rd/be	Read W8
L. 24	vt/we	H. 24			
B. 10	rd/be	H. 25	21. 07	oe	Read W9
L. 25	rd/be	H. 25			
B. 11	we	H. 26	21. 22	we	Read W10
L. 26	we	H. 26			
SW5. 03	oe	H. 27	06. 06	oe	Rx input
SW1. 13b	rd/be	H. 28	21. 20	rd/be	Select station
Y. 39	rd/be	H. 29	22. 06	rd/be	Z
Y. 38	vt/we	H. 30	22. 08	vt/we	T
Y. 37	gn	H. 31	22. 10	gn	A
Y. 36	gy	H. 32	22. 28	gy	TTY sig
Y. 40	oe	H. 33	22. 26	oe	TTY sig
SW3. 1a	we	H. 34	22. 32	we	

Table 14. 2 CSR panel GH. Plug H connections
(Plug card type DAF 1/2/13)

From	Colour	Terminal	To	Colour	Note
		01.02	02.06	rd	+ 6 V
		01.04	02.02	be	-12 V
		01.10	01.24	we	
		01.22	01.32	we	
		01.22	01.18	we	
		01.28	15.16	we	
		01.30	02.34	bk	0 V
		01.34	02.16	we	
		01.34	04.10	we	

Table 14.3 CSR panel GH. Card No 1 connections
(Card type DAF 2/3)

From	Colour	Terminal	To	Colour	Note
01.04	be	02.02	03.02	be	-12 V
01.02	rd	02.06	03.06	rd	+ 6 V
		02.09	04.17	vt/we	B
		02.09	02.32	we	
		02.10	07.30	rd/be	
		02.11	04.08	oe	$\overline{B}$
		02.13	02.12	oe	
		02.15	07.06	we	$\overline{A}$
		02.15	04.09	gy	
01.34	we	02.16			
		02.20	07.08	vt/we	C
		02.20	04.07	we	
		02.23	04.26	gy	$\overline{D}$
		02.23	07.10	rd/be	
		02.26	02.24	vt/we	
01.30	bk	02.34	03.34	bk	0 V

Table 14.4 CSR panel GH. Card No 2 connections
(Card type DAF 2/14)

From	Colour	Terminal	To	Colour	Note
02.02	be	03.02	04.02	be	-12 V
02.06	rd	03.06	06.02	rd	+ 6 V
		03.09	05.12	rd/be	
		03.10	03.28	gy	
		03.13	03.12	oe	
		03.14	03.10	rd/be	
		03.15	05.11	vt/we	
		03.16	08.14	gy	
		03.20	03.24	we	
		03.20	05.13	gy	
		03.21	05.28	rd/be	
		03.21	05.14	oe	
		03.22	16.28	we	
		03.23	05.18	we	
		03.28	03.22	oe	
		03.30	05.29	gy	
		03.32	07.28	vt/we	
02.34	bk	03.34	06.34	bk	0 V

Table 14.5 CSR panel GH. Card No 3 connections
(Card type DAF 2/14)

From	Colour	Terminal	To	Colour	Note
03.02	be	04.02	05.02	be	-12 V
		04.03	07.22	gy	$S\bar{A}\bar{B}CD$
		04.04	07.24	oe	SACD
		04.05	07.26	we	$AB\bar{C}D$
		04.06	07.12	rd/be	D
		04.06	04.14	gy	D
02.20	we	04.07	04.13	rd/be	C
02.11	oe	04.08	04.28	we	$\bar{B}$
02.15	gy	04.09	05.10	gy	$\bar{A}$
01.34	we	04.10	04.11	rd/be	S
		04.11	05.06	vt/we	
		04.12	07.16	vt/we	A
		04.12	04.16	rd/be	
		04.14	04.19	oe	D
		04.16	04.29	gy	A
02.09	vt/we	04.17	05.09	oe	B
		04.18	07.14	we	$\bar{C}$
		04.18	04.27	vt/we	
		04.19	05.07	we	D
		04.21	04.22	oe	$A\bar{B}\bar{C}\bar{D}$
		04.21	15.22	vt/we	
		04.24	04.34	rd/be	
		04.24	16.26	rd/be	
02.23	gy	04.26			$\bar{D}$
		04.27	05.08	rd/be	$\bar{C}$
		04.30	08.12	gy	
		04.31	08.30	oe	

Table 14.6 CSR panel GH. Card No 4 connections
(Card type DAF 3/9)

From	Colour	Terminal	To	Colour	Note
04.02	be	05.02	06.04	be	-12 V
		05.03	15.24	oe	$\bar{A}B\bar{C}D$
		05.04	15.08	oe	
		05.05	10.22	we	
04.11	vt/we	05.06			
04.19	we	05.07			
04.27	rd/be	05.08			
04.17	oe	05.09			
04.09	gy	05.10			
03.15	vt/we	05.11	05.16	we	
03.09	rd/be	05.12			
03.20	gy	05.13	05.17	vt/we	
03.21	oe	05.14			
03.23	we	05.18			
		05.19	09.21	rd/be	
		05.20	15.12	gy	
		05.22	05.34	vt/we	
		05.27	08.12	oe	
03.21	rd/be	05.28			
03.30	gy	05.29			
		05.34	15.26	gy	

Table 14.7 CSR panel GH. Card No 5 connections
(Card type DAF 3/9)

From	Colour	Terminal	To	Colour	Note
03.06	rd	06.02	07.02	rd	+ 6 V
05.02	be	06.04	07.04	be	-12 V
		06.05	11.15	vt/we	
H.27	oe	06.06			
		06.08	14.30	gy	
		06.10	14.11	oe	
		06.12	10.03	oe	
		06.14	10.02	gy	
		06.16	09.16	rd/be	
		06.22	14.16	we	
		06.24	13.25	vt/we	
		06.26	13.30	rd/be	
		06.28	10.06	rd/be	
		06.30	10.05	vt/we	
		06.32	10.04	we	
03.34	bk	06.34	07.34	bk	0 V

Table 14.8 CSR panel GH. Card No 6 connections
(Card type DAF 3/10)

From	Colour	Terminal	To	Colour	Note
06.02	rd	07.02	08.02	rd	+ 6 V
06.04	be	07.04	08.03	be	-12 V
02.15	we	07.06			
02.20	vt/we	07.08			
02.23	rd/be	07.10			
04.06	rd/be	07.12			
04.18	we	07.14			
04.12	vt/we	07.16	08.22	oe	
04.03	gy	07.22			
04.04	oe	07.24			
04.05	we	07.26			
03.32	vt/we	07.28			
02.10	rd/be	07.30	09.13	vt/we	
		07.32	08.10	gy	
06.34	bk	07.34	08.35	bk	0 V

Table 14.9 CSR panel GH. Card No 7 connections
(Card type DAF 3/10)

From	Colour	Terminal	To	Colour	Note
07.02	rd	08.02	09.06	rd	+ 6 V
07.04	be	08.03	09.05	be	-12 V
		08.08	11.07	gy	
07.32	gy	08.10	09.25	rd/be	
04.30	gy	08.12			
05.27	oe	08.12			
03.16	gy	08.14			
07.16	oe	08.22			
		08.24	09.21	gn	
		08.26	11.14	vt/we	
		08.28	11.03	rd/be	
04.31	oe	08.30			
		08.31	08.06	oe	
		08.32	09.02	gy	
		08.33	08.18	bk	
07.34	bk	08.35	09.35	bk	0 V

Table 14.10 CSR panel GH. Card No 8 connections
(Card type DAF 2/16)

From	Colour	Terminal	To	Colour	Note
08.32	gy	09.02			
08.03	be	09.05	10.18	be	-12 V
08.02	rd	09.06	10.20	rd	+ 6 V
		09.08	09.30	we	
		09.08	15.30	oe	
		09.09	09.19	bk	
		09.11	15.32	oe	
		09.12	09.09	bk	
07.30	vt/we	09.13			
		09.14	09.33	bk	
		09.15	15.06	gy	
06.16	rd/be	09.16			
		09.17	16.10	vt/we	
05.19	rd/be	09.21			
08.24	gn	09.21			
		09.22	16.22	gn	
		09.23	16.22	vt/we	
		09.24	16.12	rd/be	
08.10	rd/be	09.25			
		09.26	09.18	bk	
		09.28	09.11	gy	
		09.29	09.18	bk	
		09.30	15.10	rd/be	
		09.31	15.14	gy	
		09.33	09.19	bk	
		09.34	15.28	rd/be	
08.35	bk	09.35	10.34	bk	0 V

Table 14.11 CSR panel GH. Card No 9 connections
(Card type DAF 2/12)

From	Colour	Terminal	To	Colour	Note
06.14	gy	10.02			
06.12	oe	10.03			
06.32	we	10.04			
06.30	vt/we	10.05			
06.28	rd/be	10.06			
		10.07	17.26	we	
		10.08	17.28	vt/we	
		10.10	18.26	rd/be	
		10.11	18.28	gy	
		10.12	19.26	oe	
		10.13	19.28	we	
		10.14	20.26	vt/we	
		10.15	20.28	rd/be	
		10.16	21.26	gy	
		10.17	21.28	oe	
09.05	be	10.18	11.05	be	-12 V
09.06	rd	10.20	11.06	rd	+ 6 V
05.05	we	10.22			
		10.26	17.14	we	
G.31	vt/we	10.32			
09.35	bk	10.34	11.35	bk	0 V

Table 14.12 CSR panel GH. Card No 10 connections
(Card type DAF 3/6)

From	Colour	Terminal	To	Colour	Note
08.28	rd/be	11.03	16.06	vt/we	
10.18	be	11.05	12.05	be	-12 V
10.20	rd	11.06	12.06	rd	+ 6 V
08.08	gy	11.07			
		11.08	11.31	gy	
		11.08	17.04	rd/be	
		11.11	11.27	oe	
		11.13	11.02	be	
08.26	vt/we	11.14			
06.05	vt/we	11.15			
		11.17	11.19	bk	
		11.21	17.05	gy	
		11.22	18.04	oe	
		11.22	12.17	we	
		11.25	12.13	vt/we	
10.34	bk	11.35	12.35	bk	0 V

Table 14.13 CSR panel GH. Card No 11 connections
(Card type DAF 2/13)

From	Colour	Terminal	To	Colour	Note
		12.03	13.03	we	
11.05	be	12.05	13.05	be	-12 V
11.06	rd	12.06	13.06	rd	+ 6 V
		12.07	18.05	we	
		12.08	12.31	vt/we	
		12.08	19.04	vt/we	
		12.11	12.27	rd/be	
11.25	vt/we	12.13			
11.22	we	12.17			
		12.21	19.05	rd/be	
		12.22	20.04	gy	
		12.22	13.17	gy	
		12.25	13.13	oe	
11.35	bk	12.35	13.35	bk	0 V

Table 14.14 CSR panel GH. Card No 12 connections
(Card type DAF 2/13)

From	Colour	Terminal	To	Colour	Note
12.03	we	13.03	14.03	oe	
12.05	be	13.05	14.05	be	-12 V
12.06	rd	13.06	14.06	rd	+ 6 V
		13.07	20.05	oe	
		13.08	21.04	we	
		13.08	13.31	we	
		13.11	13.27	vt/we	
12.25	oe	13.13			
12.22	gy	13.17			
		13.22	14.17	rd/be	
06.24	vt/we	13.25	14.13	gy	
06.26	rd/be	13.30			
12.35	bk	13.35	14.35	bk	0 V

Table 14.15 CSR panel GH. Card No 13 connections
(Card type DAF 2/13)

From	Colour	Terminal	To	Colour	Note
13.03	oe	14.03			
13.05	be	14.05	15.04	be	-12 V
13.06	rd	14.06	15.02	rd	+ 6 V
		14.08	14.31	vt/we	
06.10	oe	14.11	14.27	rd/be	
13.25	gy	14.13			
06.22	we	14.16			
13.22	rd/be	14.17			
06.08	gy	14.30			
		14.34	16.24	bk	
13.35	bk	14.35	15.34	bk	0 V

Table 14.16 CSR panel GH. Card No 14 connections
(Card type DAF 2/13)

From	Colour	Terminal	To	Colour	Note
14.06	rd	15.02	16.02	rd	+ 6 V
14.05	be	15.04	16.04	be	-12 V
09.15	gy	15.06			
05.04	oe	15.08			
09.30	rd/be	15.10			
05.20	gy	15.12			
09.31	gy	15.14			
01.28	we	15.16			
04.21	vt/we	15.22			
05.03	oe	15.24			
05.34	gy	15.26			
09.34	rd/be	15.28			
09.08	oe	15.30			
09.11	oe	15.32			
14.35	bk	15.34	16.18	bk	0 V

Table 14.17 CSR panel GH. Card No 15 connections
(Card type DAF 3/10)

From	Colour	Terminal	To	Colour	Note
15.02	rd	16.02	17.02	rd	+ 6 V
15.04	be	16.04	17.03	be	-12 V
11.03	vt/we	16.06			
		16.08	16.20	oe	
09.17	vt/we	16.10			
09.24	rd/be	16.12			
15.34	bk	16.18	17.18	bk	0 V
09.22	gn	16.22			
09.23	vt/we	16.22			
04.24	rd/be	16.26			
03.22	we	16.28			
14.34	bk	16.34			

Table 14.18 CSR panel GH. Card No 16 connections
(Card type DAF 3/11)

From	Colour	Terminal	To	Colour	Note
16.02	rd	17.02	18.02	rd	+ 6 V
16.04	be	17.03	18.03	be	-12 V
11.08	rd/be	17.04			
11.21	gy	17.05			
		17.06	17.20	oe	
H.17	vt/we	17.07			
G.21	we	17.08			
G.13	vt/we	17.10			
G.12	oe	17.12			
10.26	we	17.14	17.16	gy	
		17.16	18.14	gy	
H.02	gy	17.17			
16.18	bk	17.18	18.18	bk	0 V
		17.20	18.06	oe	
H.18	rd/be	17.22			
G.22	rd/be	17.24			
10.07	we	17.26			
10.08	vt/we	17.28			
G.03	gy	17.30			
G.02	gn	17.32			
H.03	oe	17.34			

Table 14.19 CSR panel GH. Card No 17 connections
(Card type DAF 3/7)

From	Colour	Terminal	To	Colour	Note
17.02	rd	18.02	19.02	rd	+ 6 V
17.03	be	18.03	19.03	be	-12 V
11.22	oe	18.04			
12.07	we	18.05			
17.20	oe	18.06	18.20	oe	
H.19	oe	18.07			
G.23	we	18.08			
G.15	vt/we	18.10			
G.14	oe	18.12			
17.16	gy	18.14	18.16	gy	
		18.16	19.14	gy	
H.04	we	18.17			
17.18	bk	18.18	19.18	bk	0 V
		18.20	19.06	oe	
H.20	we	18.22			
G.24	rd/be	18.24			
10.10	rd/be	18.26			
10.11	gy	18.28			
G.05	gy	18.30			
G.04	gn	18.32			
H.05	rd/be	18.34			

Table 14.20 CSR panel GH. Card No 18 connections
(Card type DAF 3/7)

From	Colour	Terminal	To	Colour	Note
18.02	rd	19.02	20.02	rd	+ 6 V
18.03	be	19.03	20.03	be	-12 V
12.08	vt/we	19.04			
12.21	rd/be	19.05			
18.20	oe	19.06	19.20	oe	
H.21	gn	19.07			
G.25	we	19.08			
G.17	vt/we	19.10			
G.16	oe	19.12			
18.16	gy	19.14	19.16	gy	
		19.16	20.14	gy	
H.06	vt/we	19.17			
18.18	bk	19.18	20.18	bk	0 V
		19.20	20.06	oe	
H.22	gy	19.22			
G.26	rd/be	19.24			
10.12	oe	19.26			
10.13	we	19.28			
G.07	gy	19.30			
G.06	gn	19.32			
H.07	gy	19.34			

Table 14.21 CSR panel GH. Card No 19 connections (Card type DAF 3/7)

From	Colour	Terminal	To	Colour	Note
19.02	rd	20.02	21.02	rd	+ 6 V
19.03	be	20.03	21.03	be	-12 V
12.22	gy	20.04			
13.07	oe	20.05			
19.20	oe	20.06	20.20	oe	
H.23	vt/we	20.07			
G.27	we	20.08			
G.19	vt/we	20.10			
G.18	oe	20.12			
19.16	gy	20.14	20.16	gy	
		20.16	21.14	gy	
H.08	oe	20.17			
19.18	bk	20.18	21.18	bk	0 V
		20.20	21.06	oe	
H.24	rd/be	20.22			
G.28	rd/be	20.24			
10.14	vt/we	20.26			
10.15	rd/be	20.28			
G.09	gy	20.30			
G.08	gn	20.32			
H.09	we	20.34			

Table 14.22 CSR panel GH. Card No 20 connections (Card type DAF 3/7)

From	Colour	Terminal	To	Colour	Note
20.02	rd	21.02	22.14	rd	+ 6 V
20.03	be	21.03	22.12	be	-12 V
13.08	we	21.04			
20.20	oe	21.06	21.20	oe	
H.25	oe	21.07			
G.29	we	21.08			
G.20	vt/we	21.12			
20.16	gy	21.14	21.16	gy	
H.10	rd/be	21.17			
20.18	bk	21.18	22.04	bk	0 V
H.28	rd/be	21.20			
H.26	we	21.22			
G.30	rd/be	21.24			
10.16	gy	21.26			
10.17	oe	21.28			
G.11	gy	21.30			
G.10	gn	21.32			
H.11	vt/we	21.34			

Table 14.23 CSR panel GH. Card No 21 connections (Card type DAF 3/7)

From	Colour	Terminal	To	Colour	Note
H.29	rd/be	22.06			Z
H.30	vt/we	22.08			T
H.31	gn	22.10			A
H.33	oe	22.26			TTY sig
H.32	gy	22.28			TTY sig
H.34	we	22.32			TTY to SW3
		22.22	22.24	vt/we	
G.33	bk	22.04			0 V
G.32	be	22.12			-12 V
G.34	rd	22.14			+ 6 V

Table 14.24 CSR panel GH. Card No 22 connections (Card type DAF 1/14)

From	Colour	Terminal	To	Colour	Note
X. 21	gy	L. 02	17. 17	gy	Suppress W1
X. 22	oe	L. 03	17. 34	oe	" W2
X. 23	we	L. 04	18. 17	we	" W3
X. 24	rd/be	L. 05	18. 34	rd/be	" W4
X. 25	vt/we	L. 06	19. 17	vt/we	" W5
X. 26	gy	L. 07	19. 34	gy	" W6
X. 27	oe	L. 08	20. 17	oe	" W7
X. 28	we	L. 09	20. 34	we	" W8
X. 29	rd/be	L. 10	21. 17	rd/be	" W9
X. 30	vt/we	L. 12	21. 34	vt/we	" W10
H. 17	gy	L. 17	17. 07	vt/we	Read W1
P. 17	gy	L. 17			
H. 18	vt/we	L. 18	17. 22	rd/be	Read W2
P. 18	vt/we	L. 18			
H. 19	rd/be	L. 19	18. 07	oe	Read W3
P. 19	rd/be	L. 19			
H. 20	oe	L. 20	18. 22	we	Read W4
P. 20	oe	L. 20			
H. 21	we	L. 21	19. 07	gn	Read W5
P. 21	we	L. 21			
H. 22	gn	L. 22	19. 22	gy	Read W6
P. 22	gn	L. 22			
H. 23	gy	L. 23	20. 07	vt/we	Read W7
P. 23	gy	L. 23			
H. 24	vt/we	L. 24	20. 22	rd/be	Read W8
P. 24	vt/we	L. 24			
H. 25	rd/be	L. 25	21. 07	oe	Read W9
P. 25	rd/be	L. 25			
H. 26	we	L. 26	21. 22	we	Read W10
P. 26	we	L. 26			
SW6. 03	oe	L. 27	06. 06	oe	Rx input
SW1. 26b	rd/be	L. 28	21. 20	rd/be	Select station
Y. 34	rd/be	L. 29	22. 06	rd/be	Z
Y. 33	vt/we	L. 30	22. 08	vt/we	A
Y. 32	gn	L. 31	22. 10	gn	T
Y. 31	gy	L. 32	22. 28	gy	TTY sig
Y. 35	oe	L. 33	22. 26	oe	TTY sig
SW3. 14a	we	L. 34	22. 32	we	

Table 16. 2 CSR panel KL. Plug L connections
(Plug card type DAF 1/2/13)

For CSR panel KL card No 1 - 22 connections use Tables 14. 3 - 14. 24. Read K instead of G, and L instead of H.

Tables 16. 3 - 16. 24 CSR panel KL. Card No 1 - 22 connections

From	Colour	Terminal	To	Colour	Note
O. 02	gn	M. 02	17. 14	gn	Select W1
O. 03	gy	M. 03	17. 12	gn	" W2
O. 04	gn	M. 04	17. 10	gn	" W3
O. 05	gy	M. 05	17. 32	gn	" W4
O. 06	gn	M. 06	17. 30	gn	" W5
O. 07	gy	M. 07	18. 14	gn	" W6
O. 08	gn	M. 08	18. 12	gn	" W7
O. 09	gy	M. 09	18. 10	gn	" W8
O. 10	gn	M. 10	18. 32	gn	" W9
O. 11	gy	M. 11	18. 30	gn	" W10
O. 12	oe	M. 12	02. 04	we	Set φ1
O. 13	vt/we	M. 13	04. 04	we	" φ2
O. 14	oe	M. 14	06. 04	we	" φ3
O. 15	vt/we	M. 15	08. 04	we	" φ4
O. 16	oe	M. 16	10. 04	we	" φ5
O. 17	vt/we	M. 17	12. 04	we	" φ6
O. 18	oe	M. 18	14. 04	we	" φ7
O. 19	vt/we	M. 19	16. 04	we	" φ8
O. 20	oe	M. 20	18. 04	we	" φ9
O. 21	we	M. 21	17. 18	oe	Read W1
O. 22	rd/be	M. 22	17. 20	oe	" W2
O. 23	we	M. 23	17. 22	oe	" W3
O. 24	rd/be	M. 24	17. 24	oe	" W4
O. 25	we	M. 25	17. 26	oe	" W5
O. 26	rd/be	M. 26	18. 18	oe	" W6
O. 27	we	M. 27	18. 20	oe	" W7
O. 28	rd/be	M. 28	18. 22	oe	" W8
O. 29	we	M. 29	18. 24	oe	" W9
O. 30	rd/be	M. 30	18. 26	oe	" W10
O. 31	vt/we	M. 31	18. 02	vt/we	Erase
A4. 02	be	M. 32	18. 06	be	-12 V
Q. 32	be	M. 32			-12 V
gnd	bk	M. 33	18. 16	bk	0 V
O. 34	rd	M. 34	18. 08	rd	+ 6 V

Table 17. 1 CSR panel MN. Plug M connections
(Plug card type DAF 1/2/14)

From	Colour	Terminal	To	Colour	Note
R. 20	gy	N. 20	02. 28	gy	φ1
R. 21	vt/we	N. 21	04. 28	vt/we	φ2
R. 22	rd/be	N. 22	06. 28	rd/be	φ3
R. 23	oe	N. 23	08. 28	oe	φ4
R. 24	we	N. 24	10. 28	we	φ5
R. 25	gn	N. 25	12. 28	gn	φ6
R. 26	gy	N. 26	14. 28	gy	φ7
R. 27	vt/we	N. 27	16. 28	vt/we	φ8
R. 28	rd/be	N. 28	18. 28	rd/be	φ9

Table 17. 2 CSR panel MN. Plug N connections
(Plug card type DAF 1/2/15)

For CSR panel MN card No 1 - 18 connections use Tables 13. 3 - 13. 20. Read M instead of E, and N instead of F.

Note: Omit connection 01. 28 - 01. 34 vt/we

Instead of connection 18. 16 - 19. 08 bk
read M. 33 - 18. 16 bk

Tables 17. 3 - 17. 20 CSR panel MN. Card No 1 - 18 connections

From	Colour	Terminal	To	Colour	Note
N. 02	gn	O. 02	17. 32	gn	Select W1
N. 03	gy	O. 03	17. 30	gn	" W2
N. 04	gn	O. 04	18. 32	gn	" W3
N. 05	gy	O. 05	18. 30	gn	" W4
N. 06	gn	O. 06	19. 32	gn	" W5
N. 07	gy	O. 07	19. 30	gn	" W6
N. 08	gn	O. 08	20. 32	gn	" W7
N. 09	gy	O. 09	20. 30	gn	" W8
N. 10	gn	O. 10	21. 32	gn	" W9
N. 11	gy	O. 11	21. 30	gn	" W10
N. 12	oe	O. 12	17. 12	oe	Set φ1
N. 13	vt/we	O. 13	17. 10	vt/we	" φ2
N. 14	oe	O. 14	18. 12	oe	" φ3
N. 15	vt/we	O. 15	18. 10	vt/we	" φ4
N. 16	oe	O. 16	19. 12	oe	" φ5
N. 17	vt/we	O. 17	19. 10	vt/we	" φ6
N. 18	oe	O. 18	20. 12	oe	" φ7
N. 19	vt/we	O. 19	20. 10	vt/we	" φ8
N. 20	oe	O. 20	21. 12	oe	" φ9
N. 21	we	O. 21	17. 08	we	Read W1
N. 22	rd/be	O. 22	17. 24	rd/be	" W2
N. 23	we	O. 23	18. 08	we	" W3
N. 24	rd/be	O. 24	18. 24	rd/be	" W4
N. 25	we	O. 25	19. 08	we	" W5
N. 26	rd/be	O. 26	19. 24	rd/be	" W6
N. 27	we	O. 27	20. 08	we	" W7
N. 28	rd/be	O. 28	20. 24	rd/be	" W8
N. 29	we	O. 29	21. 08	we	" W9
N. 30	rd/be	O. 30	21. 24	rd/be	" W10
N. 31	vt/we	O. 31	10. 32	vt/we	Erase
PS3. 05	be	O. 32	22. 12	be	-12 V
gnd	be	O. 33	22. 04	bk	0 V
Q. 34	rd	O. 34	22. 14	rd	+ 6 V

Table 18. 1 CSR panel OP. Plug O connections (Plug card type DAF 1/2/12)

From	Colour	Terminal	To	Colour	Note
X. 11	gy	P. 02	17. 17	gy	Suppress W1
X. 12	oe	P. 03	17. 34	oe	" W2
X. 13	we	P. 04	18. 17	we	" W3
X. 14	rd/be	P. 05	18. 34	rd/be	" W4
X. 15	vt/we	P. 06	19. 17	vt/we	" W5
X. 16	gy	P. 07	19. 34	gy	" W6
X. 17	oe	P. 08	20. 17	oe	" W7
X. 18	we	P. 09	20. 34	we	" W8
X. 19	rd/be	P. 10	21. 17	rd/be	" W9
X. 20	vt/we	P. 11	21. 34	vt/we	" W10
L. 17	gy	P. 17	17. 07	vt/we	Read W1
T. 17	gy	P. 17			
L. 18	vt/we	P. 18	17. 22	rd/be	Read W2
T. 18	vt/we	P. 18			
L. 19	rd/be	P. 19	18. 07	oe	Read W3
T. 19	rd/be	P. 19			
L. 20	oe	P. 20	18. 22	we	Read W4
T. 20	oe	P. 20			
L. 21	we	P. 21	19. 07	gn	Read W5
T. 21	we	P. 21			
L. 22	gn	P. 22	19. 22	gy	Read W6
T. 22	gn	P. 22			
L. 23	gy	P. 23	20. 07	vt/we	Read W7
T. 23	gy	P. 23			
L. 24	vt/we	P. 24	20. 22	rd/be	Read W8
T. 24	vt/we	P. 24			
L. 25	rd/be	P. 25	21. 07	oe	Read W9
T. 25	rd/be	P. 25			
L. 26	we	P. 26	21. 22	we	Read W10
T. 26	we	P. 26			
SW7. 03	oe	P. 27	06. 06	oe	Rx input
SW1. 13c	rd/be	P. 28	21. 20	rd/be	Select station
Y. 29	rd/be	P. 29	22. 06	rd/be	Z
Y. 28	vt/we	P. 30	22. 08	vt/we	A
Y. 27	we	P. 31	22. 10	gn	T
Y. 26	gy	P. 32	22. 28	gy	TTY sig
Y. 30	oe	P. 33	22. 26	oe	TTY sig
SW3. 1b	we	P. 34	22. 32	we	

Table 18. 2 CSR panel OP. Plug P connections
(Plug card type DAF 1/2/13)

For CSR panel OP card No 1 - 22 connections use tables 14. 3 - 14. 24. Read O instead of G, and P instead of H.

Tables 18. 3 - 18. 24 CSR panel OP. Card No 1 - 22 connections

From	Colour	Terminal	To	Colour	Note
X. 01	gy	T. 02	17.17	gy	Suppress W1
X. 02	oe	T. 03	17.34	oe	" W2
X. 03	we	T. 04	18.17	we	" W3
X. 04	rd/be	T. 05	18.34	rd/be	" W4
X. 05	vt/we	T. 06	19.17	vt/we	" W5
X. 06	gy	T. 07	19.34	gy	" W6
X. 07	oe	T. 08	20.17	oe	" W7
X. 08	we	T. 09	20.34	we	" W8
X. 09	rd/be	T. 10	21.17	rd/be	" W9
X. 10	vt/we	T. 11	21.34	vt/we	" W10
P. 17	gy	T. 17	17.07	vt/we	Read W1
P. 18	vt/we	T. 18	17.22	rd/be	" W2
P. 19	rd/be	T. 19	18.07	oe	" W3
P. 20	oe	T. 20	18.22	we	" W4
P. 21	we	T. 21	19.07	gn	" W5
P. 22	gn	T. 22	19.22	gy	" W6
P. 23	gy	T. 23	20.07	vt/we	" W7
P. 24	vt/we	T. 24	20.22	rd/be	" W8
P. 25	rd/be	T. 25	21.07	oe	" W9
P. 26	we	T. 26	21.22	we	" W10
SW8. 03	oe	T. 27	06.06	oe	Rx input
SW1. 26c	rd/be	T. 28	21.20	rd/be	Select station
Y. 24	rd/be	T. 29	22.06	rd/be	Z
Y. 23	vt/we	T. 30	22.08	vt/we	A
Y. 22	gn	T. 31	22.10	gn	T
Y. 21	gy	T. 32	22.28	gy	TTY sig
Y. 25	oe	T. 33	22.26	oe	TTY sig
SW3. 14a	we	T. 34	22.32	we	

Table 20. 2 CSR panel ST. Plug T connections
(Plug card type DAF 1/2/13)

For CSR panel ST card No 1 - 22 connections use Tables 14. 3 - 14. 23. Read S instead of G, and T instead of H.

Tables 20. 3 - 20. 24 CSR panel ST. Card No 1 - 22 connections

From	Colour	Terminal	To	Colour	Note
D. 10	gy	U. 02			$\alpha 9$
D. 09	oe	U. 03			$\alpha 8$
D. 08	gn	U. 04			$\alpha 7$
D. 07	vt/we	U. 05			$\alpha 6$
D. 06	rd/be	U. 06			$\alpha 5$
D. 05	we	U. 07			$\alpha 4$
D. 04	gy	U. 08			$\alpha 3$
D. 03	oe	U. 09			$\alpha 2$
D. 02	gn	U. 10			$\alpha 1$
B. 25	rd/be	U. 12			$\overline{S5}$
B. 24	we	U. 13			$\overline{S4}$
B. 23	vt/we	U. 14			$\overline{S3}$
B. 22	we	U. 15			$\overline{S2}$
B. 21	gn	U. 16			$\overline{S1}$
gnd	bk	U. 17			0 V
T1. 01	gn	U. 18			1. 2 VAC
F. 13	vt/we	U. 19			+50 V
VM1. 09	vt/we	U. 19			+50 V
		U. 20			0 V
B. 26	we	U. 21			$\overline{S6}$
B. 27	rd/be	U. 22			$\overline{S7}$
B. 28	we	U. 23			$\overline{S8}$
D. 11	we	U. 24			Q1
D. 12	rd/be	U. 25			Q2
C. 02	gn	U. 27			$\varphi 1$
C. 03	oe	U. 28			$\varphi 2$
C. 04	gy	U. 29			$\varphi 3$
C. 05	we	U. 30			$\varphi 4$
C. 06	rd/be	U. 31			$\varphi 5$
C. 07	vt/we	U. 32			$\varphi 6$
C. 08	gn	U. 33			$\varphi 7$
C. 09	oe	U. 34			$\varphi 8$
C. 10	gy	U. 35			$\varphi 9$

Table 21.1 CSR indicator card plug U connections (Card type DAF 15/16)

From	Colour	Terminal	To	Colour	Note
		SW1.03a			
		SW1.05a	SW1.07a	bk	
		SW1.07a	SW1.09a	bk	
		SW1.09a	SW1.11a	bk	
		SW1.11a		bk	0 V
B.29	gn	SW1.13a			
		SW1.16a			
		SW1.18a	SW1.20a	be	
		SW1.20a	SW1.22a	be	
		SW1.22a	SW1.24a	be	
		SW1.24a		be	-12 V
SW2.13		SW1.26a			
B.12	oe	SW1.03b			
		SW1.05b		bk	0 V
		SW1.07b	SW1.09b	be	
		SW1.09b	SW1.11b	be	
		SW1.11b		be	-12 V
H.28	rd/be	SW1.13b			
B.13	gn	SW1.16b			
		SW1.18b	SW1.22b	be	
		SW1.20b		bk	0 V
		SW1.22b	SW1.24b	be	
		SW1.24b		be	-12 V
L.28	rd/be	SW1.26b			
B.14	gy	SW1.03c			
		SW1.05c	SW1.07c	be	
		SW1.07c	SW1.11c	be	
		SW1.09c		bk	0 V
		SW1.11c		be	-12 V
P.28	rd/be	SW1.13c			
B.15	we	SW1.16c			
		SW1.18c	SW1.20c		
		SW1.20c	SW1.22c		
		SW1.22c			-12 V
		SW1.24c		bk	0 V
T.28	rd/be	SW1.26c			

Table 22.8a CSR switch SW1 connections (STATION SELECTOR)

From	Colour	Terminal	To	Colour	Note
		SW2.01	B.07	gn	
		SW2.03	B.08	gy	
		SW2.05	B.09	vt/we	
		SW2.07	B.10	rd/be	
		SW2.09	B.11	we	
SW1.26a		SW2.13			
		SW2.17	B.02	gy	
		SW2.19	B.03	vt/we	
		SW2.21	B.04	rd/be	
		SW2.23	B.05	oe	
		SW2.25	B.06	we	

Table 22.8b CSR switch SW2 connections (WORD SELECTOR)

From	Colour	Terminal	To	Colour	Note
H.34	we	SW3.01a	SW3.16a	we	Rx A
SW5.01	rd/be	SW3.13a			
L.34	we	SW3.14a			Rx B
SW3.01a	we	SW3.16a	SW3.05b	we	
SW6.01	we	SW3.26a			
P.34	we	SW3.01b			Rx C
SW3.16a	we	SW3.05b	SW3.20b	we	
SW7.01	gy	SW3.13b			
T.34	we	SW3.14b			Rx D
SW3.05b	we	SW3.20b			
SW8.01	gn	SW3.26b			

Table 22.8c CSR switch SW3 connections (LOCAL RECEIVER)

From	Colour	Terminal	To	Colour	Note
		SW4.05a	SW4.10a	bk	
C.31	vt/we	SW4.08a			Inhibit $\overline{P3}$
C.28	gy	SW4.08a			
SW4.05a	bk	SW4.10a	SW4.14a	bk	
SW4.10a	bk	SW4.14a	SW4.21a	bk	
C.29	we	SW4.17a			Inhibit $\overline{P2}$
SW4.14a	bk	SW4.21a	SW4.23a	bk	
SW4.21a	bk	SW4.23a	SW4.01b	bk	
C.30	rd/be	SW4.26a			Inhibit $\overline{P4}$
SW4.23a	bk	SW4.01b		bk	0 V
		SW4.03b	SW4.05b	be	
SW4.03b	be	SW4.05b		be	-12 V
D.21	gn	SW4.08b			Control reset
		SW4.12b	SW4.14b	bk	
SW4.12b	bk	SW4.14b			
A.20	vt/we	SW4.17b			

Table 22.8d CSR switch SW4 connections (SINE TABLE)

From	Colour	Terminal	To	Colour	Note
SW3.13a	rd/be	SW5.01			
D.33	rd/be	SW5.02			
		SW5.03	H.27	oe	Rx A
SW3.26a	vt/we	SW6.01			
D.32	vt/we	SW6.02			
		SW6.03	L.27	oe	Rx B
SW3.13b	gy	SW7.01			
D.31	gy	SW7.02			
		SW7.03	P.27	oe	Rx C
SW3.26b	gn	SW8.01			
D.34	gn	SW8.02			
		SW8.03	T.27	oe	Rx D

Table 22.8e CSR switches SW5, SW6, SW7, SW8 connections (NORMAL-SIMULATOR)

From	Colour	Terminal	To	Colour	Note
		SW9.01	A.21	gy	
		SW9.02	A.14	gn	
		SW9.03	D.23	rd/be	
		SW10.01	A.15	rd/be	
		SW10.02	A.16	gn	
		SW10.03	SW3.09b	bk	0 V
		SW11.01	SW1.18a	be	-12 V
		SW11.02	D.28	we	Reset
		SW13.1a	VC.01	we	
		SW13.1b	VC.02	bk	
		SW13.2a	Fuse 1	bk	
		SW13.2b	Fuse 2	bk	

Table 22.8f CSR switches SW9, SW10, SW11 and SW13 connections (NORM-MAN TRIG, TRIGGER, RESET, MAINS)