Improved passivation effect due to controlled smoothing of the CdTe-HgCdTe interface gradient by thermal annealing

R. Haakenaasen[1], E. Selvig, A. C. Heier, T. Lorentzen and L. Trosdahl-Iversen

FFI – Norwegian Defence Research Establishment, P.O. Box 25, NO-2027-Kjeller, Norway.
1.   e-mail: randi.haakenaasen@ffi.no, Phone: +47 63 80 73 09, Fax: +47 63 80 72 12

ABSTRACT

HgCdTe films grown by liquid phase epitaxy (LPE) were passivated with CdTe grown by molecular beam epitaxy (MBE). A series of annealing tests with different temperatures and durations were then carried out in order to reach a two-fold goal: to smooth the gradients in Hg and Cd content across the HgCdTe film-passivation interface, and to create a Hg-vacancy concentration of $\sim 1 - 2 \times 10^{16}$ cm^{-3}. We want the composition gradient to prevent minority carrier electrons from reaching the actual interface, as this may contain recombination centers that trap the electrons. Four different temperature-time combinations were tried for the first part of the annealing procedure (the smoothing of gradients), while they were all followed by a Hg-vacancy procedure of 250 °C for 18-24 h. Then some samples were cleaved, and energy-dispersive x-ray spectroscopy (EDS) line profiles were recorded on the cross-sections to monitor the composition gradients. We could clearly see differences between the profiles from samples with the higher temperature anneal, the lower temperature anneals, and no anneal. Secondary ion mass spectroscopy (SIMS) profiles on two samples verified the EDS results. On another subset of similar samples, planar diodes were processed and resistance-area (RA) values determined. The current-voltage (I-V) curves from the high-temperature annealed samples seemed dominated by leakage current and did generally not display diode characteristics. This could be explained by their EDS profiles, which showed a lot of Hg in the entire passivation layer. The EDS profiles from the three low-temperature annealing procedures were very similar, but planar diode I-V curves revealed diodes of varying quality, and their RA values were used to differentiate among them. The optimal annealing procedure was 300°C for 4 h, followed by 250°C for 24 h.

Key words: HgCdTe, CdTe passivation, anneal, composition gradient, vacancy doping, planar diode

INTRODUCTION

The highest performance infrared (IR) detectors are made of the narrow band gap semiconductor material HgCdTe. In order for the detector to work optimally, it is necessary to protect the HgCdTe surface with a passivation layer that prevents band bending due to surface charges or defects. CdTe has the same crystal structure and almost the same lattice constant as HgCdTe, in addition to a higher band gap of 1.6 eV. It is also less brittle. CdTe is therefore an excellent passivation which can be grown directly on HgCdTe. However, the Hg and Cd interface gradients between HgCdTe and the CdTe passivation layer should be gradual, so that minority carrier electrons will be prevented from reaching the actual interface which may have recombination centers that effectively remove the carriers before they reach the read-out electronics. Therefore it is usual to anneal the material after passivation, which leads to diffusion of Hg and Cd atoms and a more gradual gradient across the interface. The CdTe is often followed by a layer of ZnS, which has an even higher band gap and therefore ensures that the combination has a high resistivity.

We have earlier made planar diodes by ion beam milling Hg-vacancy-doped HgCdTe films grown by molecular beam epitaxy (MBE)[1-3]. Here we report on the same diode architecture in liquid phase epitaxy (LPE) - grown HgCdTe. Whereas the MBE technique allows growth of a CdTe passivation layer *in-situ*, the LPE HgCdTe films must be passivated after the LPE growth. One possibility is to use the MBE machine to grow an epitaxial layer of CdTe layer on top of the LPE-grown HgCdTe detector film. The *as-grown* LPE film will have a significant amount of Hg vacancies due to the high LPE growth temperature ($\sim$ 480ºC). Deposition of the CdTe passivation layer on HgCdTe will also involve heating the sample, although to a much lower temperature, which will lead to some Hg vacancies in the film. After passivation it is therefore necessary to run the samples through an annealing process with a two-fold goal:

i) smooth the gradient in composition at the film-passivation interface and

ii) create a specified Hg vacancy concentration in the material

When a bare HgCdTe film is annealed in a Hg atmosphere, so that Hg can freely diffuse into and out of the surface, the vacancy concentration is determined by the temperature of the system.[4] To fill the vacancies to a concentration lower than the residual background n-type impurity concentration, an anneal at T < 300°C is required.[5] Different laboratories use procedures in agreement with this; for example will 250°C for ~24 h reduce the vacancy concentration below 5×10^{13} cm^{-3}, while 200°C for 120 h will reduce it further to below 5×10^{12}

2

cm^{-3}, which are well below the background n-type doping concentration.[6,7] Higher temperatures will lead to larger vacancy concentrations.

When HgCdTe is passivated by a thick (0.5 μm) CdTe layer and annealed in vacuum, so that no Hg enters or leaves the sample, there is also a balance between vacancy concentration and temperature, although with a different set of values.[4,8,9] Annealing at 250°C for 24 h will in this case result in a Hg vacancy concentration < 3 × 10^{16} cm^{-3}. Destefanis concluded that since the same vacancy concentration is created homogeneously even in thick bulk crystals (in which case it is not necessary with CdTe passivation on the surface), the phenomenon most likely involves some short range reorganization or diffusion (vacancy capture or emission) rather than a long range diffusion process.[8] Presumably the Hg atoms come from/go to interfaces, crystal defects and other local irregularities inside the HgCdTe layer. Another version of this anneal is carried out at 270°C for 20 h in a He atmosphere.[10]

After annealing there are many ways to characterize the change in the CdTe/HgCdTe interface with the different procedures. Pal *et al.* have used thermal evaporation of 2500 Å CdTe plus 500 Å ZnS for the passivation layer. They obtained composition depth profiles by recording consecutive x-ray photoelectron spectroscopy (XPS) spectra in combination with argon-ion sputtering. They have also performed capacitance – voltage (C-V) and photoconductive decay (PCD) measurements to reveal properties such as fixed-charge density, interface trap density and surface recombination velocity, which all affect the quality of the passivation on the HgCdTe film.[11]

Lee *et al.* have also used thermal evaporation to deposit CdTe/ZnS on HgCdTe, and they have investigated the effects of different surface treatments on the electrical properties of the surface with C-V measurements. They conclude that a 1% Br:methanol solution should not be carried out for longer than ~ 1 min. to minimize fixed surface charge density, and air exposure after etching should be avoided as it induces hysteresis in the C-V curves.[12] An *et al.* formed a compositionally graded HgCdTe passivation layer by annealing a HgCdTe p-n junction in a Cd/Hg atmosphere, then adding a ZnS layer. They found an order of magnitude higher resistance-area at zero bias (R$_0$A) values on diodes passivated with this technique than on diodes passivated with thermally deposited CdTe.[13]

We have performed a complementary study, in which we have measured Hg, Cd, and Te energy-dispersive x-ray spectroscopy (EDS) profiles in the scanning electron microscope (SEM) and the smoothing of these profiles with different annealing procedures. The profiles give an immediate impression of how much diffusion has taken place at the interface, and they are easier to perform than XPS profiles that require sputtering between

3

each depth.[11] To further optimize the annealing procedure for similar composition profiles, we have measured an important device property which depends directly on the quality of the passivation, namely diode resistance-area (*RA*) values, for planar diodes processed on CdTe/HgCdTe films. Thus optimizing *RA* values leads directly to a better annealing procedure for ion milled planar diodes on Hg-vacancy-doped HgCdTe, and the results are presented here. This procedure is different from the procedures described in Refs. 11 and 13.

EXPERIMENTAL DETAILS

Several 30×30 mm^2 Hg$_{1-x}$Cd$_x$Te films with different *x*-values and with indium *n*-type doping $\sim 1 \times 10^{14}$ cm^{-3} - 1×10^{15} cm^{-3}, were grown by the LPE tipping technique (Te-rich LPE). In order to grow an epitaxial passivation layer on top of HgCdTe, we used an MBE machine. The entire film (or part of a film) was etched 2 - 10 μm in a Br:Methanol solution to leave the HgCdTe film approx. 15 μm thick. The film (or part of a film) was then quickly loaded into the Riber 32P MBE machine and transferred into a separate chamber and cleaned with atomic hydrogen (aH). We have in a previous x-ray photoelectron spectroscopy (XPS) study shown that aH removes oxygen atoms from the surface of HgCdTe at low temperatures ($<$ 80°C).[15] Furthermore, the measurements showed that the HgCdTe surface becomes Te-rich and with a decreased *x*-value after a Br:Methanol etch. While aH removes the extra Te, it also leaves the surface with an increased *x*-value. Carbon is not so easily removed by aH, but heating the sample above 200°C before growth will remove a lot of the carbon.

After aH cleaning, the film was transferred to the growth chamber. In order not to degrade the surface, the films were heated with a Hg flux incident on the surface until the growth of the CdTe passivation layer started. A CdTe and a Hg source were used in this process, and approx. 0.5 μm CdTe was grown at 260°C with a growth rate of 75 Å/min. Figure 1 shows an x-ray diffraction (XRD) scan across the <444> direction of a sample with a grown passivation layer which has been annealed at low temperature (300°C for 4 h followed by 250°C for 24 h). There are distinct peaks from CdTe and HgCdTe, showing that the passivation layer is crystalline and epitaxial.

Smaller samples were cut from the passivated films and placed on a quartz plate in a quartz tube. The tube was placed in an oven and mounted onto a small vacuum chamber with a turbopump. The pump evacuated the tube and pumped on it during the entire annealing process. From the phase diagram of Vydyanath and our previous work with MBE-grown HgCdTe, we have found that part ii) above is obtained by annealing at 250°C for 18-24 h in vacuum.[4,1] We did not find any difference between samples annealed at

4

18 or 24 h, which is in agreement with Ref. 8, but we decided to use the longer time of 24 h to be consistent with other groups. (Part i) will need a higher temperature than part ii) since we want diffusion of Cd and Hg over a longer distance. We tried four combinations of anneal temperature and anneal time for part i), shown in Table I, with the aim to smooth the Hg and Cd gradients at the interfaces. All four combinations were followed by part ii), as described above, to create a vacancy concentration of $1 - 2 \times 10^{16}$ cm^{-3} throughout the film. To investigate the amount of smoothing a particular procedure created, we cleaved the samples and recorded EDS line profiles from the substrate to the top of the passivation layer in a Hitachi SU6600_VP FEG SEM with a Bruker XFlash5010 spectrometer. We used mostly an acceleration voltage of 10 kV as this is high enough to cover all the relevant peaks but does not completely ruin the resolution. The depth and width from which x-rays can emerge increases very fast with electron energy. For 10 kV the x-ray diameter is roughly 0.4 µm. It is also possible to use 5 kV, but then the count rate becomes very low. The line profiles were accompanied by point spectra from the HgCdTe film, the middle and the top of the passivation layer to find the composition with higher accuracy. We sent two samples to Evans Analytical Group for secondary ion mass spectroscopy (SIMS) measurements to check the validity of the EDS compositions. Hall measurements gave the carrier concentration and mobility for all the different types of samples. The EDS profiles were very similar for the three low temperature annealing procedures. We then optimized further by processing planar diodes and determining *RA* values.

The diodes were linear arrays of 32 96 ×71 µm^2 and/or 64 26 × 26 µm^2 diodes. Figure 2 shows a schematic drawing of a diode. The diodes are made by etching openings in the passivation layer and ion milling these to create a p-n junction approx. 8 µm down. The p-n junction will extend approx. half of its depth – 4 µm – laterally outside the opening in the passivation.[3] The milling was immediately followed by deposition of Cr/Au contacts. To save time and effort, the fabrication process was usually carried out to include the steps of making the diodes and the p-type common contact and in some cases depositing 200 nm ZnS. Then the diode I-V characteristics at 77 K were measured in a modified probe station which allows > 1 hour of measuring time in air and ambient room light before ice freezes on the surface. If the I-V curves were good, the remaining steps of sputtering Au lead-out wires and bonding were carried out, and the I-V curves were measured in a cryostat at 77 K. We have earlier shown that measuring I-V curves in ambient light may lower the *RA* values, and this is probably due to a bias-induced modulation of the collection efficiency, analogous to the Early effect in bipolar transistors.[1] Therefore, the RA values for samples measured in the probe station are listed in Table 1 as larger than (>) the actual value found.

5

RESULTS AND DISCUSSION

Before anneal

To have a basis for comparison, we measured EDS profiles in passivated, non-annealed films. We cleaved small 5×5 mm^2 samples and mounted them in the SEM. Figure 3 shows SEM images of the cross-section of (a) the whole HgCdTe layer, and (b) just the passivation layer with higher magnification in an *as-grown* sample (no anneal). We drew the arrows where we wanted the line scans. Figs. 3c and 3d show the line profiles of Cd, Hg, and Te recorded along the arrow in the narrow images below the graphs. At the film-passivation interface, the Hg intensity falls steeply, and it continues to fall throughout the passivation layer, but it does extend to the surface, although with a very small value. The Cd profile increases steeply at the interface and decreases again steeply at the surface. Figure 4 shows point spectra from the middle of the HgCdTe film and the middle of the passivation layer in a similar non-annealed sample. These give an *x*-value of 0.27 in the HgCdTe film, while there is 3 at % Hg in the middle of the passivation layer. The amount of Hg in the different films is listed in Table I.

Hot anneal

We first tried annealing at 360ºC for 4.5 h followed by 250ºC for 24 h, all in vacuum, and planar diodes were processed on several samples. We then measured I-V curves and found that most of them did not display diode characteristics; with the exception of a few poor diodes most of the curves seemed dominated by a small 'shunt' resistance. Figure 5a shows three I-V curves from sample 222-1: a poor diode (diode 1), a diode dominated by a small resistance (diode 2) and a similar curve measured with one probe on the p-side common contact and the other probe on the passivation near diode 2 (Pas 2) instead of on the n-type diode contact. The curves from diode 2 and from Pas 2 are very similar, so it seems that the passivation layer contributes a low-resistance parallell path to conduction through the p-n junction and that this leakage current dominates the I-V curves for most of the diodes on samples with hot anneal. To understand these results, we cleaved some of the samples and measured EDS profiles on the cross-sections. Figure 6 shows SEM images of the cross-section of (a) the HgCdTe film, and (b) the passivation layer with higher magnification, in a sample that had undergone hot anneal. Figs. 6c and 6d show the line profiles of Cd, Hg and Te recorded along the arrow in the narrow images

6

below the graphs. The cleaved surface is not completely smooth in this sample, but we have managed to avoid large features, and corresponding topographic spikes, in the recorded line profiles. While the Hg profile in Fig. 3d was lower than the Cd profile almost throughout the passivation layer, and it fell continuously through the passivation layer, the Hg profile in Fig. 6d decreases somewhat towards the interface, then stays constant (and higher than the Cd profile) until it falls off at the surface. Cd has a very smeared-out profile at the film-passivation interface. Figure 7 shows point spectra from the middle of the HgCdTe film and the middle and top of the passivation layer. These give an x-value of 0.29 in the HgCdTe film, while there is 15 at% and 12 at% Hg in the middle and top of the passivation layer, respectively. In other words, the passivation layer has become a HgCdTe layer with x-value ranging from 0.29 (film interface) via 0.7 (middle) to 0.76 (top). We can compare this to the line profiles from the *as-grown* film in Fig. 3d, which has 1.6/0.5 at% Hg in the middle/top of the passivation layer. It is also clear that the rather steep line profiles at the interface in Fig. 3d have become very smeared out in Fig. 6d.

The resistance of such a layer will be reduced compared to that of a CdTe layer, and when in parallel with the p-n junction, it can dominate the current through a device. The Cr/Au that is sputtered on the diode immediately following ion milling is deposited at a 45° angle, so that it should reach most of the CdTe side walls after the Br:methanol etch.

Low temperature anneals

We then tried several lower temperature variations on the first part of the anneal, namely

LT1: 325 °C for 1.5 h

LT2: 300 °C for 4 h

LT3: 300 °C for 2 h.

After using these anneal parameters, we could see that the profiles were a bit smoother than in the non-annealed samples, but nowhere near the smeared 'hot-anneal' profiles. Figure 8 shows SEM images of the cross-section of (a) the HgCdTe film and (b) the passivation layer with higher magnification in a sample which had gone through annealing procedure LT2. Figs. 8c and 8d show the line profiles of Cd, Hg and Te recorded along the arrow in the narrow images below the graphs. The cleaved surface was a bit rough in this sample, and therefore the line profile through the film is not level. However, the surface is quite smooth over the passivation layer, and the line profiles here do not seem to contain any topographic information. We get the composition of the film from the point spectra seen in Figure 9.

7

Comparing Figs. 3d, 6d and 8d, we find that the line profiles of Cd and Hg at the interface are steep in non-annealed, more gradual in the LT2 sample, and very smeared out in the hot annealed sample. The profiles of the three low-temperature anneals were quite similar, so to further optimize the annealing procedure, we processed planar diodes and compared RA-values to determine the best annealing process. The results are listed in Table 1, and some I-V curves are shown in Figure 10. We thus found LT2 to be the best annealing procedure. Figure 11 shows the Cd and Hg line profiles for two samples with (a) no anneal and (b) LT2 anneal, respectively. To better see the profiles, the scans have been slightly smoothed (3 pt adjacent-averaging). The curves for both Cd and Hg are clearly more gradual after LT2. Similarly, we can see small differences in the SIMS profiles of two similar samples (non-annealed and LT2 annealed, respectively) in Figure 12, both in x-value and shape of profile, with the annealed sample having smoother transitions between the different regions.

We finally processed Hall clovers on some of the samples and measured hole carrier concentrations in the range $0.7 - 2 \cdot 10^{16}$ cm^{-3}. These are also listed in Table 1. We have included Hall measurements on films that have been annealed in Hg atmosphere to fill in the Hg vacancies for completeness. Thus, among the annealing procedures tried here, the one which gave the best I-V characteristics of planar diodes on Hg-vacancy-doped HgCdTe films passivated with CdTe *ex-situ*, was a vacuum anneal with the combination 300ºC for 4 h followed by 250ºC for 24 h.

CONCLUSION

A good annealing procedure for making the HgCdTe /CdTe passivation interface more gradual and creating vacancy doping with a carrier concentration $0.7-2\times10^{16}$ cm^{-3} was found to be 300ºC for 4 h followed by 250ºC for 24 h. The CdTe passivation layer protects and prevents depletion of Hg atoms from the HgCdTe film. EDS line profiles can be used to determine the smoothing that results from different annealing procedures, but to determine which procedure is best among similar low-temperature anneals, diode characteristics such as RA values must also be used.

REFERENCES

1. R. Haakenaasen, H. Steen, E. Selvig, T. Lorentzen, A.D. van Rheenen, L. Trosdahl-Iversen, H. Syversen, D. Hall and N. Gordon, *J. Electron. Mater.* 34, 922 (2005).

2. R. Haakenaasen, H. Steen, T. Lorentzen, L. Trosdahl-Iversen, A.D. van Rheenen and H. Syversen, *J. Electron. Mater.* 31, 710 (2002).

3. R. Haakenaasen, T. Moen, T. Colin, H. Steen and L. Trosdahl-Iversen, *J. Appl. Phys.* 91, 427 (2002).

4. H.R. Vydyanath, *J. Cryst. Growth* 161, 64 (1996).

5. P. Capper, *Properties of narrow Gap Cadmium-based Compounds*, Emis Data Reviews Series No. 10, ed. P. Capper (INSPEC, UK, 1994), p. 151.

6. H.F. Schaake, *J. Electron. Mater.* 14, 513 (1985).

7. B. Pelliciari, *Prog. Cryst. Growth Charact.* 29, 1 (1994).

8. G.L. Destefanis, *J. Cryst. Growth*, 86, 700 (1988).

9. A. Takami, Z. Kawazu, T. Takiguchi, K. Mitsui, K. Mizuguchi, T. Murotani, K. Yasumura, T. Kanno, and M. Saga , *J. Cryst. Growth*, 117, 16 (1992).

10. P.A. Bakhtin, S.A. Dvoretskii, V.S. Varavin, A.P. Korobkin, N.N. Michailov, I.B. Sabinina, and Y.G. Sidorov, *Semiconductors* 38, 1172 (2004).

11. R. Pal, A. Malik, V. Srivastav, B.L. Sharma, V.R. Balakrishnan V. Dhar, and H.P. Vyas, *IEEE Trans. Electron Devices* 53, 2727 (2006).

12. T.S. Lee, K.K. Choi, Y.T. Young, H.K. Kim, J.M. Kim, Y.H. Kim, J.M. Chang, W.S. Song, S.U. Kim, M.J. Park, S.D. Lee, *J. Electron. Mater.* 26, 552 (1997).

13. S.Y. An, J.S. Kim, D.W. Seo, and S.H. Suh, *J. Electron Mater.* 31, 683 (2002).

14. L.S. Hirsh, R. Haakenaasen, T. Colin, K.S. Ziemer, C.D. Stinespring, S. Lovold, and T.H. Myers, *J. Electron. Mater.* 28, 810 (1999).

FIGURE CAPTIONS

Fig. 1. XRD scan around the 444 reflection of a sample with a grown passivation layer. The sample has been annealed with the optimal (low temperature) procedure found in this study. The distinct peaks from CdTe and HgCdTe show that the passivation layer is epitaxial.

Fig. 2. Schematic drawing of a planar diode. The p-n junction extends approx. 8 µm down and 4 µm laterally.

Fig. 3. Sample before anneal. SEM overview images of the cross-section of (a) the HgCdTe layer and (b) the CdTe passivation layer at higher magnification. The arrows are placed where we wanted the line profiles. (c) and (d) recorded EDS line profiles of Cd, Hg and Te along the arrows in (a) and (b) . Below the line profiles are narrow images around the actual scan location.

Fig. 4. Point spectra from HgCdTe film and middle of passivation in a sample before anneal.

Fig. 5. Measured I-V characteristics of diodes on samples that had undergone 'hot' anneal. Most of the I-V curves did not display diode behavior, but were dominated by leakage current through the passivation layer.

Fig. 6. Sample after hot anneal. SEM overview images of the cross-section of (a) the HgCdTe layer and (b) the CdTe passivation layer at higher magnification. The arrows are placed where we wanted the line profiles. (c) and (d) recorded EDS line profiles of Cd, Hg and Te along the arrows in (a) and (b). Below the line profiles are narrow images around the actual scan location. The cleaved surface is a bit rough, but we have placed the scan arrows in regions without many features in order to avoid topography influence on the scan intensity.

Fig. 7. Point spectra from HgCdTe film, middle of passivation, and top of passivation in a sample after hot anneal.

Fig. 8. Sample after LT2 anneal procedure. SEM overview images of the cross-section of (a) the HgCdTe layer and (b) the CdTe passivation layer at higher magnification. The arrows are placed where we wanted the line profiles. (c) and (d) recorded EDS line profiles of Cd, Hg and Te along the arrows in (a) and (b). Below the line

10

profiles are narrow images around the actual scan location. As the cleaved surface was a bit rough, the line scan across the layer has topography features in addition to composition information. The passivation scan was placed in a smooth region and should be free from topography (except at the surface).

Fig. 9. Point spectra from HgCdTe film and top of passivation in a sample after the LT2 anneal procedure.

Fig. 10. I-V characteristics of diodes on a sample that had been annealed with procedure LT2.

Fig. 11. Slightly smoothed EDS profiles of a sample before anneal and a sample after LT2 (optimized anneal procedure) for (a) Cd and (b) Hg. The smoothing consisted of 3 pt adjacent-averaging.

Fig. 12. Cd (x) and Hg (1- x) SIMS profiles in a sample before anneal and a sample after LT2 (optimized anneal procedure).

11

Table I: Summary of measured properties on samples undergone different annealing procedures

Sample	Anneal type	FTIR x-value	d_{CT} (μm)	EDX x-value middle HgCdTe film	Hg middle of passivation (at%)	Hg top of passivation (at%)	Hall 77 K p (10^{16} cm^{-3})	Hall 77 K μ (cm^2/V-s)	$R_{max}A$ (Ω cm^2)
468 -1	n-type	0.23					0.024	189000	
448-1	n-type	0.28					0.024	88900	
035-1	None	0.27					52	240	
132-9	None	0.27	0.46	0.27	4	<1			
222-5b	None	0.28	0.45	0.29	4	1			
124ann-3	Hot	0.27	0.57				0.65	510	-
222ann-14	Hot	0.29	0.45				0.81	440	
132ann-10	Hot	0.27	0.46	0.29	15	12	2.1	50	
132ann-7a	Hot	0.26	0.46	0.26	22	10			
222ann-5	Hot	0.28	0.45	0.30	15	12			
038ann-A5	LT1	0.26				1.5			30
222ann-8	LT1	0.29	0.45		4	1.4			80
205ann-A4	LT2	0.29					2.2	580	
132ann-9	LT2	0.27	0.46	0.29	3-4	1.6	0.94	560	
222ann-12	LT2	0.29	0.45	0.30	3	1.4	0.70	490	
232ann-A5	LT2	0.32							>5×10^5
205ann-B2	LT2	0.29							>10^5
147ann-A4	LT2	0.23							1800
222ann-4	LT3	0.29	0.45						9
038ann-B7	LT3	0.26							1.5

Vacuum anneals: Hot: 360ºC/4.5h + 250ºC/18h   LT1: 325°C/1.5h + 250ºC/18h   LT2: 300°C/4h +250ºC/18h   LT3: 300°C/2h + 250ºC/18h
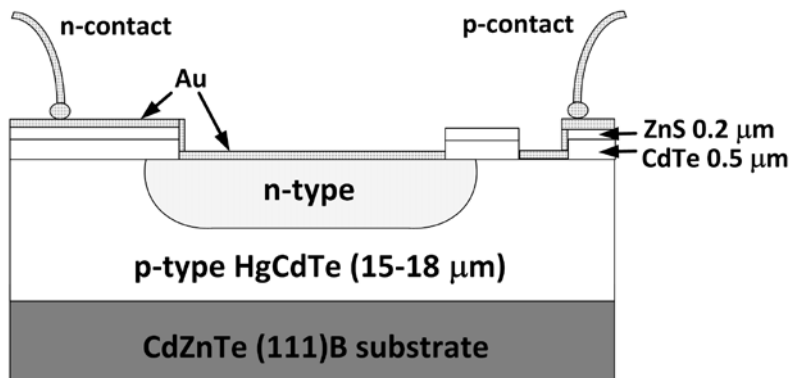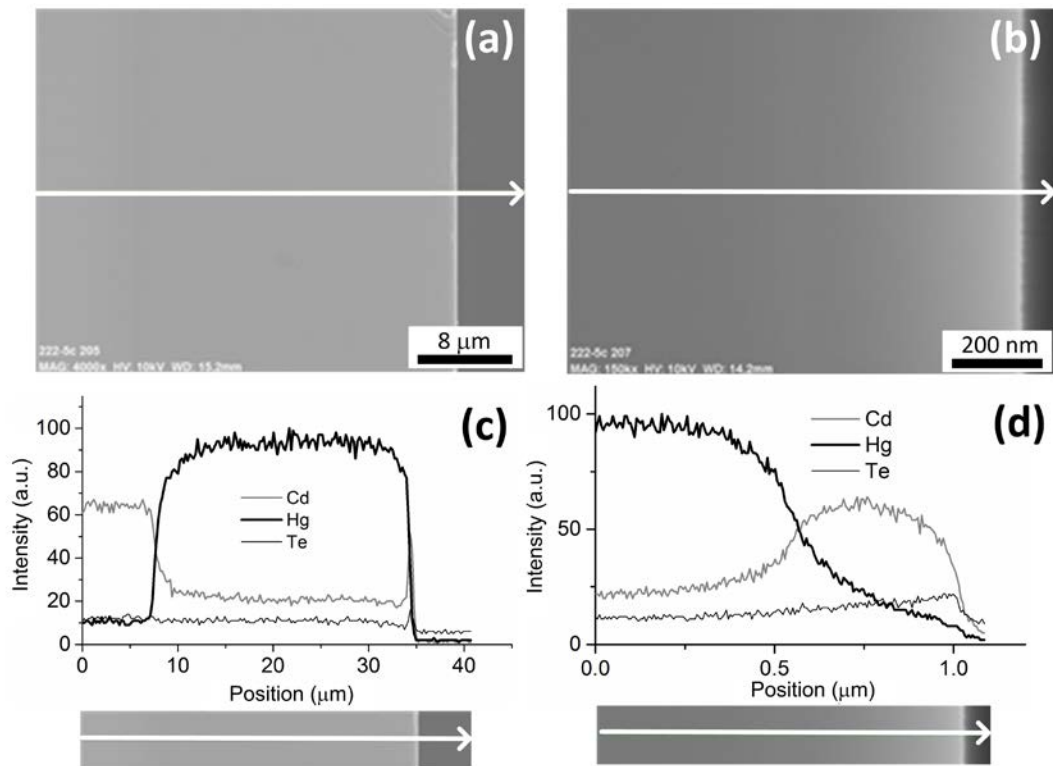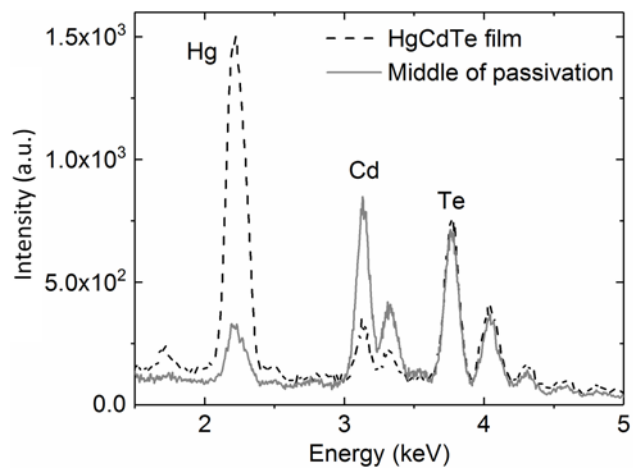n-type in Hg atm: 200ºC/120h in Hg atmosphere
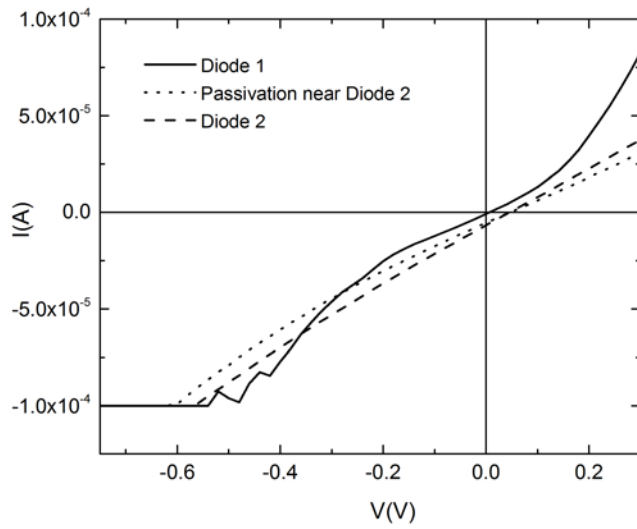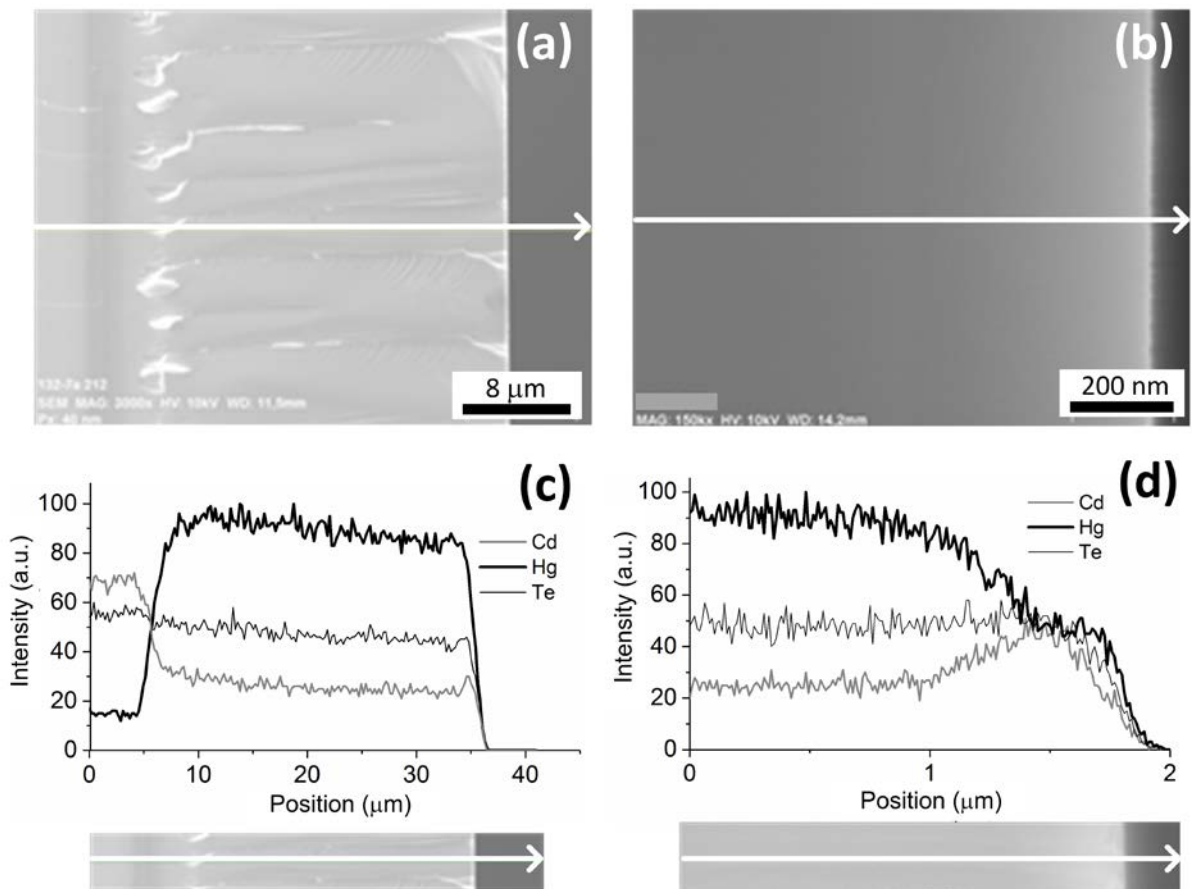
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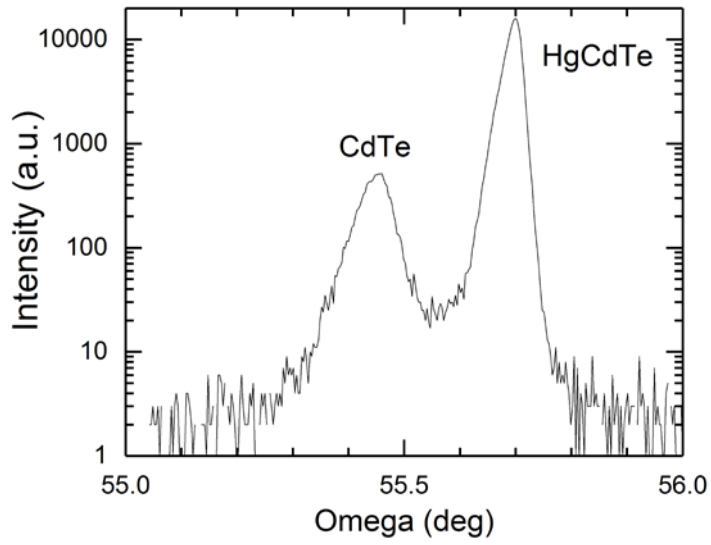
Figure 2.

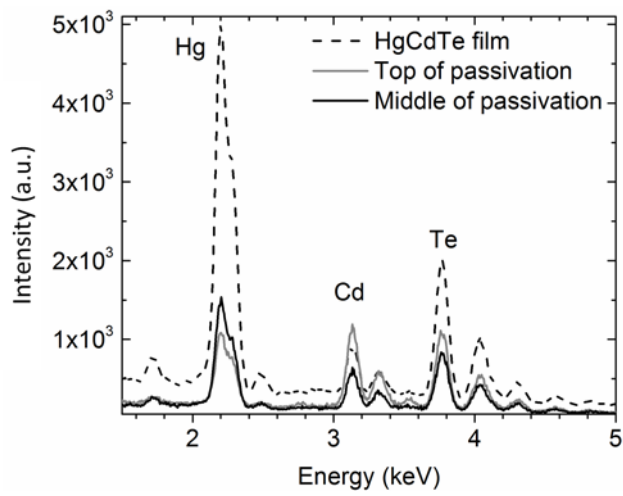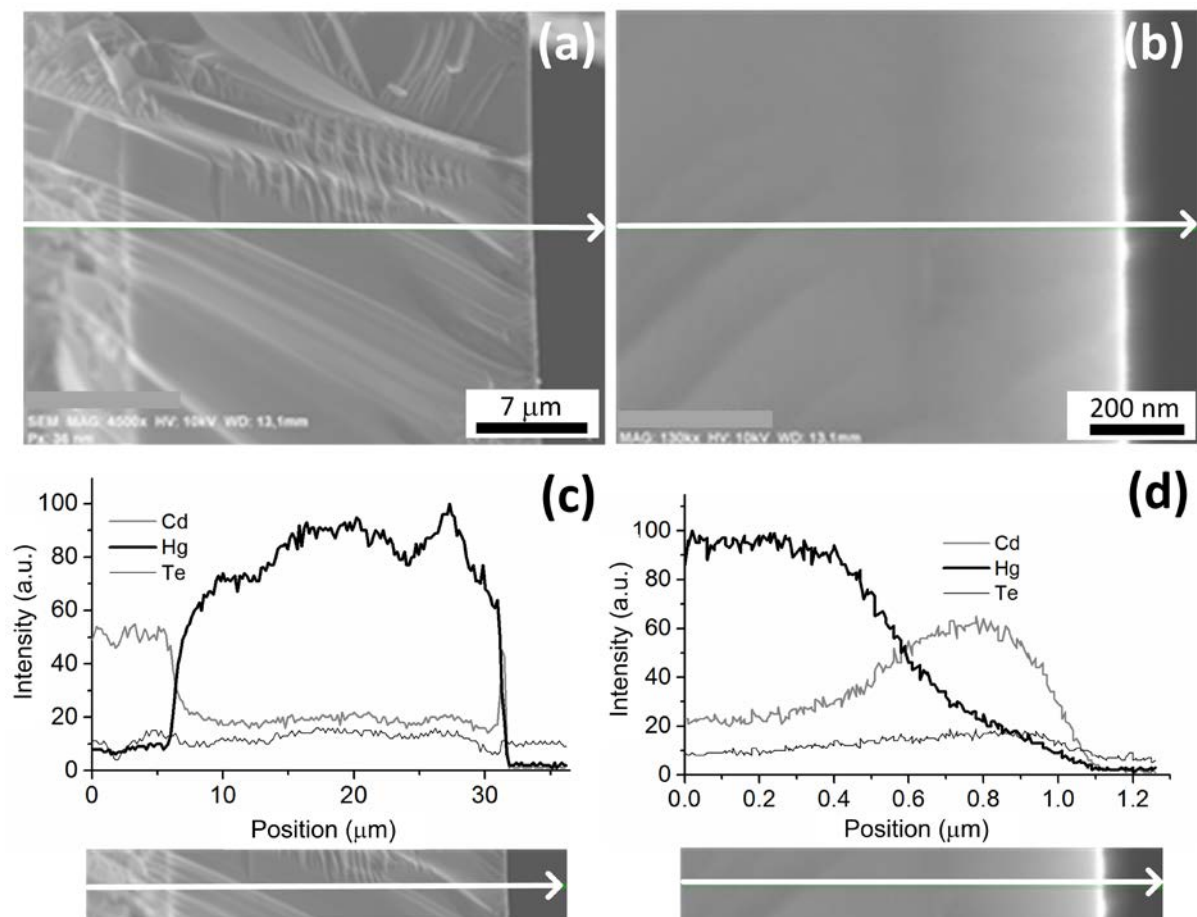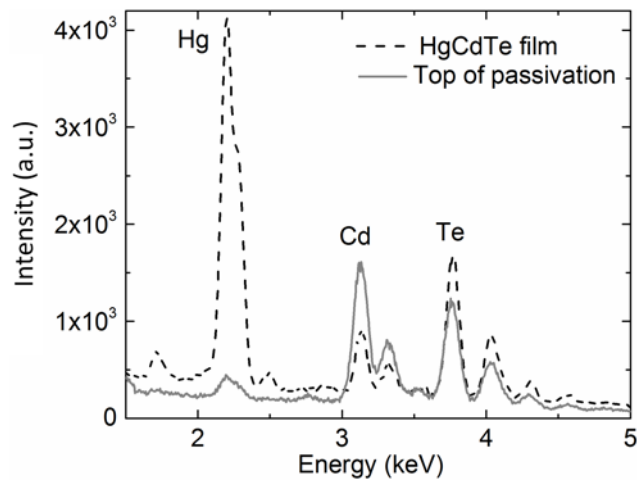Figure 3.
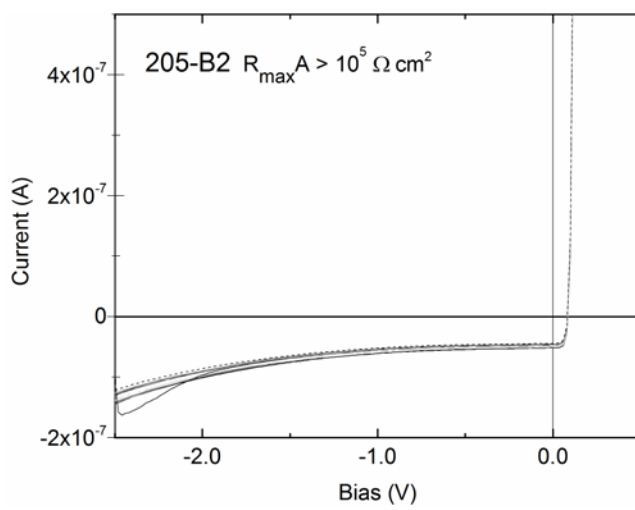

Figure 4.
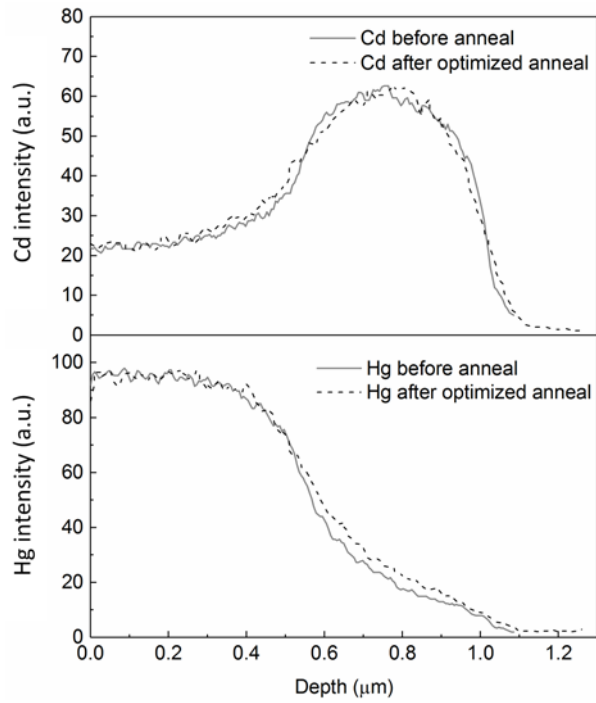

13

Figure 5.

Figure 6.

Figure 7.

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Figure 9.

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Figure 11.

Figure 12.